

Introduction

Memory is an important, essential and integral part of a system to process any information, whether a machine or a human. The current computation systems are based on von Neumann architecture as shown in figure 1.1 where the computation and storage units are physically separated as the central processing unit and memory unit [Nawrocki et al., 2016]. The location of stored data in the memory unit allowed the processing unit to fetch the data for computation. Over the last 50 years, the revolution in the field of data computing and information technology has significantly increased the demand for efficient memory devices. Further, the technological advancements in machine learning and artificial intelligence and their extensive use in modern life need a compact, denser, efficient and big data storage solution [Seo et al., 2011]. Currently, the conventional MOSFET based memory technology is widely accepted to mitigate computing and storage applications. The MOSFET-based static random-access memories (SRAM), dynamic random-access memories (DRAM) and flash memories are used in current for data storage and computing [Deshmukh et al., 2005].

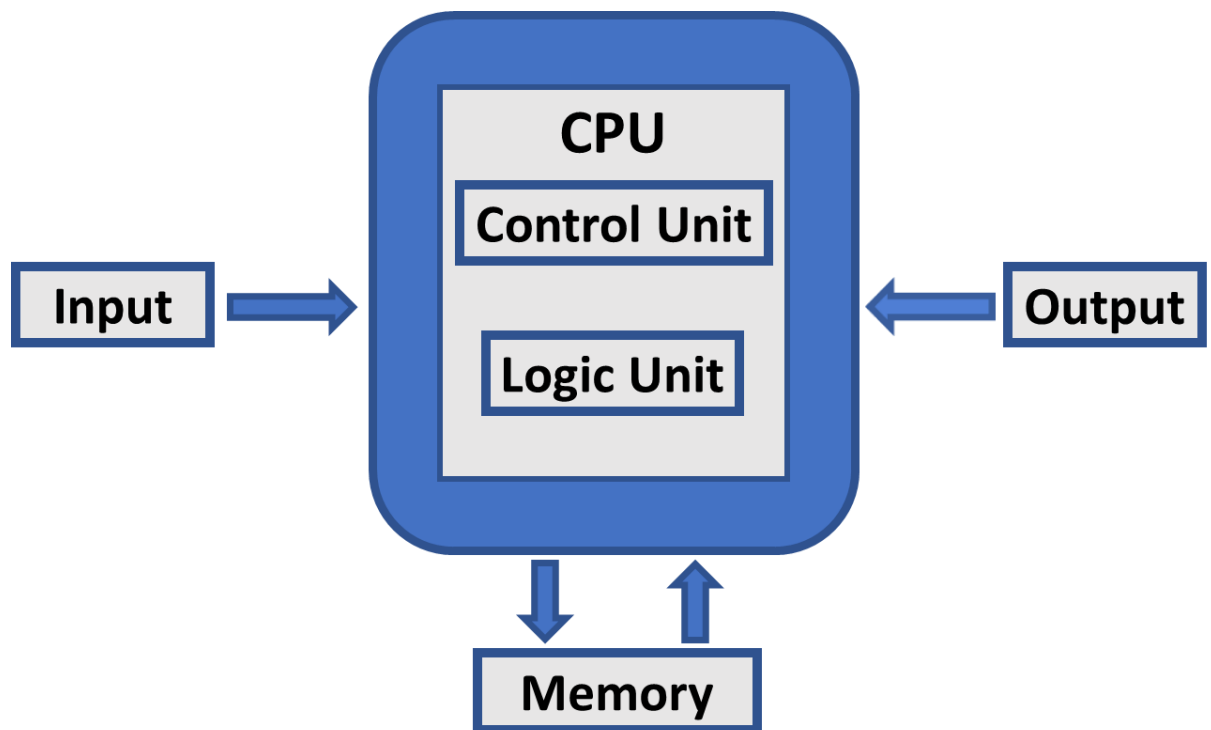


Figure 1.1: Von-Neumann architecture

The data explosion due to the advancement and availability of communication technology like 4G and 5G to the extended population has dramatically increased the demand for fast and large data storage. On the other hand, the internet revolution has generated explosive growth in the data storage of electronic devices including mobile, laptops and computers as well as commercial data centres and server farms for entertainment and various

media platforms. Currently, the NAND-based flash memory technology is being employed as a low-cost solution to meet the high density and fast storage demand due to an outburst in the demand for electronic devices [Wang et al., 2016b]. The flash memory devices store the data in the form of electric charges within a floating gate embedded with a gate stack of a field effect transistor and an oxide layer to isolate the floating gate. The floating gate flash suffers from draining off the charges due to shorting and to overcome this issue a thin layer of Si_3N_4 is employed as a charge-trapping layer [Wu et al., 2016]. Considering the current scenario and to mitigate the increased demand of data storage requirements in future the research momentum of fertility gat shifted towards the emerging non-volatile memory technologies like ferroelectric random-access memories (FeRAM), resistive random-access memories (RRAM), spin transfer torque magnetoresistive random-access memories (STT-MRAM) and phase change random-access memories (PCRAM) [Ishimaru, 2018; Ishiwara, 2012]. All these emerging memory technologies have the potential to mitigate future memory requirements as an efficient option for flash and DRAM as main memory.

1.1 Challenges Associated with Current Memory Technologies

The current silicon-based memory technology has followed Moore’s law scaling but now they are facing the downscaling limit. Hence it is believed that Moore’s law will not abide by the current memory technology in the next few years. The research focused to address the issues like power consumption and downscaling limit with current memory technology by developing capable alternative memory technologies [Freitas et al., 2008]. Further, in-memory computation is a major requirement for a fast and efficient system to overcome the bottleneck of current computer architecture where separate processing and memory units are required [Chu et al., 2017]. These separate units and their operation gap form a memory wall and significant power consumption and time taken for data transfer only in comparison to computation time.

The new and emerging non-volatile memory technologies like STT-MRAM, PCRAM, FeRAM and RRAM have the potential to be employed as compact, denser, energy-efficient and high-speed solutions over the current memory technology. These emerging technologies are capable to reduce the distance between data and computation in traditional memory hierarchy to solve the bottleneck of von Neumann architecture.

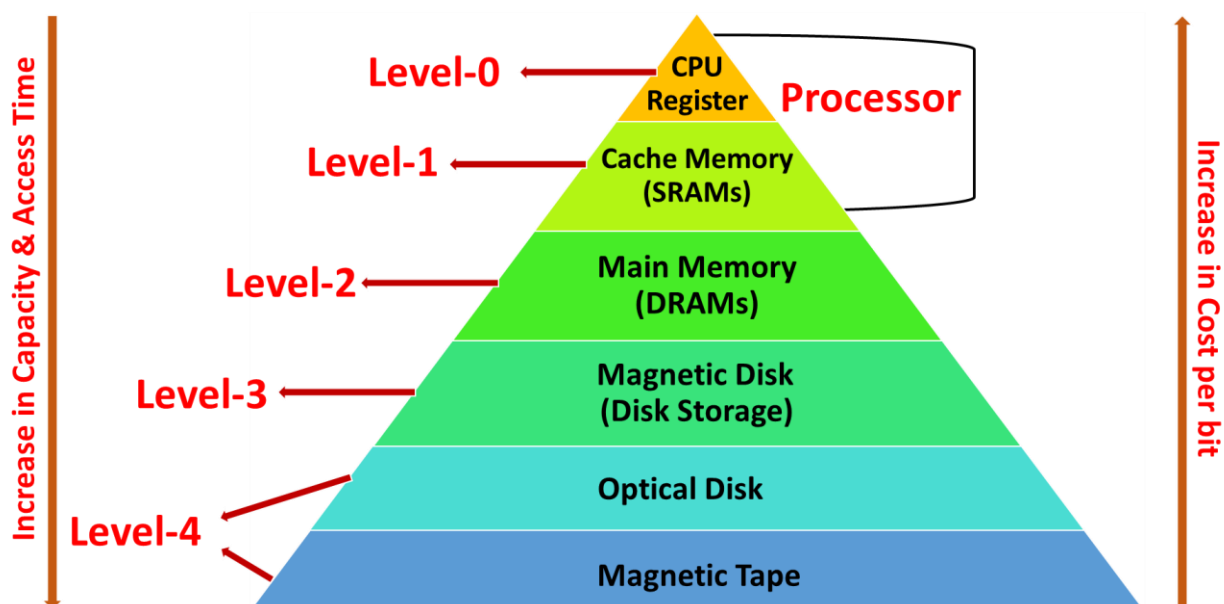


Figure 1.2: Memory hierarchy with their speed and cost comparison.

1.2 Classification of Memories

Semiconductor memories are classified in two broad categories based on their retention capabilities as volatile memories and non-volatile memories (NVM). The volatile memories are able to retain the stored data until the availability of an applied field across it while NVMs are able to retain data for a long time and do not require any supply to retain stored data. In the conventional memory architecture, as illustrated in figure 1.2, the different types of memories are in use for different applications in the system [Spaanenburg et al., 2016]. The memories are assigned to the different applications based on their speed, storage capacity, volatility and cost. We can see in figure 2 that as we move to the top in the hierarchy the access time is very low and the cost per bit is high. Hence to reduce the cost of the system the data transfer takes place between the NVNs and the computational memories.

1.2.1 Volatile Memories

The definition of volatile memory confirms that it requires continuous power to be in operation and hence can only be used as computational or primary memory. The volatile memories are of two types; dynamic random-access memory (DRAM) and static random-access memory (SRAM). The simple architectural representation of typical SRAM and DRAM cells is shown in figure 1.3 (a-b). The ultra-fast operation (0.3 ns) and higher programming cycles offered by SRAM makes it suitable to use as cache memory but the expensive and complex fabrication limits its use as main memory [Jeong et al., 2012]. The SRAM suffers from lower integration density due to the large feature size. The DRAM is widely employed as the main memory component in a computer system centered on Von Neumann's architecture. A typical DRAM cell has a simple architecture that comprises one transistor-one capacitor (1T-1C) and the stored bit "1" or "0" is defined by the charge and discharge of the capacitor [Siddharth et al., 2018]. The integration density of DRAM is higher in comparison to SRAM due to the lower feature size but it has higher latency than SRAM. The power consumption in a DRAM is very high as have a shorter retention time and needs to be refreshed regularly during the computation.

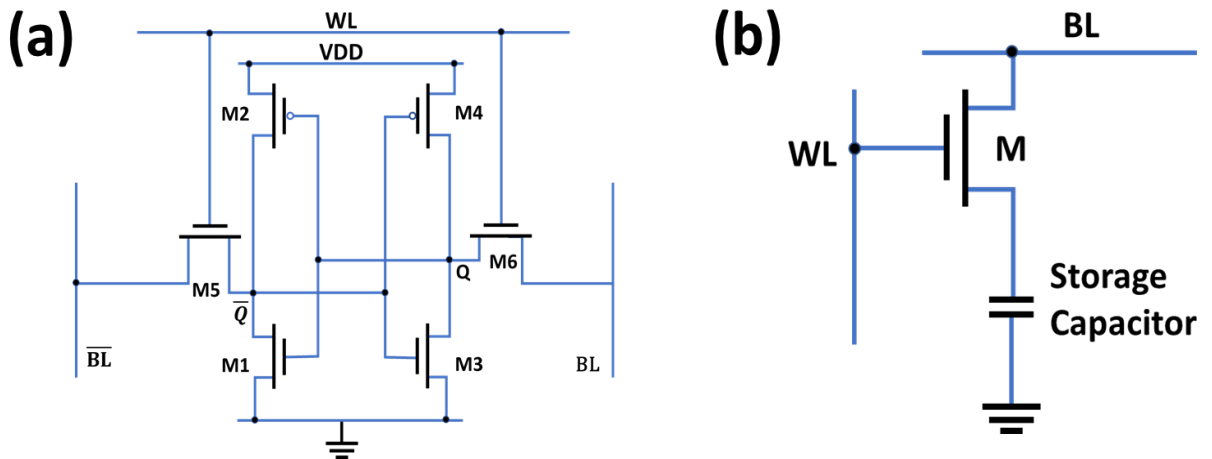


Figure 1.3: (a) Conventional 6T SRAM cell architecture. (b) Typical DRAM cell.

1.2.2 Non-volatile Memories

The non-volatile memories can hold the stored information or bit even after the removal of the applied field. Hard disk drives (HDDs) and flash memories are typical examples of NVM. The HDD is also known as magnetic disk drive as the information bit is stored in form of a magnetic field. The HDDs offer a high storage capacity but the weight, high power consumption, latency and the use of mechanical components are the major issues. HDDs served the systems for a long time but as time progressed flash memories have replaced the HDDs for efficient and high-performance systems as flash memory offers the advantages like lightweight,

less power consumption, fast read/write operations, less fragile and compact in size. The above-mentioned advantages of flash memories are able to address the current requirement of fast, lightweight and energy-efficient systems.

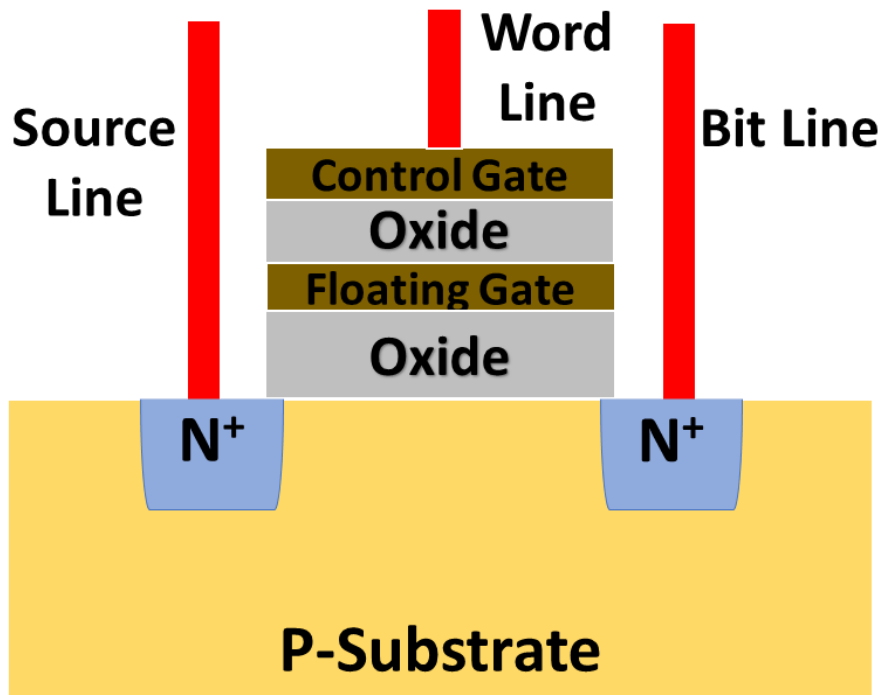


Figure 1.4: Schematic representation of floating gate Flash memory.

Typical flash memory is composed of a MOSFET with a floating gate and a layer of blocking oxide for insulation as shown in the figure 1.4. The flash memories are programmed to store data in the form of accumulated charge in a floating gate and trapped charge can be retained for years. The erasing operation is performed Fowler-Nordheim (FN) tunnelling that discharges the charges to the MOSFET channel. The stored charges govern the read operations. To read the stored data a low voltage is applied to the control gate. The applied read voltage is low enough that it doesn't change the amount of stored charge and can differentiate between charged and uncharged states. The current flash memory technologies are classified as NOR-based and NAND-based flash memories. Both NOR and NAND-based flash memories have their own advantages and disadvantages [Wang et al., 2014]. NAND-based flash memories have advantages like less area consumption, and fast write and erase operations make it a better option over NOR-based flash. NAND-based flash memories offer a very high storage capacity to be employed in secondary storage devices like flash drives, memory cards and hard drives. The floating gate flash memories have an issue of leakage current if the thickness of blocking oxide is reduced and hence the charge drain takes place. To overcome the issue of charge drain, the silicon-oxide-nitride-silicon (SONOS) flash memories are used as an extended version of floating gate flash memories [Chou et al., 2009]. The use of this architecture further reduced the gate stack thickness by 50% and lesser leakage current made the write and erase operations faster.

1.3 Emerging Non-volatile Memory Technologies

The current silicon-based memory technologies are facing the issue of downscaling limits as they will not be able to abide by Moore's law in the next few years. In such a scenario the scientific community is dedicated to exploring other alternative memory solutions to develop a scalable, fast, energy-efficient, CMOS-compatible and cost-effective memory technology. The estimated growth in memory market is expected to have ~45% compound annual growth rate (CAGR) of and will reach a valuation of \$8 billion by 2025.

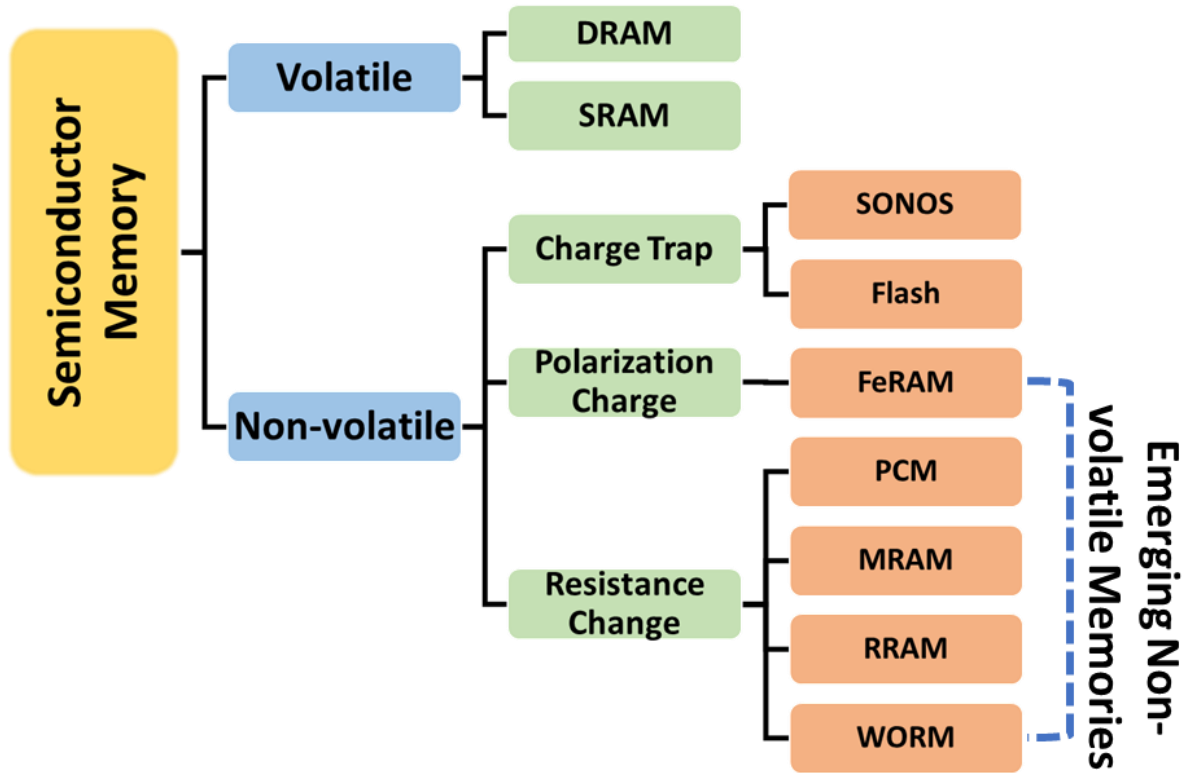


Figure 1.5: Classification of semiconductor memories.

The classification of semiconductor memories is given in figure 1.5. The four major NVM technologies evolved in the last few years and are being explored as an alternative to current memory technology, these are STT-MRAM, FeRAM, PCRAM and RRAM. The global players in the domain of memory and semiconductor devices such as TSMC, Micron, Global Foundries, Sony, Hewlett Packard, Intel, Western Digital, Samsung, Toshiba, Crossbar, Hynix, Fujitsu, IBM and many others have already started the scalable production of some of these technologies; however, the research is still going on to improve the performance and efficiency of these technologies. The researchers are still exploring the materials and the fabrication process to develop scalable, high-density, fast and cost-effective NVM technology [Wang et al., 2015].

1.3.1 Ferroelectric Random Access Memory (FeRAM)

FeRAMs are polarization change-based memory device which consists of a thin film of ferroelectric material (generally metal oxides) sandwiched between the bottom and top electrodes [Ishiwara, 2012]. The figure 1.6 (a) shows the schematic representation of a typical FeRAM memory cell. HfO_2 , HfZrO_2 , $\text{Pb}_{1-x}\text{Zr}_x\text{TiO}_3$ (PZT) and $\text{SrBi}_2\text{Ta}_2\text{O}_9$ (SBT) are the most popular materials explored for FeRAM and its scalable production. The applied electric field across the device causes ionic polarization in the ferroelectric layer of the device [Fan et al., 2016]. This ionic polarization is irreversible even after the removal of the electric field due to the ferroelectric properties of the material and this remanent polarization is termed as polarization hysteresis shown in figure 1.6 (b). Both the positive and negative states of polarization represent the two distinct states of memory. The reversal of polarization takes place when the applied field is reversed. The read process is destructive due to the application of positive write voltage to read the state in terms of current which limits the speed of operation. FeRAM offers fast read and write operations but the scalability is the issue to be addressed.

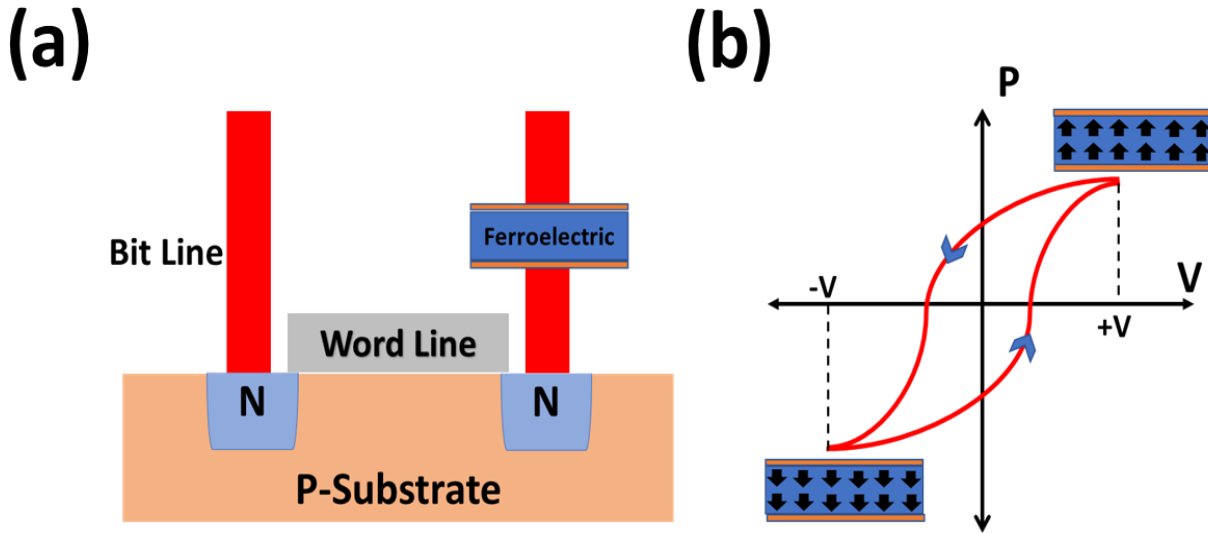


Figure 1.6: (a) Device structure of a FeRAM device. (b) Representation of polarization versus voltage curve for a FeRAM. The direction of polarization saturation indicates the '1' and '0' states.

1.3.2 Spin-torque Transfer Magnetic Random Access Memory (STT-MRAM)

The cell architecture of an STT-MRAM is illustrated in the figure 1.7 (a). The structure comprises two thin films of different ferromagnetic materials isolated by a layer of tunnel oxide and forms a magnetic tunnel junction. The applied bias across the device terminals governs the direction of magnetic polarization in both ferromagnetic layers and hence the magnitude of tunnelling current changes. The occurrence of parallel and antiparallel magnetization will vary the tunnel current as illustrated in figure 1.7 (b). The modulation of magnetoresistance (R_m) forms high and low resistance states due to parallel and antiparallel magnetization representing the binary states of memory. The STT-MRAM offers a high endurance of the order of 10^{16} and high-speed read and write operation (10 ns) but these devices have very small memory window [Endoh et al., 2016]. There are other scalability and complexity issues with multilayer device fabrication and CMOS integration without affecting the magnetic properties of the ferromagnetic layers.

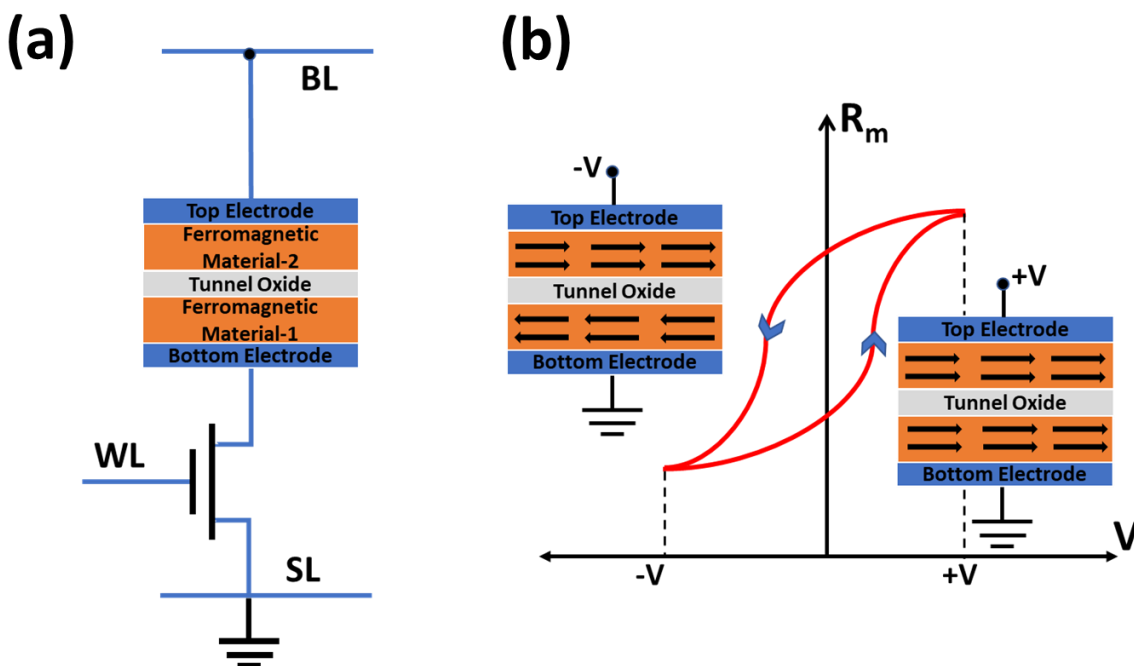


Figure 1.7: (a) Device architecture of an STT-MRAM cell. (b) Magnetoresistance curve for a typical STT-MRAM.

1.3.3 Phase Change Random Access Memory (PCRAM)

The PCRAMs store the information bits in the form of resistance change of the switching layer due to phase change [Sebastian et al., 2019]. The cell architecture of a PCRAM is shown in the figure 1.8 (a). The structure comprises a phase change material, a heating element embedded with two adjacent dielectric layers for insulation sandwiched between the bottom and top electrodes. $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST) is a chalcogenide alloy widely explored as a phase change material for PCRAM [Gyanathan et al., 2011]. These phase change materials are temperature sensitive and show the competence to change the resistance as the crystallinity of the material transforms from crystalline to amorphous or vice versa. Two distinct resistance states define the two memory states due to the phase change of the switching layer. The time of applied voltage to the heater changes the resistance state i.e. high resistance or low resistance state as illustrated in figure 1.8 (b). The writing operation takes place upon the heating temperature through the heater to the adjacent part of the switching layer to get crystallize and a low resistance state is obtained. While the execution of reset or erase operation requires a high current pulse to melt and quench the switching layer for a very short period to achieve the high resistance state [Lotnyk et al., 2019]. The higher switching voltage is the major issue associated with the PCRAM in comparison to other NVM technologies [Lacaze et al., 2014]. However, it has been explored by many global players in the memory industry as a commercial product because of its storage density, fast operation and high endurance.

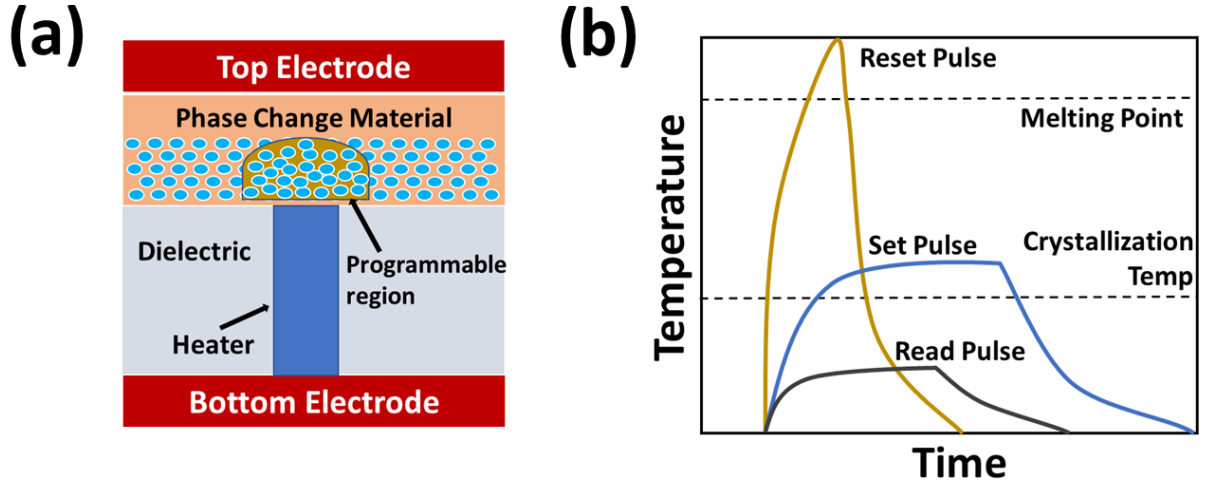


Figure 1.8: (a) Schematic representation of a PCRAM cell. (b) Representation of a typical PCRAM programming scheme for both set and reset state where phase transition from amorphous to crystalline and reverse is governed by pulse time.

1.3.4 Resistive Random Access Memory (RRAM)

Memory operation in a RRAM device is governed by the resistive changes in the switching or active layer due to its resistance switches from LRS to HRS or reverse upon the application of the applied electrical signal. Unlike STT-MRAM or PCRAM, no other mechanisms (magnetization or phase change) are responsible for switching the applied electric field is the direct cause of switching. The typical architecture of an RRAM cell comprises a switching or active layer placed between the electrode pair (top and bottom electrodes) as depicted in the figure 1.9 (a). The HRS corresponds to '0' and LRS corresponds to '1' for a cell [Zahoor et al., 2020]. The change in resistance state is due to the formation or dissolution of a conductive path or filament between the top and bottom electrodes upon the applied bias as shown in figure 1.9 (b). A variety of semiconductor and dielectric materials like metal oxides, perovskite oxides, transition metal dichalcogenides (TMDC), organic polymers and hybriide composites have been explored as switching layers [Wang et al., 2019]. For bottom electrodes, generally inert metal/conductive materials like Au, Pt, Ti and ITO are used while both the inert and electrochemically active materials are used as top electrodes depending upon the

requirement. The switching phenomenon in RRAM is hypothesized or explained by various mechanisms which are explained further in the subsequent part of this chapter. The electrochemical nature of the top electrode and its interaction with the active layer defines the switching mechanism of RRAM.

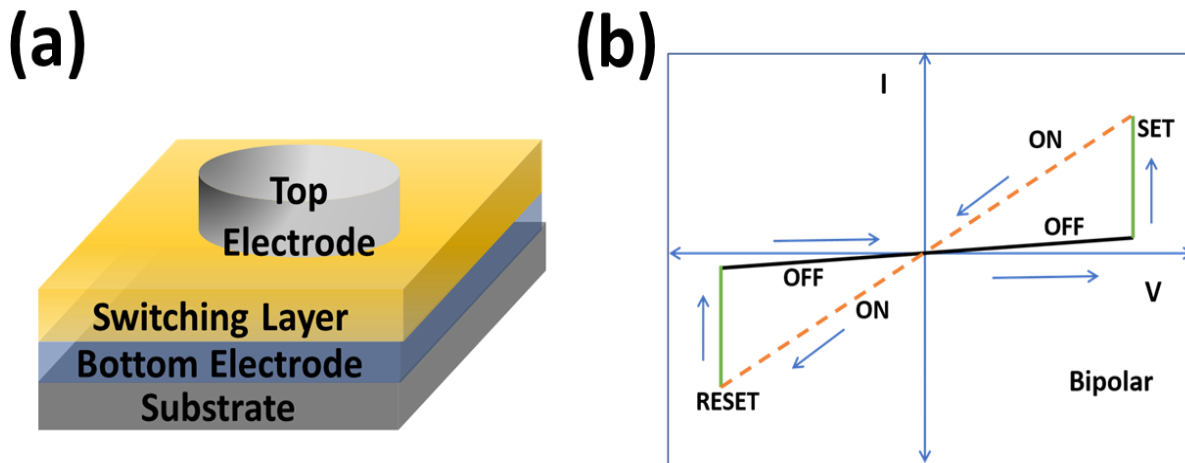


Figure 1.9: Schematics diagram of RRAM metal-insulator structure with single switching layer (a) and bi-layer switching layer. (b) Schematic diagram representing current-voltage characteristics of unipolar and bipolar resistive switching.

Further, the polarity of bias for the switching operation of RRAM divides the RRAM into two categories; bipolar and unipolar RRAM. The bipolar RRAMs are popular due to their reliable and stable performance. The erase process in RRAM is governed by the dissolution of conductive filament. RRAM offers the advantages like low switching voltage, high-speed operations, excellent endurance, high retention and low feature size over the other emerging NVM technologies [Chang et al., 2016] as shown in table 1.1. The comparison of different existing and emerging NVMs based on the different parameters is given in table 1.

Table 1.1 : A benchmark table for the performance comparison of various parameters of emerging and existing memory technologies [Wong et al., 2016].

Parameters	Flash	STTRAM	MRAM	PCRAM	FeRAM	RRAM
Feature Size (nm)	16	65	65	45	180	<5
Density (Gbit/cm ²)	52	20	1.2	12	0.14	154-309
Read Time	0.1ms	20ns	20ns	12ns	40ns	<1ns
Write/Erase time	0.1ms	20ns	20ns	100ns	65ns	<1ns
Retention Time	10yr	10yr	10yr	>10yr	10yr	>10yr
Endurance (cycles)	10 ⁵	10 ¹⁴	10 ¹⁴	10 ⁸	10 ¹²	10 ¹⁴
Write cycle	1x10 ⁵	>1x10 ¹²	1x10 ¹²	1x10 ⁹	1x10 ¹⁴	>1x10 ¹²
Write operation voltage (v)	8-10	2.5	3	3	1.3-3.3	<1

1.4 Resistive Switching Devices

As the name refers, resistive switching is a change in the resistance state of material sandwiched between two electrodes due to the formation and dissolution of a conductive path in presence of an applied electric field. A simple metal-insulator-metal configuration is used for the realization of a resistive switching device. The resistance change in these devices may be reversible or permanent. Based on the nature of resistive switching, resistive switching devices can be broadly classified into two categories; resistive random-access memory (RRAM) and write once read many (WORM). The switching in both cases is non-volatile in nature as it can retain the data even after the removal of the applied voltage across the cell. The resistive switching phenomenon has been explored for a variety of semiconducting and dielectric materials. Each type of material has its advantages and limitation to be used as an active layer in resistive switching devices. Inorganic materials like metal oxides, nitrides and chalcogenides offer a reliable, robust and stable memory performance over organic materials [Gao et al., 2016]. While the involvement of expensive fabrication techniques and high-temperature processing are the limitations associated with these materials being used for flexible and low-cost applications but organic materials can do so. Among all the available materials for the active layer, metal oxides are more popular and widely used in the development of resistive switching memories at the commercial level. Again, the selection of electrode materials also alters the switching performance and as discussed earlier a variety of metals/conductors have been explored for resistive switching applications.

The first resistive switching phenomenon was observed by Hickmott in the year 1962 when he explored it in an aluminium oxide (Al_2O_3) layer sandwiched between gold (Au) and aluminium (Al) electrodes [Hickmott, 1962]. He observed the negative differential resistance (NDR) properties in Al_2O_3 and explained the resistive switching mechanism for these devices. NDR is a kind of resistive switching behaviour where the device shows an exponential rise in current upto a certain level of voltage and then a sharp decrement in device current occurs [Pergament et al., 2014]. Afterwards, in the late 1960s and 1970s, a significant number of reports and reviews were published on the resistive switching behaviour of metal oxide thin film and its application as NVM. Further, the unavailability of experimental techniques to prove the physics behind the resistive switching behaviour phenomenon and the availability of matured silicon-based memory techniques slows down the research in this domain. During this period silicon-based memories and electronic devices gained huge attention due to their commercial viability over metal oxide-based resistive switching devices. The demand for oxide layers in metal oxide semiconductor (MOS)-based technology triggered the research to develop facilities to deposit a very high-quality thin film. At the same time, the major spectroscopy and microscopic techniques for thin film characterization to explain the physics behind different mechanisms were in the advanced stage. In the year 1965, Gordon Moore proposed Moore's law and predicts that the number of transistors will get double by every 18 months. As time moves the focus of the electronic industry shifted to developing compact, denser, energy-efficient and fast MOS devices. The aggressive efforts for scaling by the year 2000 resulted in a reduced feature size of about 100 nm. In early 2000 the physical limits of available MOS devices attracted the attention of the scientific community as it was not able to follow Moore's law in the near future and the research focus gets shifted towards the development of alternatives to present electronic memory techniques for large area applications.

At the same time in early 2000, the reports published by Bednorz et al. and Ignatiev et al. on metal oxide-based RRAM devices presented impressive results and received significant attention from the scientific community to be explored as an emerging NVM technology. Till this period from the 1960s, the development of advanced analytical techniques and the optimized growth process for high-quality oxide thin films further triggered the pace of the research in this domain. Now the available analytical tools were able to express the physics behind the resistive switching phenomenon such as the formation and dissolution of the conductive path in a memory cell. The industries and research centres focused their studies to

develop a combination of an active layer and a pair of electrodes to achieve stable, fast and cost-effective NVM devices with CMOS compatibility [Kargar et al., 2022]. Currently, the major semiconductor foundries have commercialized resistive switching-based memories and further research is going on. Referring to a report the resistive switching-based memory market is growing with a CAGR of ~16% and it will hit a millstone of \$ 655 million by the year 2025.

1.4.1 Write Once Read Many (WORM) Resistive switching

WORM is commercially used as a data storage element in RF id tags. These devices show excellent capabilities to store large data for a long period and to prevent data alteration. The WORM devices are widely used for applications where the permanent archival of big data like images, videos and other non-editable information is required. For the commercial application of these devices, they should possess low switching and read voltage with fast-switching speed and long data retention. Based on the switching state after the writing process, the WORM devices are broadly classified into two categories; type-I WORM or fuse memory and type-II WORM or anti-fuse memory [Qi et al., 2011b].

The typical structure and switching curve of type-I WORM are shown in figure 1.10 (a). In type-I WORMs, the pristine (original) state of the device is LRS and after the application of a voltage signal for the writing process the irreversible switching from LRS to HRS takes place [Zhu et al., 2018]. Type-I WORM consists of a conducting filament (fuse) of low melting current between two electrodes and the current flow through the fuse is blown up the fuse after a certain value of the bias turns the memory cell in HRS as shown in figure 1.10 (b). A variety of materials including metals, semiconductors, organic polymers and hybrid composites have been explored for the realization of type-I WORM devices.

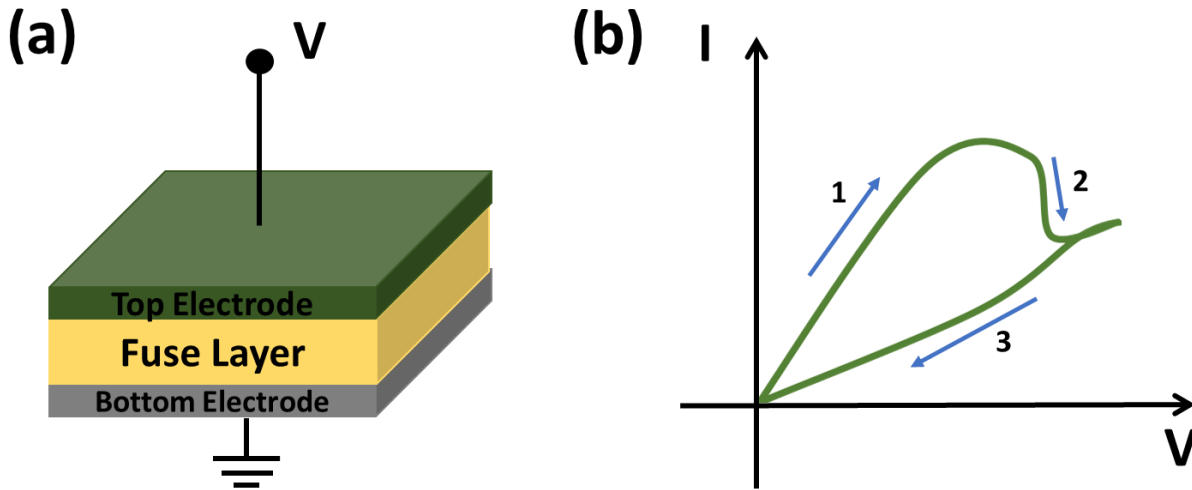


Figure 1.10: (a) Schematic diagram representing of type-I WORM. (b) Schematic diagram of the switching curve of type-I WORM.

The switching transition in type-II or anti-fuse is just the opposite of the type-I WORM [Leppäniemi et al., 2014a]. After the execution writing process, there is a permanent transition from HRS to LRS as shown in figure 1.11 (b). A typical structure of type-II WORM consists of a semiconducting or a dielectric switching layer placed between two metal electrodes as illustrated in figure 1.11 (a). A variety of inorganic and organic materials have been explored for type-II WORM including binary, ternary metal oxides, composited and organic polymers. Among all materials, the metal oxide layers show excellent WORM performance. Upon the applied potential the current through the device abruptly switches to higher values by forming an irreversible conductive path. Type-II WORM offers the advantages of low voltage operations

and fast speed over type-I WORM. The extensive acceptance of the metal oxide active layer makes it a cost-effective and scalable candidate for permanent data storage.

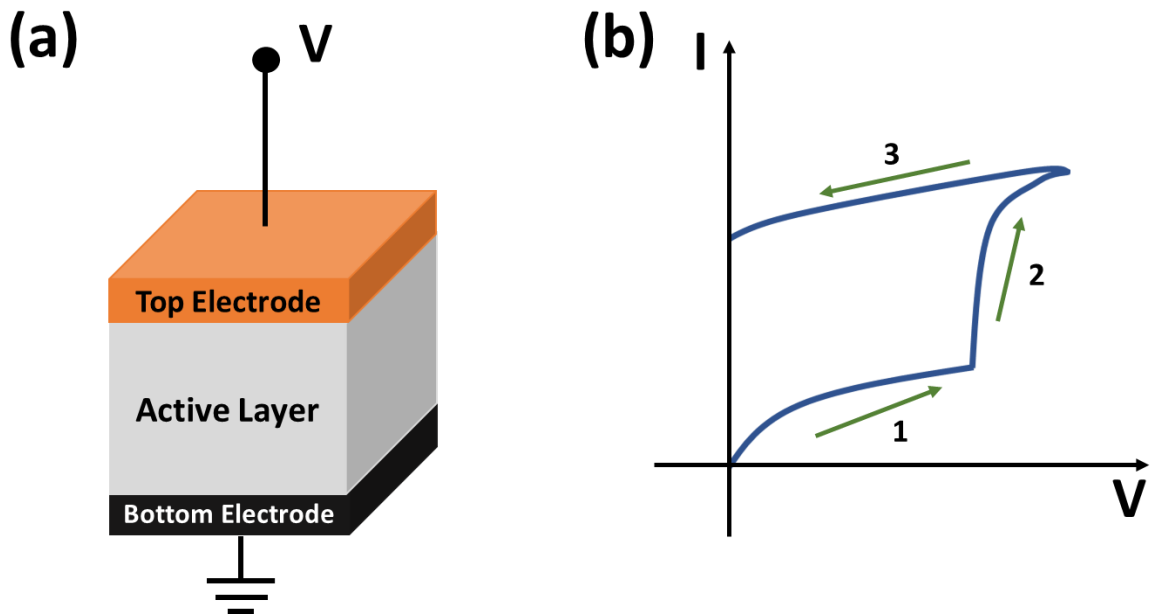


Figure 1.11: (a) Schematic diagram representing type-II WORM. (b) A Schematic diagram of the switching curve of type-II WORM.

1.4.2 Resistive Random-Access Memory (RRAM)

As explained in section 1.3.4 RRAM is an emerging NVM based on the principle of change in resistive state. The structure of the RRAM cell is given in figure 1.12. The transition of the resistance state takes place during the write ('1') and erase ('0') process from HRS to LRS and LRS to HRS respectively. The stored bit can retain itself for a prolonged period and can be read by applying a very low voltage. Figure 1.12 represents a schematic demonstration of various switching processes involved in the memory operation of RRAM. The fabricated device shows high resistance behaviour in starting while upon applying a sufficient voltage the switching process gets triggered either it is abrupt or soft. At this voltage level, the filament formation takes place and the device switches to set state or LRS or the write process takes place. After the writing process, the device can hold the LRS for a long time even after the removal of applied voltage. A soft forming or forming free RRAM has the advantage of low voltage operation. Generally, the RRAM is used with current compliance imposed by a transistor to avoid the risk of permanent damage in the active layer if the forming is abrupt. Further, the current compliance can regulate the filament dimensions and hence better device performance is achieved. To execute the erase process after the writing the dissolution of the conduction filament is required to bring back the device to HRS or reset. A sufficient voltage bias is applied across the electrodes and the filament rupture takes place. RRAM devices need a very low voltage to read the stored data as it offers a very good switching ratio or window. Sometimes the incomplete dissolution of conductive filament leads to the leakage current and variation in the switching window after each successive cycle. The issue of reliability can be overcome by the optimization of the active layer. The writing process is termed set and erase process is termed as reset for RRAM devices. The requirement of SET and RESET voltage depends on various factors including film thickness, quality of the thin film, electrode material and testing environment.

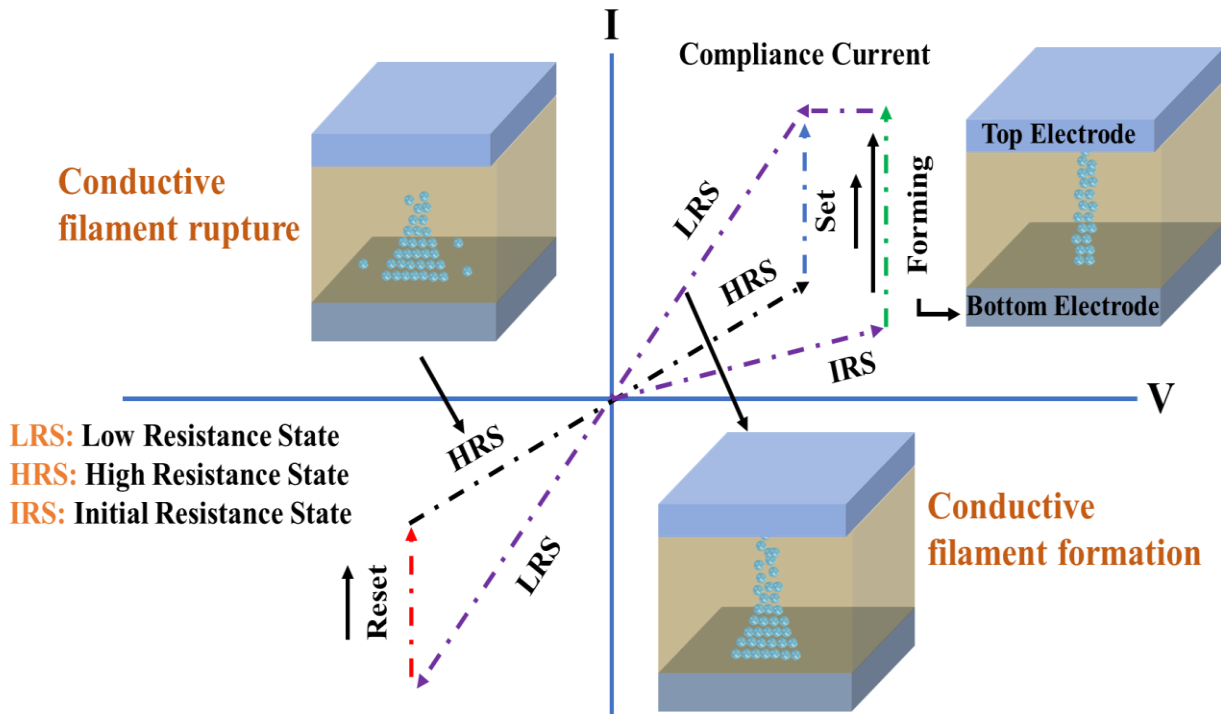


Figure 1.12: Schematic demonstrating the resistive switching mechanism with the demonstration of forming, set, and reset processes in a typical bipolar RRAM cell.

1.5 Classification of RRAM

The RRAM is further divided into different categories depending on the polarity of applied voltage at which switching takes place and the filament formation mechanism. The resistive switching mechanism broadly classified the RRAM devices into two categories including conductive bridge RRAM (CBRAM) and valence change RRAM (VCRAM).

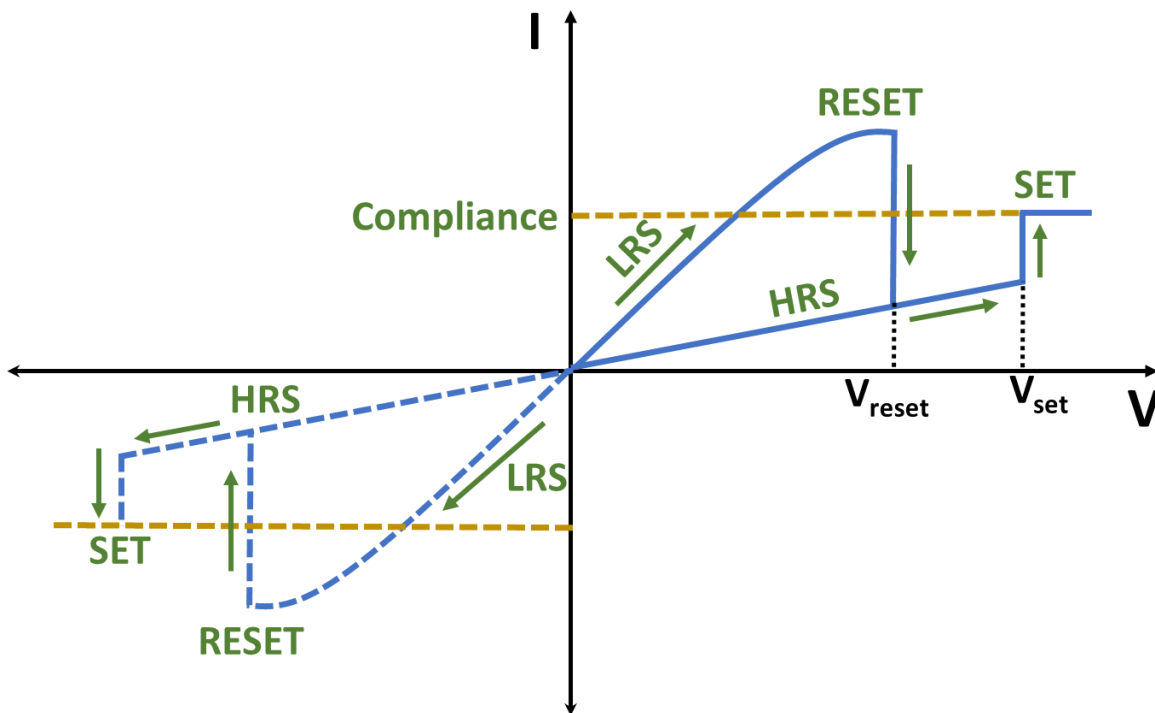


Figure 1.13: Schematic demonstration of unipolar resistive switching using device I-V characteristic.

1.5.1 Based on the Polarity of Switching Operations

The switching voltage polarity-based classification involves unipolar and bipolar resistive switching. A detailed description of the polarity-based classification of RRAM devices is provided in the following subsections.

1.5.1.1 Unipolar Resistive Switching

A resistive switching device is termed unipolar if the write and erase process is executed for the same polarity of applied voltage. The device switches from LRS to HRS and HRS to LRS or set and reset states take place at the same polarity either positive or negative. The device switching at positive polarity is called positive unipolar switching and if it is at negative bias polarity then is called negative unipolar switching. The graphical representation of positive as well as negative unipolar resistive switching characteristics is shown in figure 1.13. As shown in the figure the set current is controlled by using current compliance to avoid permanent destruction to the device while the reset process is kept compliance free because of the high reset current.

Metal oxide semiconductors and dielectrics including ZnO, TiO_x, NbO_x, TaO_x, HfO_x and AlO_x have been widely reported for unipolar resistive switching. Besides these metal oxides other material systems like TMDCs, organic polymers, organic semiconductors and composites also have been investigated for the realization of unipolar resistive switching devices. Many reports are available showing the both type of switching behavior (unipolar and bipolar) for different voltage levels and current compliance for a same device. The pair of top and bottom electrodes is the controlling factor for a unipolar device where both contacts are of the same material or have the least tendency of oxidation and reduction (i.e. inert metals). The write process is governed by the ionic motion due to Soret force and further, a joule heating assists the dissolution of filament during erase process.

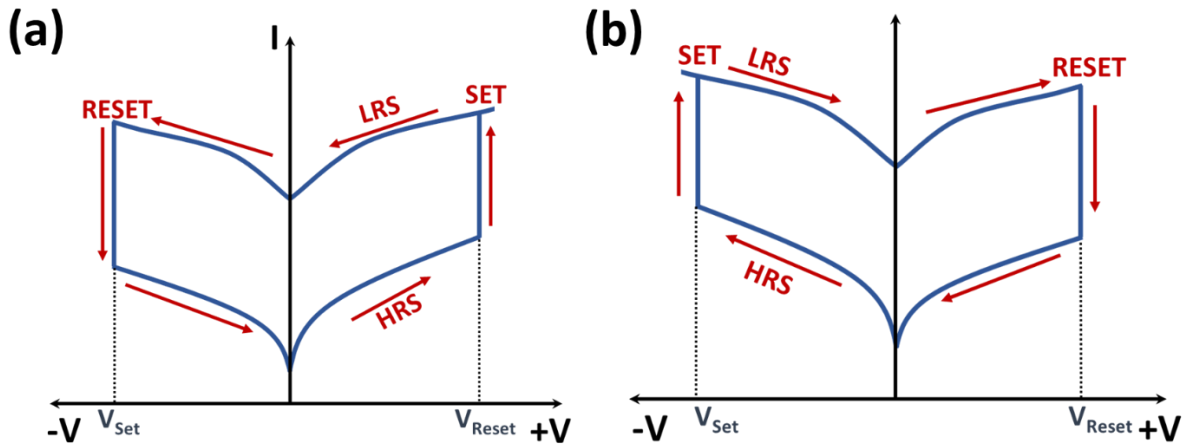


Figure 1.14: Typical I-V characteristics of bipolar resistive switching characteristics in F8 (a), and cF8 modes (b).

1.5.1.2 Bipolar Resistive Switching

As the name suggests, for a bipolar resistive switching device write and erase process is executed for the opposite polarity of the applied bias. Hence if the write process occurred for the positive polarity, then the erase process will take place for the negative polarity of the applied bias and vice versa is also possible. The write state for positive polarity refers to the figure-of-eight (F8) scheme and for negative polarity write state it refers to the counter-figure-of-eight (cF8). The graphical representation of current vs voltage characteristics for both F8 and cF8 bipolar switching schemes is shown in figure 1.14. The resistive switching in bipolar switching devices is governed by two major switching mechanisms (VCRAM and CBRAM) discussed in the next sections. The compliance current control offers a low risk of permanent damage to the filamentary path due to the joule heating effect at a high current.

Different combinations of electrode pair and active layer have been studied for the realization of bipolar RRAM. The electrochemical properties of the top electrode are a deciding factor for the type of resistive switching mechanism. Further, the defect density of the active layer also governs the switching in a device. A wide variety of different materials including metal oxides, semiconductors, dielectrics, organic polymers, TMDCs and composites have been studied and showed excellent potential to be used for RRAM. Among the all-promising materials, metal oxide dielectrics have gained huge attention for years because of their outstanding retention, endurance and wide memory window. HfO_x , AlO_x , TiO_x , BaTiO_3 , and graphene oxide-based RRAM devices show the F8-type bipolar resistive switching behaviour and WO_x and LaFeO_3 show the cF8-type switching behaviour. Few binary and ternary oxides including WO_x , Nb-STO and PCMO showed both kinds of switching behaviour. The F8 type switching is highly preferred over the cF8 type switching behaviour because of their high switching ratio and stable operation.

1.5.2 Based on the Switching Mechanisms

RRAM devices can be further classified based on the switching or conduction phenomenon. The conduction phenomenon for the RRAMs was not cleared for years but the development of advanced microscopy and spectroscopy techniques in recent years helped to understand the physics behind the switching behaviour. The switching mechanisms are majorly explained by either valance change RRAM (VCRAM) or conductive bridge RRAM (CBRAM). There are many different terms are coined to explain the switching as Oxide RRAM (OxRAM), electrochemical metallization (ECM) etc.

1.5.2.1 Valance Change Resistive Random Access Memory (VCRAM)

The movement of vacancy ions in the active layer governs the switching in VCRAM. The primary reports were produced on metal oxide-based VCRAM. The applied potential across the device initiates the redox reaction in the metal oxide active layer and the movement of ions forms the conductive path. Ti, Ta and Al have been widely employed for the realization of VCRAM due to their oxidizing nature. For the bottom electrode Pt, Ir, and other metals offering high work function are used to form a Schottky junction between the metal contact and switching layer interface. The pair of electrodes of the same metals are also reported for VCRAM. Upon the applied voltage sweep the generation of negatively charged oxygen (O^{2-}) and positive oxygen vacancies takes place and hence the change in valance state of contact metal cation changes (M^{n+}). The variation in the valance state of metal cation significantly alters the conductance of the active layer. The equations given below can explain the generation and movement of vacancy ions:



Where O_o denotes the oxygen ion and V_o represents the oxygen vacancy. The negatively charged oxygen ions will move towards the anode and the ion migration will be governed by the potential gradient, ion concentration gradient and thermal gradient. At the same time, the positively charged vacancy ions will migrate towards the cathode and hence the vacancy ions inside the bulk will form a conductive path or filament through the switching layer. The illustrative representation of all the events (forming, set and reset) involved in the VCRAM-based unipolar and bipolar switching is shown in figure 1.15. Further except for the process explained above the interface-VCRAM kind mechanism also explains the switching mechanism where the interface of the insulator and metal regulates the switching. The Schottky barrier formed at the interface will cause a band banding of energy bands to match the fermi levels. In

such a scheme, the migrated ions due to the field will alter the Schottky barrier and hence the resistance of the memory cell will get regulated. Interface-VCRAM-based RRAM devices generally offer the gradual set and reset process that makes them a suitable choice for neuromorphic applications but the low switching window is a limiting factor.

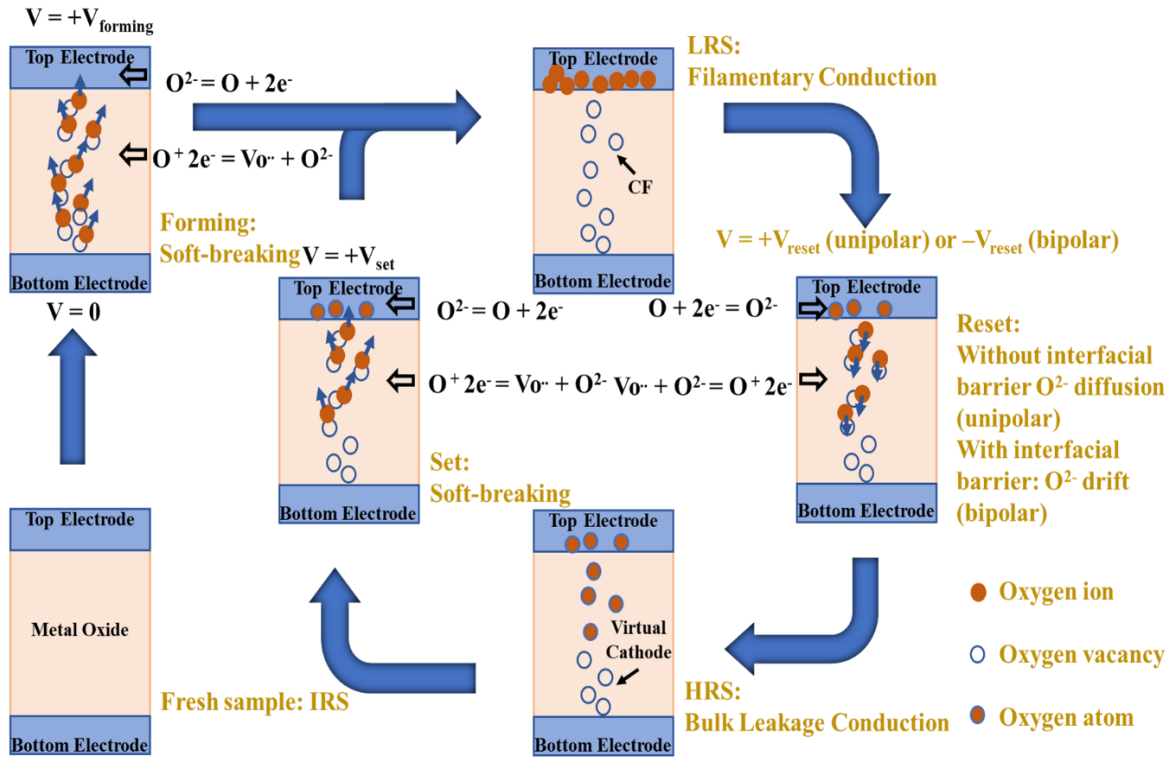


Figure 1.15: Schematic demonstration of resistive switching mechanism in a VCRAM.

1.5.2.2 Conductive Bridge Resistive Random Access Memory (CBRAM)

The resistive switching behaviour due to conductive path formation between the bottom and top electrodes governed by the migration of metal ions of the electrochemically active top electrode for a resistive switching device is explained with the CBRAM conduction mechanism. Upon the applied voltage the electrochemically active electrode the metal starts migrating towards the inert bottom electrode through the dielectric layer. Figure 1.16 illustrates a graphical representation of the switching phenomenon governed by the CBRAM switching mechanism where the top electrode is Ag. It involves different processes including initiation of forming, set process or filament formation and reset process or the filament destruction. The complete switching process is divided into four parts with respect to their respective voltage and the numbers are assigned for better understanding. When voltage signal is applied to the fresh memory cell (point 1) the Ag ion starts migrating towards the bottom electrode (point 2) and as the voltage attains the switching value the formation of a complete filament takes place (point 3) and the device switches to LRS. Further, as the applied voltage of reverse polarity starts the dissolution of filament (point 4) and the memory cell switches to HRS again. There are a lot of reports have been produced the experimental evidence for the formation and dissolution of metal ion filament between the electrodes. The cross-sectional TEM images have been widely used to visualize the metal filament in CBRAM devices. Ag, Cu and Ni are the commonly used active metals to form top contacts in CBRAM devices. The switching in CBRAM is governed by the top electrode migration and defect sites of active layer. Generally, the switching observed in CBRAM devices is bipolar in nature. The CBRAM devices offer a very high switching ratio (on/off) with stable and high speed switching.

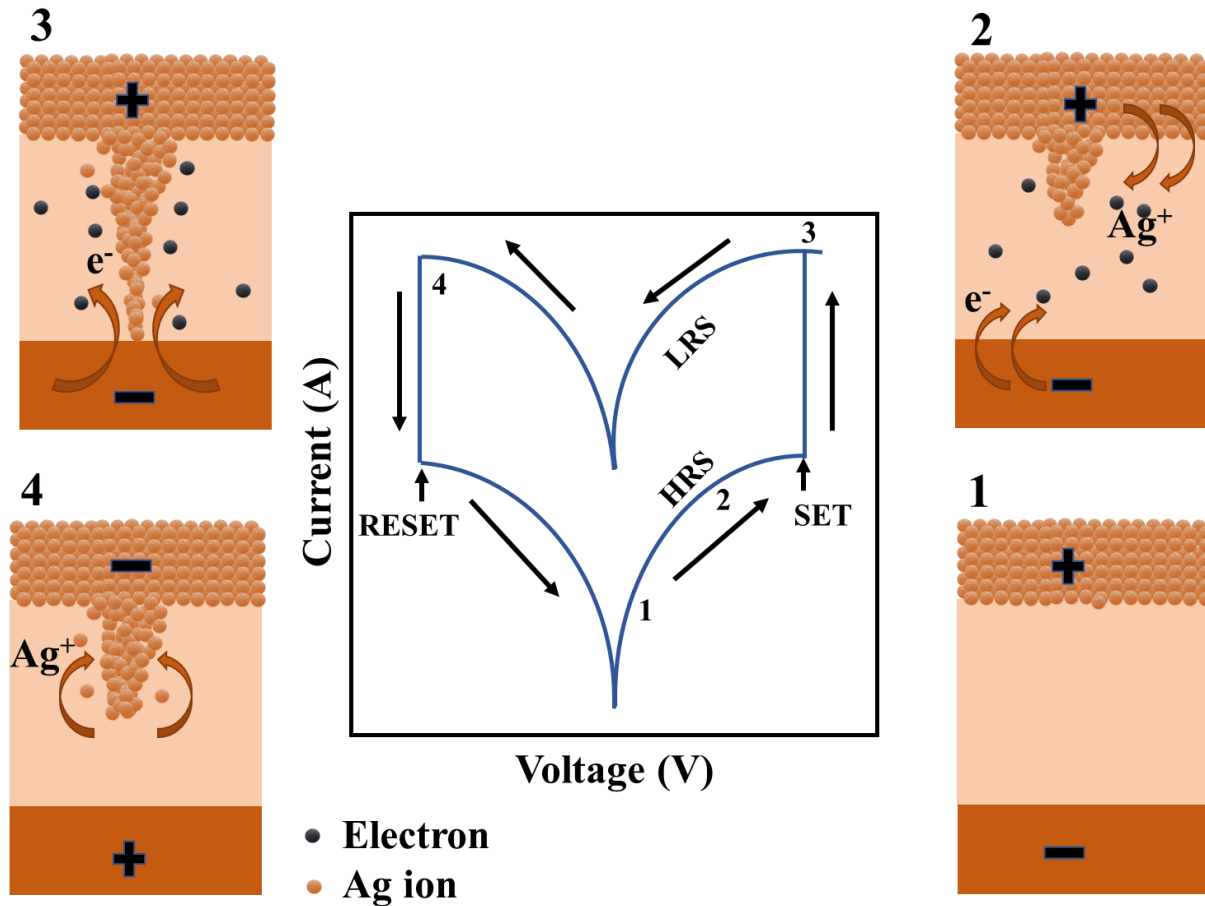


Figure 1.16: Demonstration of switching mechanism in a CBRAM device using typical current-voltage characteristics and related movement of ions and atoms during each transition (1-4) between the HRS and LRS.

1.6 Resistive Switching Device Structure

A typical resistive switching memory cell as discussed in previous section consists of a MIM structure where an active/switching layer is placed between the top and bottom electrodes. The dimension of the active area of a memory cell plays a notable role in the memory performance of a memory cell. To control the cell area of a device generally the dimensions of the top electrode are controlled. Generally, research institutes and universities don't have a state-of-the-art facility for the fabrication of wafer-scale memory chips and hence they used the simplified and small MIM configuration for the realization of memory cells. There are different device configurations have been proposed to form a resistive switching memory cell including the lateral and MIM structure. The commonly used device configurations to explore the resistive switching properties of a device are:

- Common bottom electrode
- Cross-point structure
- Cross-bar structure

Each device configuration has its advantages, disadvantages and fabrication complexities. The commonly used device architectures for resistive switching devices are depicted in figure 1.17 (a). The common bottom electrode structure is widely reported for laboratory-based resistive switching devices because it involves simple fabrication steps. An active layer is deposited on the bottom electrode and a small region is kept open to take electrical connections for characterization. Then the top contact of desired size and shape is deposited over the active layer with the help of a shadow mask or lithography depending on

the feature size of the top electrode. This configuration faced the issue of making electrical connections using a probe tip if scaled below $100\ \mu\text{m}^2$. However, many sophisticated characterization techniques like conductive AFM (CAFM) offer the solution to this issue and it can be further scaled down but it doesn't seem feasible for institute-level research.

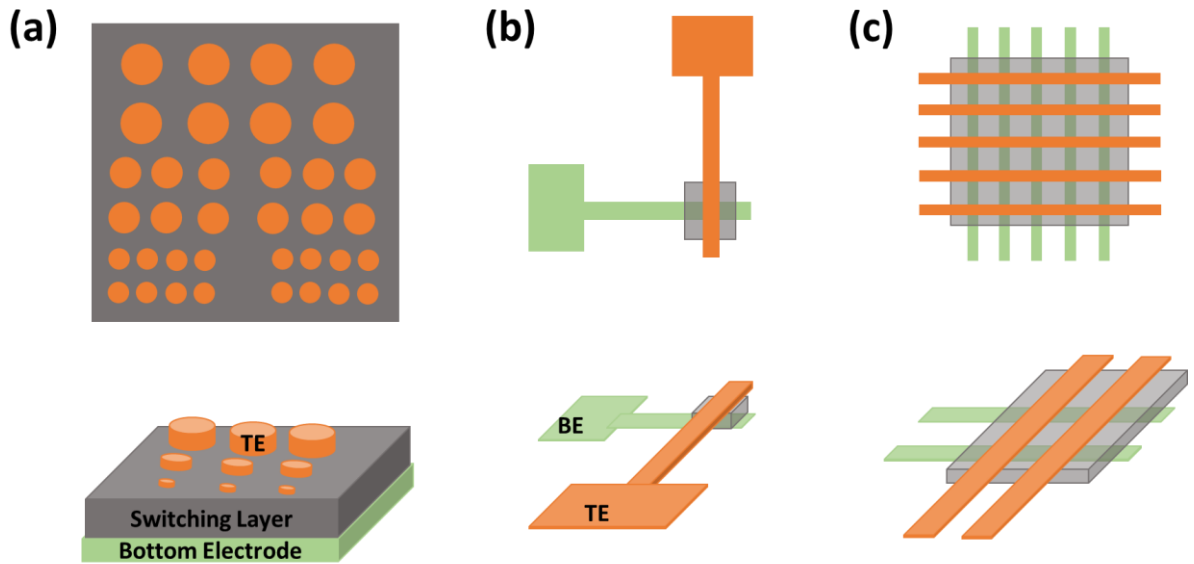


Figure 1.17: Schematic representation of the commonly used RRAM device architectures. (a) The BE is common to every cell and the switching layer and TEs were patterned. (b) The cross-point structure provides isolation between each device with separate bottom and TEs. (c) Cross-bar structure forms multiple cross-point cells interconnected to each other, providing higher density and the advantage of 3D architecture fabrication.

To overcome the issue of electrode probing due to low contact size in common bottom electrode structures the cross-point configuration was introduced. A pair of electrodes of low dimension and extended large contact pads for electrical connections are used in this configuration. The active layer is placed between the electrode pair as depicted in figure 1.17 (b) and the overlapping area between the electrode defines the cell area for the device. The fabrication process involves two-stage lithography which is quite complex in comparison to the common bottom electrode configuration. The contact dimension can be scaled down from $1\ \text{m}^2$ to $100\ \text{nm}^2$ depending on the type of lithography process involved in fabrication [Govoreanu et al., 2011]. It offers excellent scalability, stability and reliability but there is an issue of sneak path leakage current analysis.

To address the issue of sneak path leakage current a more complex cross-bar device configuration is used. It offers a higher cell density while fabricating a chip. The active layer is sandwiched between the array of parallel contacts of lower dimensions as shown in figure 1.17 (c). It is a combination of multiple cross-point structures connected in an array. These small bottom and top electrodes are connected to larger pads with the help of thin wires. The fabrication of a cross-bar structure is complex as it involves two stage lithography process and wire bonding to make electrical connections. The characterization setup for these devices requires to die packaging and PCB with a switching matrix tool [Prezioso et al., 2015]. The excellent scaling is offered by the cross-bar structure. As the size is reduced the electrical probing is unable to measure the performance. In such a scenario the CAFM is used for characterization.

1.7 Performance Parameters for Resistive Switching Devices

The various parameters extracted during the electrical characterization of a resistive switching device help to understand the device's performance. Electrical characterization is the

last process for performance analysis but the complete fabrication process plays the important role in device performance. To develop a high-performing device all constituent layers should be optimized in terms of thickness, structure and morphology. With this controlling parameter the fabrication environment, equipment used and sample handling are also important for device performance. The performance of a resistive switching device is defined by analysis of the following parameters given below:

- Retention characteristics (read and write resistance vs time)
- Endurance characteristics (resistance vs no. of Cycle)
- Switching speed
- Power consumption
- Variability
- Scalability

a) Retention Characteristics

Retention time is the most important performance parameter to decide the performance and application of a memory device for the NVM application. It is defined as the time for the retention of stored data under zero bias conditions. To examine the retention time of a resistive switching device, a low bias voltage is subjected to read the current for both set and reset states and the explored data is plotted in the form of a current versus time (I-t) curve. The figure 1.18 represents a typical retention curve for an RRAM device for both states at the same bias voltage. The retention for a device depends on various factors like compliance current and the switching mechanism. The higher compliance will cause a high retention time for the device. Generally, there is a slight reduction in the set state current is observed while the reset state current doesn't fluctuate much. Typically for an NVM device, the retention should be more than 10 years at an elevated temperature. RRAM offers a long retention time of more than a decade.

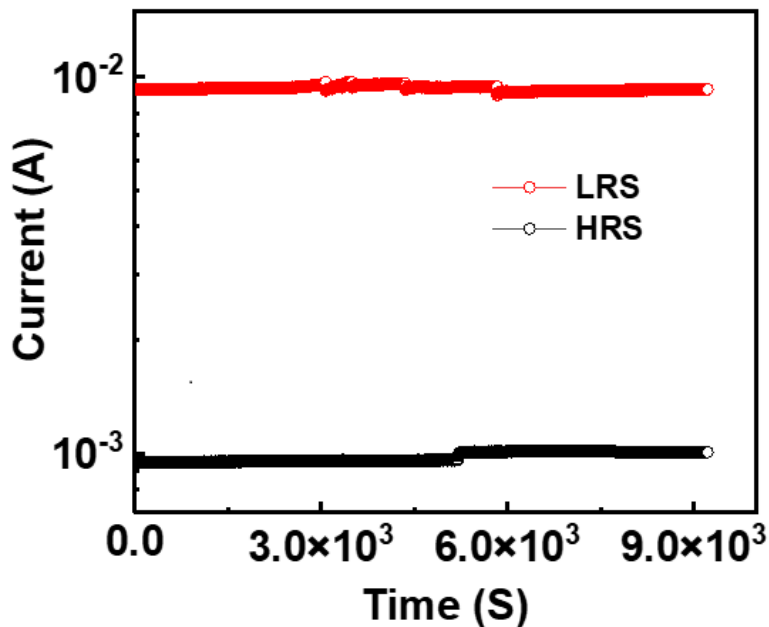


Figure 1.18: The retention time measurement of LaFeO₃ RRAM.

b) Endurance Characteristics

Endurance for a resistive switching device is explained as the number repetitive of cycles of execution of switching action while maintaining the sufficient switching ratio for each cycle. It is highly desired that a device should show high endurance and the resistance ratio should not fluctuate with the cycles. The reduction in switching ratio beyond a certain level may lead the device failure. However, failure is a common phenomenon over the multiple cycle

execution but it should not occur suddenly. To analyse the endurance performance of a resistive switching device there are two methods are widely employed:

- Voltage sweep method
- Pulsed stress method

For the I-V sweep method, a voltage sweep for the defined number of cycles is applied across the device under test. The resistance value for each cycle is taken for both set and reset state at a voltage where we are getting the maximum on/off ratio and plotted against the number of execution cycles. Figure 1.19 demonstrates a typical endurance curve for a device using the voltage sweep method. This method is quite slow in comparison with the pulsed stress method as it takes more time to collect the data points and if the current lies in the nano ampere or lower range then it is much slower.

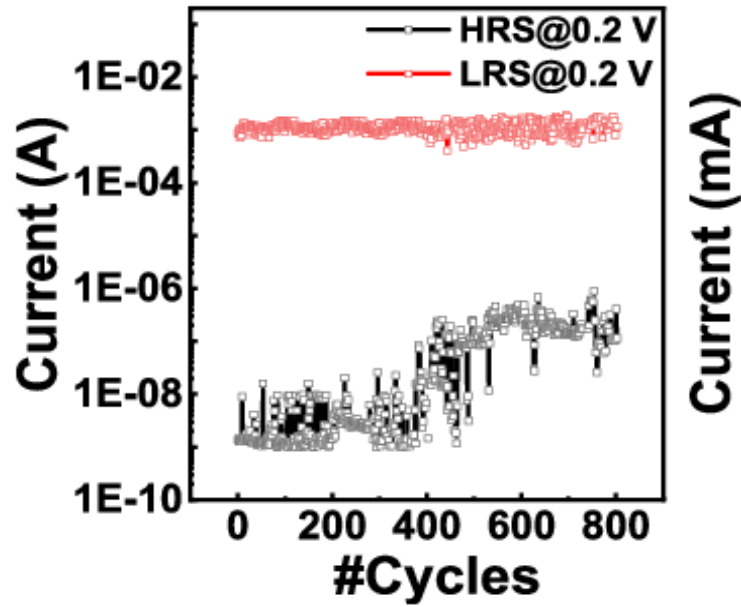


Figure 1.19: Endurance characteristics for a metal oxide based RRAM.

The pulsed stress method involves a set of pulses to execute the write-read-erase-read operation for a resistive switching device and the current concerning each state is recorded. The pulse amplitude and time can be varied as per the requirement of the study. The read current for each state is plotted against the number of cycles to get the endurance curve for the device. The pulse stress measurement requires an additional pulse source with a normal source meter and hence the system costs more. The RRAM devices have been reported for endurance of more than 10^9 cycles.

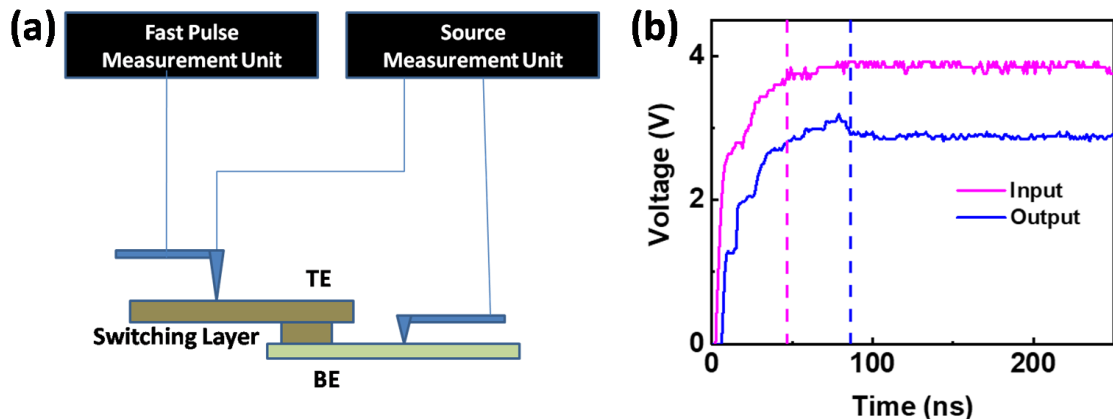


Figure 1.20: (a) Schematic diagram of setup for high-speed switching measurements. (b) Switching speed of a LaFeO_3 based RRAM device using a voltage pulse.

c) Switching Speed

The fast execution of memory operation is the primary requirement for a memory device hence the switching speed is a deciding factor when we talk about performance. The switching speed for a resistive switching device is defined by the time taken to transit from one resistive state to another. The switching time is measured using a pulse source integrated with a source meter as shown in figure 1.20 (a). The material used for the switching layer and film quality plays an important role in the modulation of switching speed. For RRAM devices the ideal switching speed is of the order of a few nanoseconds which is quite higher in comparison to current NVM technology. Figure 1.20 (b) shows a graphical representation of transient characteristics for switching time measurement.

d) Power Consumption

As far as the memory devices are concerned power consumption is an important factor to take care of for an efficient and compact system. The power consumption in a resistive switching device is generally governed by the current of the set state and can be altered using a current compliance. Power consumption for a CBRAM device is comparatively low than VCRAM. The power consumption can be measured using I-V characteristics under varying loads.

e) Variability

The reliability of chip-level devices is generally explained using the variability characteristics where a more number of the same devices are fabricated on a single chip. The variability is defined by the cycle-to-cycle and device-to-device variation in the electrical performance and operating parameters. The higher variability leads the false operation or a wide range of operating forces which limits their use for memory applications. The fabrication environment control including uniform layer and smooth interface will reduce the cell-to-cell variations significantly. The cycle-to-cycle variation is still an unresolved issue for RRAM as the filament formation after each cycle is not at the same place. Hence the variability study for a resistive switching device provides information on device reliability.

f) Scalability

Scaling is an important measure to be taken care of to fulfil the futuristic demand of the growing electronic device industry. RRAM is still in the development phase and they are considered to address the scaling limit issues with the current memory technology hence the lower dimensions for RRAM devices are being explored. The feature size significantly modulates the switching performance as it alters the conduction phenomenon. Generally, for the sake of fabrication and characterization convenience the RRAM devices are fabricated with the $100\mu\text{m} \times 100\mu\text{m}$ area. The RRAM offer scaling upto nm^2 but the involvement of electron beam lithography (EBL) or extreme ultra-violet (EUV) lithography further increases the fabrication complexities. Further, the lower feature size faces the issue of characterizations as it requires advanced characterization to examine the memory performance.

1.8 Thesis Outline

Since the realization of a 64-bit RRAM array processed by 500 nm CMOS technology using a perovskite oxide active layer in the year 2002, these materials have gained sufficient interest as a switching layer for memory applications. Perovskite oxides offer a stable crystal structure with structural flexibility and defect tolerance for the migration of nonstoichiometric ions. The migration of nonstoichiometric ions contributes to resistive switching as a result of thermochemical reactions and ionic migration. Moreover, these materials show multifunctionality governed by electrons such as electroresistance, magnetoresistance, ferroelectricity, Multiferroic and superconductivity. The metal-insulator transition in perovskite oxides allows a significant transition in resistance. The stable crystal structure of these materials makes them radiation hard and they can withstand harsh conditions by maintaining a stable performance.

In this work, we focused on the realization of resistive switching devices using perovskite oxides as the active or switching layer. The effect of deposition parameters was observed to optimize the deposition parameters to obtain the best performance. Various perovskite oxides including BaTiO₃, SrTiO₃ and LaFeO₃ were synthesized to prepare the sputtering targets. To achieve the best results, we optimized the thickness and deposition temperature of these layers using Rf-sputtering. Further, the devices were studied for their memory performance with respect to the deposition parameters. The best-performing layers were further studied for their radiation stability test using low and a very high-energy irradiation facility. The effect of ion irradiation on surface morphologies and memory performance has been explored. Hence with these perovskite oxides as a switching layer, the aim was to study the following effects:

- Optimized thickness and deposition temperature of switching layers.
- The radiation stability upon exposure to ionic radiation.
- Neuromorphic studies for LaFeO₃ switching layers.

This thesis work includes the resistive switching studies for RF-sputtered perovskite oxide switching layers. The outline of the presented thesis is described as:

Chapter 1: This chapter describes the current and emerging memory technology in detail. The challenges associated with current memory technology and the need of resistive switching devices are described in detail. Further, the type of switching in resistive switching devices and performance parameters are discussed.

Chapter 2: This chapter describes the different experimental and analytical tools used for material synthesis, device fabrication and characterization. A brief introduction of the irradiation facility is also described.

Chapter 3: In this chapter, detailed studies on the resistive switching performance of BaTiO₃ WORM memory cells are provided. In this regard, the effect of thickness and temperature was studied.

Chapter 4: The radiation stability of the am-BTO WORM memory cells were studied and discussed in this chapter. The low-energy Ar ion irradiated thin films were studied for morphological and switching characterizations.

Chapter 5: This chapter describes the realization and stability analysis of SrTiO₃ thin film-based RRAM devices under swift heavy ion irradiation. In this regard, the SrTiO₃ thin films were irradiated with Au ions of 180 MeV energy and the RRAM performance was studied.

Chapter 6: In this chapter, detailed studies on the memory performance of LaFeO₃ RRAM devices are provided. Further, the synaptic behaviour of these devices was analyzed for their application in neuromorphic computing. In this regard, the effect of thickness was studied to achieve stability and a good memory window.

Chapter 7: This chapter describes the radiation stability of the LaFeO₃ RRAM devices. The low-energy Ar ion irradiated thin films were studied for morphological and switching characterizations. Further, the effect of irradiation on synaptic behaviour is explained.

Chapter 8: This chapter concludes the findings of this research work and also described the future scope.

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