

Introduction

The advancement of human civilization has been strongly intertwined with the development of information storage. It has helped us in recording, learning, and spreading of knowledge throughout the globe. The earliest means of information transfer can be attributed to story telling or oral transfer of knowledge, relying solely on narrator's memory. Subsequently, cave painting/carving can be regarded as an important milestone in information storage, and it has been found across the globe in different civilizations and cultures. With the advancement of civilization, methods of storage and transfer of information has also evolved. The invention of writing systems in ancient civilizations of Egypt, China, and India on materials like stone or clay tablet, leaves, and leather has contributed significantly in easy storage and transfer of information. Thereafter, around 15th century, the mass production of documents and books enabled by the creation of printing press has revolutionized the storage and spread of information. A pivotal milestone in information storage is the innovation of computer and digital storage media in the 20th century. The emergence of internet lifted the boundaries on information sharing, making vast amount of data accessible to everyone irrespective of their location. Today with the advent of cloud storage and artificial intelligence, the modern human civilization continues to advance at a rapid pace with vast amount of information at their fingertip.

1.1 Memory Devices and their Advancements

Memory Device is often referred to a modern electronic component or hardware that can store data and instructions. Earlier the memory component was mostly mechanical, such as punch cards and magnetic drums. These devices were bulky and limited in storage capacity and speed, but laid the foundation for further development and improvement of memory devices. The earliest solid state memory came into reality in 1955 with *An Wang's* patent for *Pulse Transfer Controlling Device* which made magnetic core memory a practical reality, marking the transition from mechanical memory to solid state memory [An, 1955]. Later with the advent of transistors, Read-Only Memory (ROM) and Random Access Memory (RAM) has emerged, and research for transistor based memory boosted. Dynamic RAM (DRAM) invented by *Robert Dennard* at the IBM T.J. Watson Research Center, stored information in the form of an electrical charge within a circuit, however it required timely refresh to maintain the stored data [Dennard, 1968]. The significant advancement in development of memory device was observed after the invention of flash memory by *Fujio Masuoka* in 1984, that was able to store data even in absence of supply power [Masuoka *et al.*, 1984]. Further to enhance memory density 3-D stack structures were developed by utilizing flash memories. The relentless drive for the development of advanced memory devices for high memory density, low power, and fast speed has met by some extent by scaling of

the devices. However, scaling has its own challenges that limit the reliable operation of these devices, and thus a search for new type of devices has gained momentum [Hong, 2010]. A simple metal-insulator-metal (MIM) structure device that can hold data without power supply emerged as the most suitable candidate, and its development boosted after publication of the article titled *The Missing Memristor Found* by D B Strukov *et al.* in 2008 [Strukov *et al.*, 2008].

1.2 Classification of Memory Devices

The electronic memory devices can be broadly categorized in two sections, volatile and non-volatile devices. One which can not store data without supply power and requires timely refresh are termed as volatile memory devices. Moreover, the devices which can store data even in absence of power are termed as non-volatile memory (NVM) devices.

1.2.1 Volatile Memory Devices

These devices make up the primary memory of any computer system as they can perform fast read and write operations. Static RAM (SRAM) and DRAM are two types of RAMs that are used in computer for in-processor and primary memory application.

Dynamic Random Access Memory

The earliest proposed DRAM cell had two elements, a transistor and a capacitor, thus known as 1T-1C DRAM cell [Dennard, 1968]. Fig. 1.2.1 (a) and (b) shows the schematic of 1T-1C DRAM cell. The charge stored in the capacitor is treated as a memory level, here when the capacitor is charged it has a bit '1' stored in it, while a discharged capacitor represents bit '0'. Wordline is used to activate the transistor so that the capacitor gets connected with bitline. Bitline is used to both read and write the data from/on the capacitor.

Static Random Access Memory

SRAM is also a volatile memory device, however unlike DRAM it does not require timely refresh [Shimada *et al.*, 1988]. Fig. 1.2.1 (c) shows a simple schematic of 6T SRAM cell. When WL is activated the cell comes in contact with BL and complement BL allowing both read and write operation of the cell. The cross coupled inverter of SRAM cell helps in retaining the data without the need of timely charging.

1.2.2 Non Volatile Memory Devices

As these devices can store data even in absence of power supply, these are most suitable memory for long term data storage and offline transport of data from places. ROM, flash, magnetic and optical devices are few popular NVMs available in the market.

Read Only Memory

These are the earliest electronic NVM devices and were programmed during manufacturing process and earlier it was not possible to change the written data. However, the successors Programmable ROM (PROM) and Electrically Erasable Programmable ROM (EEPROM) allowed users to change the written data. Fig. 1.2.2 (a) shows a 2X4 ROM cell schematic.

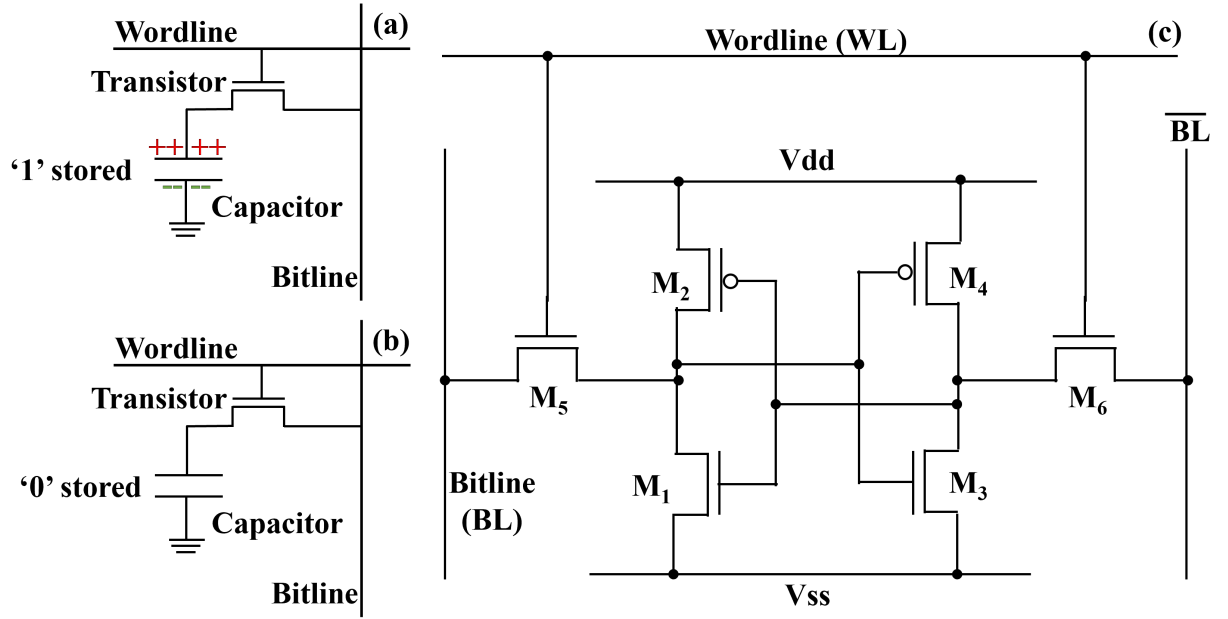


Figure 1.2.1: Schematic of the DRAM cell with (a) '1' bit stored and (b) '0' bit stored. (c) Schematic of 6T SRAM cell.

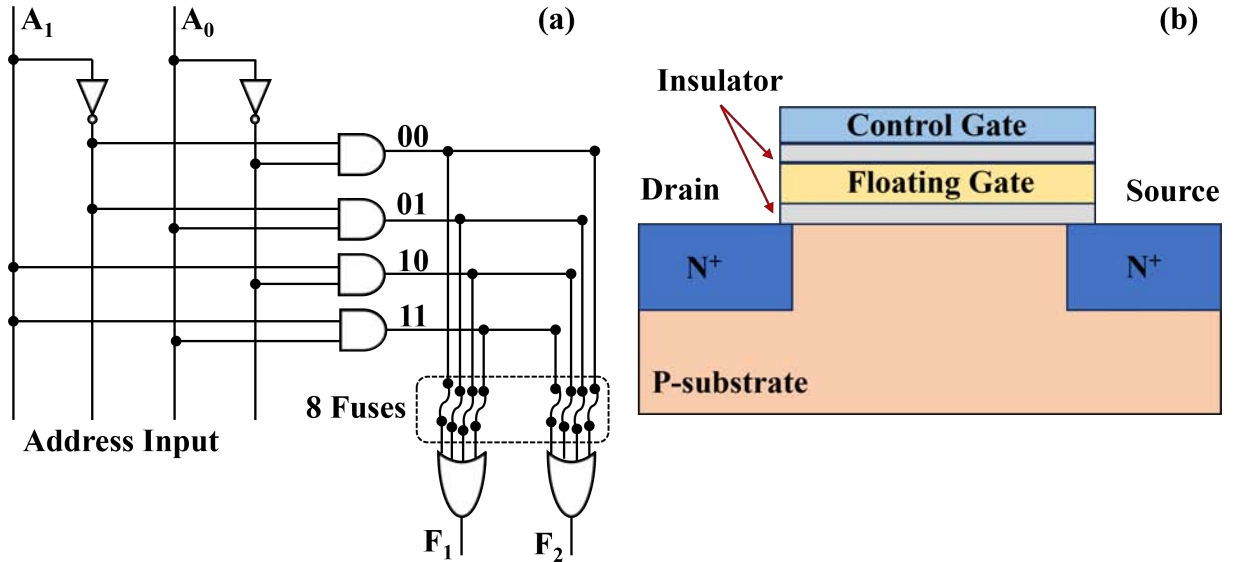


Figure 1.2.2: Schematic of (a) 2 X 4 ROM cell, and (b) floating gate flash memory cell.

Flash Memory

Fig. 1.2.2 (b) shows the schematic of floating gate flash memory device. This device stores data in the floating gate of a transistor. The write and erase process is accomplished by tunneling of electron also known as Fowler-Nordheim tunneling, and hot-electron injection process [Capasso *et al.*, 1988]. Memory cards, USB flash drive and SSDs are few popular commercially available flash memory devices.

Magnetic and Optical Devices

Magnetic devices utilize rotating disks with magnetic material coated on them to store information. Although, they are slower compared to flash memory, but they offer high storage at lower cost. Floppy disk and hard disk drive (HDD) are some popular magnetic memory devices. Similarly, optical devices use optical media to store data and laser beam to read and write the underlying data. Compact disk (CD) and Digital versatile disk (DVD) are still used to store and transport large volume of data.

1.3 Emerging Non-Volatile Memory Devices

The growing demand of higher memory density has pushed the memory devices on their scaling limit. For example, in DRAM technology at floating state, the gate induced drain leakage induces holes that reduce the threshold voltage of the transistor which in turn results in off-leakage failure. Similarly, threshold voltage that is expected to result from dopant fluctuation also rises rapidly, limiting the device performances. The trend of leakage current density and threshold voltage variation with technology node is illustrated in Fig. 1.3.1 [Hong, 2010].

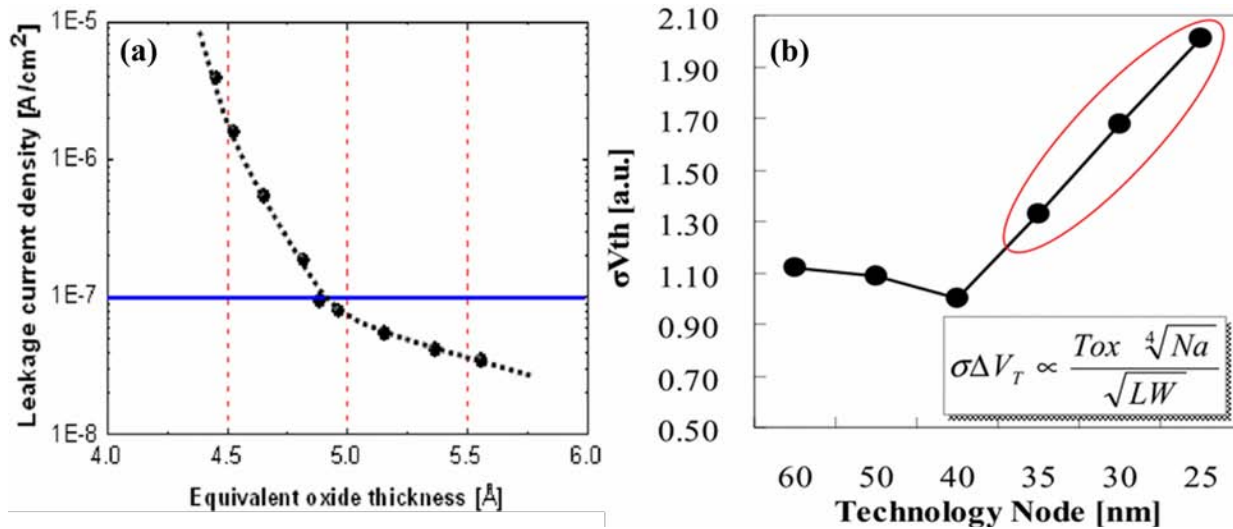


Figure 1.3.1: (a) Leakage current with equivalent oxide thickness. (b) Trend of threshold voltage variation with technology node. Image Copyright © 2010, IEEE.

Similar types of scaling limitations are prevalent in other devices as well, that motivated researches to find suitable memory devices. These new class of memory devices are often termed as emerging non-volatile memory devices, and are discussed briefly in this section.

1.3.1 Ferroelectric Random Access Memory

This memory has a simple stack structure where a ferroelectric material is sandwiched between two metal electrodes as shown in Fig. 1.3.2 (a). A ferroelectric material is capable of holding two distinct polarization states at zero voltage potential, and can switch states upon application of an electric field strong that coercive field [Scott and Paz de Araujo, 1989]. This behaviour is illustrated in Fig. 1.3.2 (b) as $P - V$ plot. The bi-stable hysteresis curve of polarization versus applied field forms the base for ferroelectric random access memory (FeRAM). The property of ferroelectric

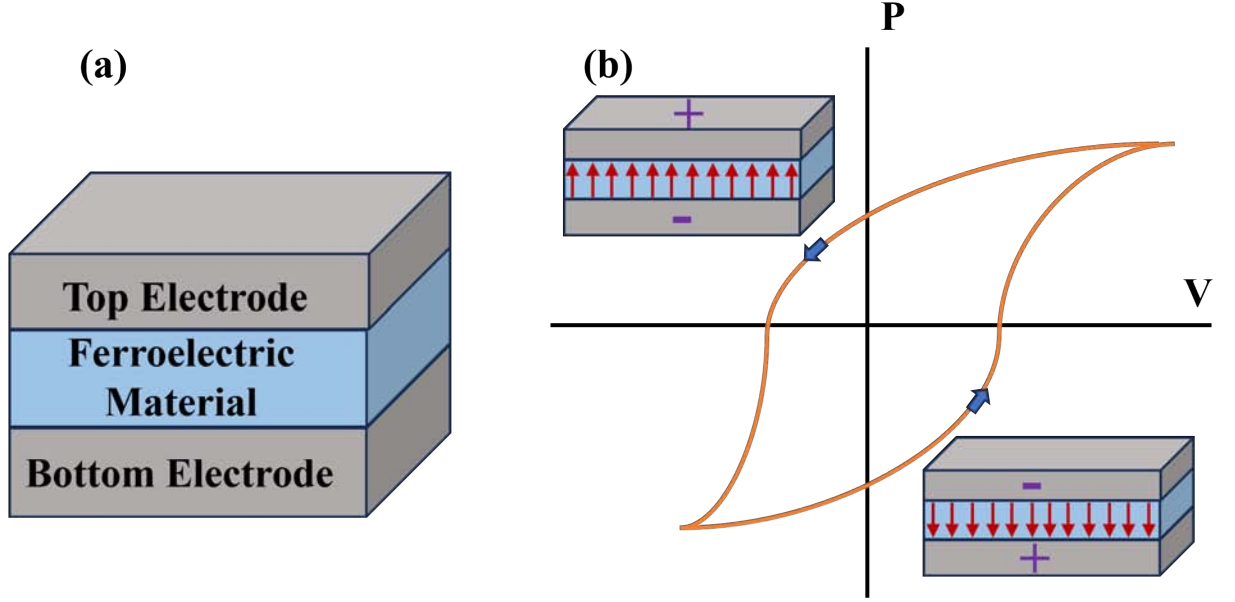


Figure 1.3.2: Schematic of (a) FeRAM cell, and (b) P - V curve showing switching of polarization with applied voltage.

requires that the material should not be centro-symmetric, as the remanent polarization occurs from the movement of ions from charge neutral position. Lead zirconium titanate (PZT), barium titanate (BTO), and strontium bismuth tantalate (SBT) are few examples of inorganic ferroelectric material. Similarly, polyvinylidene flouride (PVDF) shows β phase ferroelectric property when copolymerized with tetrafluoroethylene (TRFE) [Mikolajick *et al.*, 2020]. The concept of ferroelectric memory was first reported by *D. A. Buck* in his Masters's thesis in 1952, and later it was explored by other researchers [Buck, 1952; Campbell, 1957]. It can also be observed from Fig. 1.3.2 (b), that at any lower voltage the device state can be read and two distinct states can be achieved by switching the polarization of the material. The discovery of ferroelectricity in hafnium dioxide is an important milestone in pushing this device back in emerging memory device category [Böscke *et al.*, 2011]. However, the high coercive force (0.8-2 MV/cm) during endurance cycle results in high electrical field stress on the switching material [Mehmood *et al.*, 2019].

1.3.2 Phase Change Memory

The idea of utilizing the phase change of chalcogenides material from amorphous to crystalline for memory application was first published by Ovshinsky in 1968 [Ovshinsky, 1968]. While the concept of phase change memory (PCM) is not new, the rapid development of material and device technologies have made it possible for PCM to compete with the current technologies [Lai, 2003]. The data is stored by exploiting the large difference in resistivity between polycrystalline (SET, low resistivity) and amorphous (RESET, high resistance) phase of the switching material. Fig. 1.3.3 (a) shows a schematic of a typical mushroom configuration of the PCM device. The switching and reading of memory state is accomplished by applying an electrical pulse that generate heat to induce phase transformation in the memory device [Fong *et al.*, 2017]. Fig. 1.3.3 (b) shows the profile of set, reset, and read voltages along with the change of temperature induced in the switching layer. The reset pulse transitions the programmable region into amorphous phase

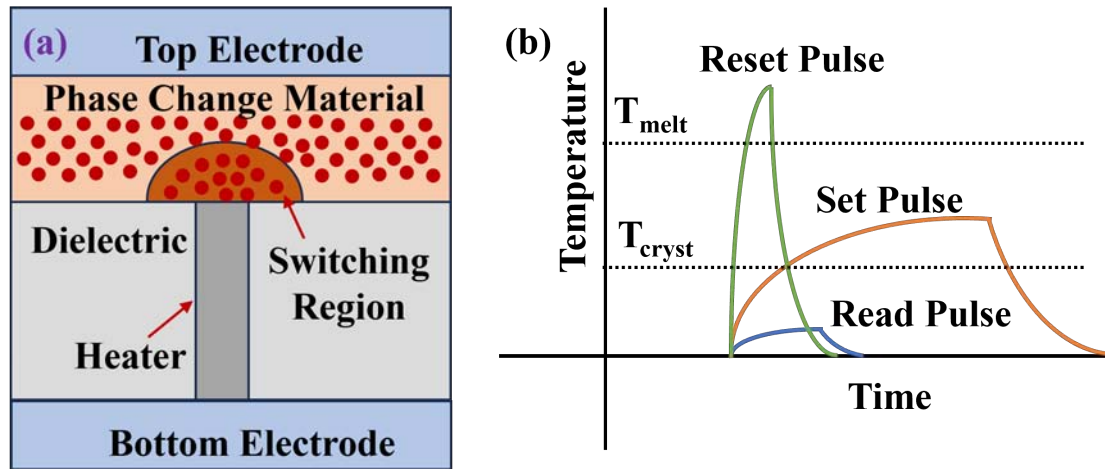


Figure 1.3.3: Schematic of (a) PCM cell, and (b) programming and reading of PCM cell by applying electrical pulses with change of temperature.

by melting and then rapidly quenching the material by utilizing large electrical pulse of short duration. Similarly, the set pulse transitions the region to crystalline phase by utilizing medium amplitude current of relatively longer duration. The read pulse is applied to measure the current state of the device without disturbing the present state of the device.

1.3.3 Spin Transfer Torque Magnetic RAM

The Nobel prize in physics in 2007 was awarded to *Albert Fert* and *Peter Grunberg* for the discovery of the giant magnetoresistance (GMR) phenomenon. The change in electrical resistance of a device with alternating ferromagnetic and non magnetic material layers, on the application of external magnetic field is referred as GMR. In 1996, *J. C. Slonczewski* and *L. Berger* independently proposed an adverse effect of GMR, the spin-transfer effect, in which the spin orientation of the magnetic layers can be tuned by utilizing external current [Slonczewski, 1996; Berger, 1996].

Fig. 1.3.4 (a) shows the schematic of a magnetic tunnel junction (MTJ) cell which consists of layers, an oxide layer between free layer and fixed layer, sandwiched between two metal electrodes. MTJ cell shows low resistance state in parallel and high resistance state in anti-parallel configuration [Zhang *et al.*, 2016]. Fig. 1.3.4 (b) and (c) shows a spin transfer torque magnetic RAM (STT-MRAM) cell that consists of one MTJ cell and one transistor in series. The resistance offered by the device depends on the magnetization or relative spin direction of the free layer and fixed layer. The different resistance states can be assigned the value of '0' and '1'. The write operation can be performed by applying a voltage to the bit line (BL) and source line (SL). When a positive voltage is applied to the BL, electrons will start to flow from fixed layer to free layer, resulting in the change of magnetization of free layer to parallel of fixed layer. Similarly, when a negative voltage is applied to the BL, the magnetization will change in anti-parallel configuration to fixed layer.

1.3.4 Resistive Random Access Memory

The resistive random access memory (RRAM) is a simple device in which an insulating layer is sandwiched between two metal electrodes i.e., top and bottom electrodes, as shown in Fig. 1.3.5

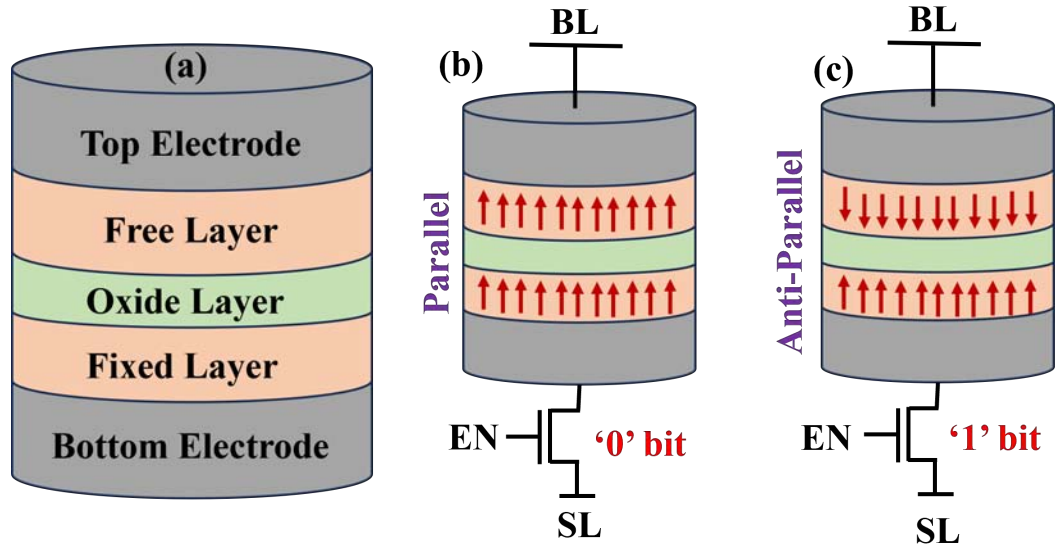


Figure 1.3.4: Schematic of (a) MTJ cell structure. STT-MRAM cell with (b) write '0', and (c) write '1' operation.

(a). The resistance of the dielectric/insulating layer changes by the application of external electric field, and these resistance states are assigned as '0' or '1' bit to be used as a digital memory. Fig. 1.3.5 (b) shows a typical $I - V$ characteristic of the RRAM device. The SET and RESET processes indicate the change of state of device from high resistance state to low resistance state and vice-versa, respectively. The change of resistance can be due to formation and dissolution of conductive filament in the dielectric/insulating medium. Mostly, the fresh fabricated device remains in high resistance state, and by application of positive voltage, its state can be changed to low resistance state. Similarly, to change the state of device from low resistance state to high resistance state, an opposite polarity of voltage is applied.

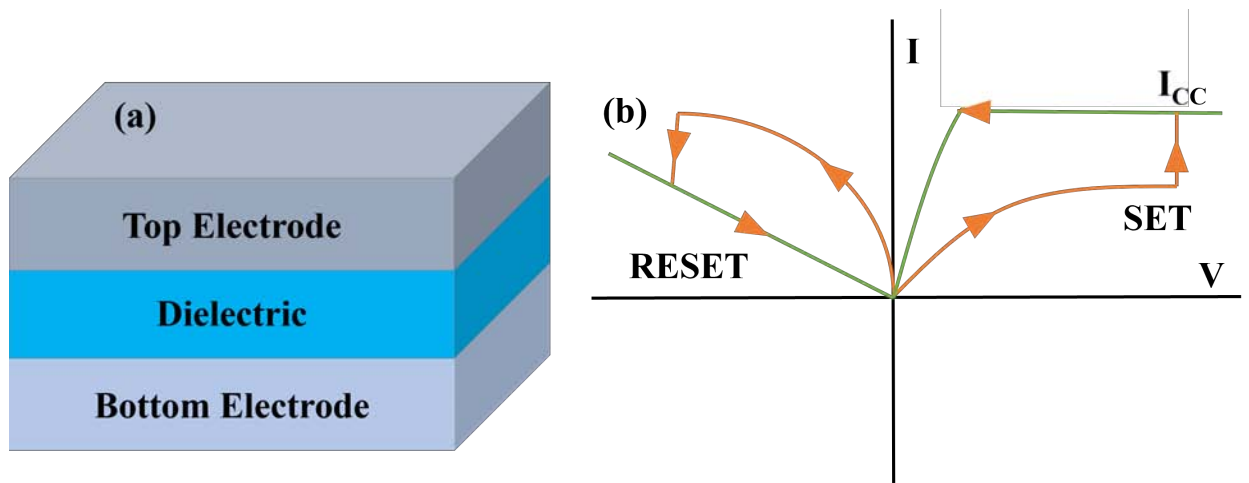


Figure 1.3.5: Schematic of (a) RRAM cell, and (b) $I - V$ characteristic of RRAM cell by applying voltage on top electrode.

RRAM device has emerged as the most suitable candidate among the emerging non-volatile

memory technologies as it has best of both memory functionalities i.e., as a working memory it has fast read-write speed, lower power operation, and good reliability, and as main memory it is non-volatile and has good memory density [Chang *et al.*, 2016]. Table 1.3.1 shows a brief comparative table of different emerging memory technologies like PCM and STT-MRAM with RRAM. Along with the mentioned advantages of RRAM, its CMOS compatibility gives it an added advantage over other memory technologies [Zahoor *et al.*, 2020].

Table 1.3.1: Comparison of few emerging memory technologies

Memory Technology	FeRAM	PCM	STT-MRAM	RRAM
Cell Area	22 F ²	4-20 F ²	6-20 F ²	< 4 F ²
Read Time	< 10 ns	< 10 ns	< 10 ns	< 10 ns
Write Time	~ 20 ns	~ 50 ns	< 10 ns	< 10 ns
Write energy	~ 0.01 pJ	~ 10 pJ	~ 0.1 pJ	~ 0.1 pJ
Multibit capacity	Yes	Yes	Yes	Yes
Non-Volatility	Yes	Yes	Yes	Yes
Scalability	Yes	Yes	Yes	Yes

1.4 Sustainable Electronics for E-waste Management

Electronic waste (e-waste) refers to the electrical and electronics devices that are no longer in active use, either because of their end of life or by choice of its owner. The unprecedented rise in e-waste is a global concern which was reflected in Global E-Waste Monitor 2024, as shown in Fig. 1.4.1. The rapid technological development makes the life cycle of electronics items shorter as a new and improved model is introduced in a short time span of few years. This drives the consumer to discard their current equipment, even if it is in working condition, and go for the new released model, which has increased the volume of worldwide generated e-waste. Moreover, the generation of e-waste is around 5 times the amount of formal collection and recycling. This poses a serious threat to both human health and ecosystem as these electronic items contain hazardous materials like lead, cadmium, and mercury.

Sustainable electronics offer a way to reduce the global impact of e-waste, as it is designed to reduce the environmental impact. The approach is to include the use of eco-friendly and biodegradable materials along with green and low cost processing techniques. An important part of this initiative is the concept of 'circular economy', in which the product is designed and manufactured in a way that their end-of-life disposal is taken care of. The utilization of nature derived, biodegradable materials to replace their inorganic and hazardous counterparts is one of the way forward for sustainable electronics. Moreover, it can be concluded that the development of sustainable electronics will play a pivotal role in e-waste management in upcoming future.

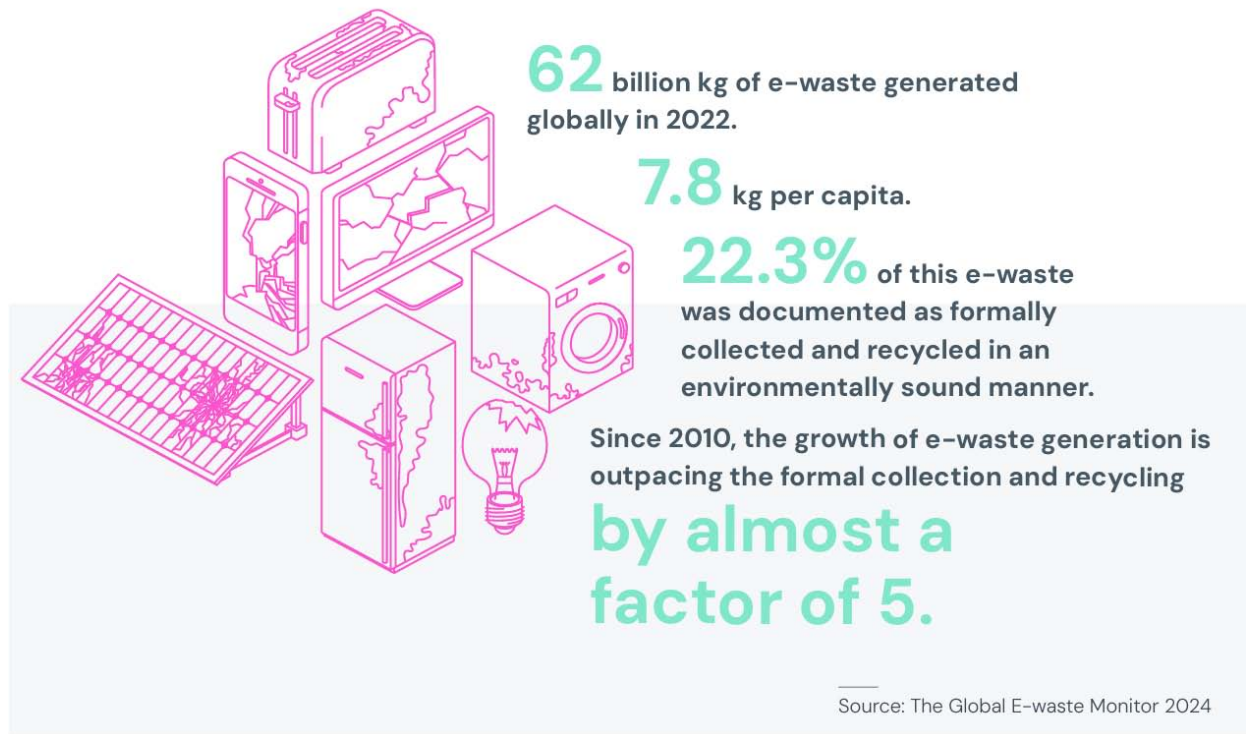


Figure 1.4.1: Illustrative executive summary of Global E-waste Monitor 2024. Image copyright © 2024 International Telecommunication Union and United Nations Institute for Training and Research, licensed under CC BY-NC-SA 3.0 IGO.

1.5 Device Model and Simulation

Device model is a set of mathematical equations that can simulate the performance characteristic of the fabricated device. Once a novel device is fabricated and improved to get reliable device performance, its model is developed to replicate the device behavior, to facilitate further simulation studies of that device. The model is referred to as a compact model when the governing equations are physics based, and most of the model parameters can be associated directly or indirectly to device performance parameters. These compact models act as the bridge between process development team and circuit design team. As fabrication is a resource demanding and costly affair, it is always recommended to first simulate the performance of the device, and for any circuit simulation a device model is a crucial part. The BSIM and HiSIM models are standard models of MOSFET, HICUM is for bipolar transistors, and ASM-HEMT and MVSG are for Gallium Nitride (GaN) transistors. The models are developed by different groups and universities with industrial collaboration for verification of their model. The Compact Model Coalition (CMC) is a group that maintains the standards of compact model, and all the above mentioned model is supported by CMC.

1.6 Thesis Organization

This thesis is organized in seven chapters. A brief description of each chapter's framework is as follows:

Chapter 1: In this chapter, an overall introduction of memory and data storage is discussed briefly. Starting from a brief history, classification, and types of memory devices, the chapter has also introductory sections on different emerging memory technologies. Lastly, a discussion on e-waste and need of sustainable electronics, followed by an introduction to device model and simulation concludes this chapter.

Chapter 2: This chapter presents a detailed introduction of resistive random access memory device. The device structure, its types, switching mechanisms, and figures of merit are discussed in detail. The chapter also discusses flexible RRAM devices followed by a discussion on utilization of organic and biodegradable materials for fabrication of flexible resistive devices.

Chapter 3: In this chapter different tools and machines that are utilized in device fabrication, material characterization, and electrical characterization are discussed briefly with their working mechanisms. The flow of data extraction from the fabricated devices, development of calibrated model, and the utilization of the calibrated model in circuit designing is also discussed briefly at the end of this chapter.

Chapter 4: This chapter presents details of device fabrication, characterization, results and discussion of Gelatin devices. Both pristine and hybrid bi-layer devices are discussed in this chapter.

Chapter 5: In this chapter, Egg-albumen as a switching layer is discussed in detail. The electrical characterizations and results of both pristine and hybrid bi-layer configuration of albumen devices are investigated in this chapter.

Chapter 6: This chapter introduces the RRAM device models, and their limitations. The fitting of Stanford model with gelatin and albumen hybrid bi-layer device to obtain model parameters is also presented. Moreover, a technique to induce cyclic variability in the compact model is discussed in detail to conclude this chapter.

Chapter 7: This chapter discussed different applications of RRAM device. Among these applications, random number generator circuit for hardware security, and synaptic behavior for neuromorphic computing are discussed in detail. The RRAM-CMOS flexible hybrid circuit is designed to generate 4-bit random number. Moreover, in next part, synaptic device is fabricated by utilizing pectin, that is obtained from orange peel.