2
Analytical Modeling of Deterministic Jitter

This chapter presents a comprehensive study for the estimation and analysis of deterministic jitter, focusing on the performance of the system in the presence of deterministic noise sources such as Power Supply Noise (PSN), Data Noise (DN), and Ground-Bounce Noise (GBN). In this, an analytical approach is used to derive the input-output relationship of CMOS inverters. Then, the expression for jitter is obtained by estimating the deviation of each transition edge from its ideal position.

2.1 Introduction

There are various techniques available in the literature used for the estimation of jitter in high-speed VLSI circuits. In [Tripathi *et al.*, 2019c], a holistic review of power supply-induced jitter (PSIJ) in high-speed VLSI circuits is presented. In this paper, several semi-analytical, analytical, statistical, and numerical methods that can be used to estimate jitter in high-speed VLSI circuits are discussed. Numerous works have been reported in the literature that focus on strategies to address Power Supply Induced Jitter (PSIJ) [Tripathi *et al.*, 2015], [Oh, 2012], [Wang and Kwasniewski, 2016], [Wang and Martin, 2013], and [Jang *et al.*, 2012].

The work in [Illikkal *et al.*, 2019] presents a semi-analytical approach to estimate PSIJ in CMOS inverters. It uses the slope-based jitter estimation technique discussed in [Tripathi *et al.*, 2017]. It also examines the sensitivity of different noise sources, provides insights into how various noise sources impact the overall performance of the circuit, and identifies the paths of noise propagation to the output. The work in [Arora *et al.*, 2021b] presents a large-signal-based analytical modeling approach used to estimate power supply-induced jitter in CMOS inverters. This technique leverages device parameters readily available in the process design kit (pdk) documentation provided by the foundry, eliminating the need to set up simulation test benches. Closed-form expressions for TIE and jitter are developed. A power supply rejection ratio (PSRR) based modeling of jitter is presented in [Sun *et al.*, 2021], where PSIJ sensitivity is evaluated using the PSRR of the driver. The voltage ripple at the supply terminal of the driver is transformed into timing deviations through the slope of the transition edges of the output response. PSIJ sensitivity for typical CMOS inverter-type drivers and for differential drivers like low-voltage differential signaling (LVDS) and current-mode differential transmitters are estimated. The work in [Chen *et al.*, 2003] presents delay-based jitter estimation method. Closed-form expressions are derived to model the variations in delay due to power and ground-level variations. It addresses the impact of power and ground noise variations on the performance of VLSI circuits. In [Kim *et al.*,

2011], a transfer function is derived analytically to determine the relationship between jitter and power supply fluctuation of the single-ended buffer. In [Hwang *et al.*, 2013], a closed-form expression is derived analytically to determine the relationship between jitter and power supply fluctuation and ground-bounce for a single-ended buffer. These transfer functions are obtained using linear differential equations obtained from asymptotic linear I-V characteristics of an inverter. Here, the noise transfer function is independently derived with respect to power supply and ground-bounce noise. Then the respective output responses are combined to estimate jitter. The work in [Wang and Kwasniewski, 2016] derives propagation delay-based expression for power supply-induced jitter sensitivity transfer function in a CMOS buffer chain. This transfer function is primarily determined by the maximum and minimum propagation delays of the buffer chain, making it very convenient to compute and practical for use in jitter budget calculations. In [Tripathi *et al.*, 2017] and [Tripathi *et al.*, 2018] slope-based jitter estimation technique is presented. This work is based on separating large signal and small signal noise responses and then combining them to obtain the overall response of the system. Simplified expressions for PSIJ are derived based on the slope of the rising and falling edges of the output signal.

As highlighted earlier, significant research has been conducted on modeling PSN-induced jitter. Some of them employ small-signal-based approaches to derive noise transfer functions in order to model jitter in CMOS inverters. These techniques consist of semi-analytical approaches, which are based on several assumptions and approximations and are not totally independent of SPICE simulators.

This work employs a large-signal-based analytical approach to establish input-output relationships. It uses the current equations of the transistors to obtain the differential equations. In this proposed analytical method, device parameters are taken into account to model the timing uncertainty. The expression for jitter is derived by estimating the deviation of each transition edge from its ideal position. Several examples, including simulations as well as measurements, are presented to validate the proposed modeling approach. These examples involve comparing the analytical results with the simulation results obtained using a SPICE-based simulator and measurement results, and are verified by considering different technology nodes and hex inverter ICs.

2.2 Theoretical Development and Derivation of Input-Output Relationship

This section discusses the behavior of the CMOS inverter in the presence of PSN, DN, and GBN. To determine the input-output relationship of the CMOS inverter for a rising/falling transition edge of the input, it is very crucial to identify the operating mode of the transistors at various voltage levels of the input data throughout its rising/falling transition. Knowledge of operating modes enables us to deduce the differential equations accurately during the transition edges. Figure 2.2.1 illustrates the CMOS inverter with the PSN, DN, and GBN. With the changing voltage level of the input transition edge, both the transistors, M_p and M_n, will dynamically enter into the different conduction modes, such as linear, cutoff, and saturation [Bisdounis *et al.*, 1998]. The charge feed-through across the gate-to-drain capacitors C_{gd_p} and C_{gd_n} of the transistors is also considered to reflect the initial overshoot [Huang *et al.*, 2010]. The capacitor C_M is the sum of the gate-to-drain capacitance of the transistors M_p and M_n, respectively, and is given by

$$C_M = C_{gd_p} + C_{gd_n}. \tag{2.1}$$

Further, the gate-to-drain capacitance of the transistor is the sum of the gate-to-drain overlap capacitance and a part of the gate-to-drain channel capacitance [Razavi, 2017], and [Weste and

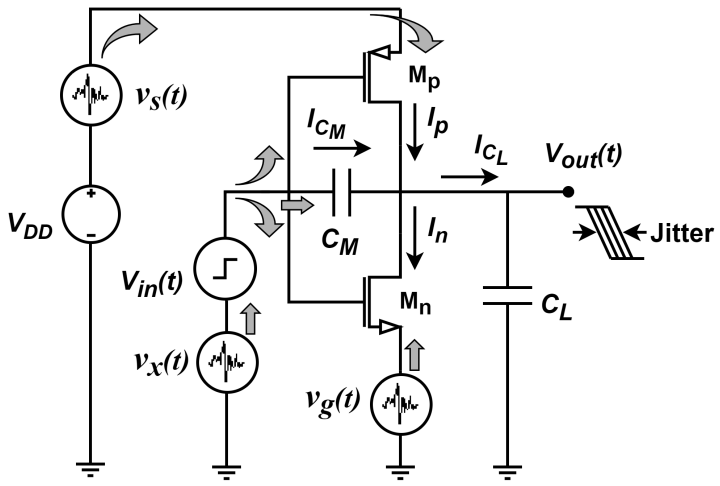


Figure 2.2.1: Model of CMOS inverter in the presence of Noise.

Harris, 2015]. The overlap capacitance is independent of voltage and can be written as:

$$C_{gd_{overlap}} = WC_{gd_o}, \tag{2.2}$$

where W is the width of the transistor, C_{gd_o} is the gate-to-drain overlap capacitance per unit area, determined by process technology. When a transistor operates in the cutoff mode, no conducting channel is formed, and in the saturation mode, the channel does not reach the drain terminal. Consequently, the component of gate-to-drain capacitance contributed by the channel charge is zero in both operating modes, leaving only the overlap capacitance. In the linear mode, the distributed gate-to-channel capacitance can be considered as being shared equally between the source and the drain [Arora *et al.*, 2021b], [Li, 2007], [Huang *et al.*, 2010], and [Wang *et al.*, 1971]. Therefore, in this mode of operation, the expression for the gate-to-drain capacitance due to the channel charge ($C_{gd_{channel}}$) is given by:

$$C_{gd_{channel}} = \frac{1}{2}C_{ox}WL. \tag{2.3}$$

For the simplified analysis, other parasitics are neglected. The current equations for different modes of conduction (such as Cutoff, Linear, and Saturation) of the transistors are written as:

- For nMOS Transistor:

$$I_n = 0, \qquad V_{in} < V_{TN} \qquad \text{Cutoff Mode} \tag{2.4}$$

$$I_n = \frac{\beta_n}{2(1+\delta_n)}(V_{in} - V_{TN})^2, \qquad V_{out} > V_{sat_n} \qquad \text{Saturation Mode} \tag{2.5}$$

$$I_n = \beta_n\left[(V_{in} - V_{TN})V_{out} - \frac{1+\delta_n}{2}V_{out}^2\right], \qquad V_{out} \leq V_{sat_n} \qquad \text{Linear Mode} \tag{2.6}$$

where V_{TN} is the threshold voltage of nMOS transistor and δ_n is a constant term obtained from the Taylor Series expansion of the bulk charge equation on nMOS transistor. The term β_n is the transconductance parameter, and V_{sat_n} is the saturation voltage of the transistor, which can be expressed as [Tsividis, 2004], and [Weste and Harris, 2015]:

$$\beta_n = \mu_n C_{ox}\left(\frac{W_n}{L_n}\right), \tag{2.7}$$

$$V_{sat_n} = V_{DD} - \frac{(V_{in} - V_{TN})}{1 + \delta_n} \tag{2.8}$$

- For pMOS Transistor:

$$I_p = 0, \qquad V_{in} > (V_{DD} - |V_{TP}|) \qquad \text{Cutoff Mode} \tag{2.9}$$

$$I_p = \frac{\beta_p}{2(1+\delta_p)}(V_{DD} - V_{in} - |V_{TP}|)^2, \qquad V_{out} < V_{sat_p} \qquad \text{Saturation Mode} \tag{2.10}$$

$$I_p = \beta_p \left[(V_{DD} - V_{in} - V_{TP})(V_{DD} - V_{out}) - \frac{(1+\delta_p)}{2}(V_{DD} - V_{out})^2 \right], \quad V_{out} \geq V_{sat_p} \quad \text{Linear Mode} \tag{2.11}$$

where V_{TP} is the threshold voltage of pMOS transistor and δ_p is a constant term obtained from the Taylor Series expansion of the bulk charge equation on pMOS transistor. The term β_p is the transconductance parameter, and V_{sat_p} is the saturation voltage of the transistor, which can be expressed as [Tsividis, 2004], and [Weste and Harris, 2015]:

$$\beta_p = \mu_p C_{ox} \left(\frac{W_p}{L_p} \right), \tag{2.12}$$

$$V_{sat_p} = V_{DD} - \frac{(V_{DD} - V_{in} - |V_{TP}|)}{1 + \delta_p} \tag{2.13}$$

These current equations are further used to derive the input-output relationship of the Inverter in the presence of various noise sources.

Here, the instantaneous fluctuating noise at the supply, data, and ground terminals affects the output response of the circuit. Due to these noise sources, the transition edges of the output signal of the inverter shift from their ideal positions (i.e., the output response of the CMOS inverter in the absence of noise). These shifts in the transition edges cause timing uncertainty in the output data. This timing uncertainty is modeled in terms of time interval error (TIE) and eventually as jitter at the output. The shift in the transition edges depends on various factors like parasitics, conduction mode, threshold voltages of the transistors, load capacitance (C_L), and the rise/fall times of the input signal [Sakurai and Newton, 1991]. In the case of a fast-switching input signal, one of the transistors remains in the cutoff mode, and the other will operate either in saturation or in linear mode at the midpoint (i.e., at $V_{DD}/2$ voltage level) of the rising/falling transition edge of the output. For the case of rising transition edge of the input signal, the transistor M_n will conduct in linear mode, and M_p will conduct in cutoff mode [Arora *et al.*, 2021a] at the corresponding falling transition edge of the output signal. Since M_n is operating in linear mode, the ground noise will be in a direct path with the output node, and the effect of PSN can not be seen directly through the equations. The effect of supply noise will be propagated through some common constants that are used to maintain continuity between the different regions (will be discussed in the subsequent section of this chapter). Thus, noise at the supply, data, and ground terminals causes a timing variation in the transition edges of the output signal. Therefore, it can be said that the PSN, DN, and GBN combinedly introduce jitter at the output. The falling transition edges of the input signal will follow the same procedure [Arora *et al.*, 2021b].

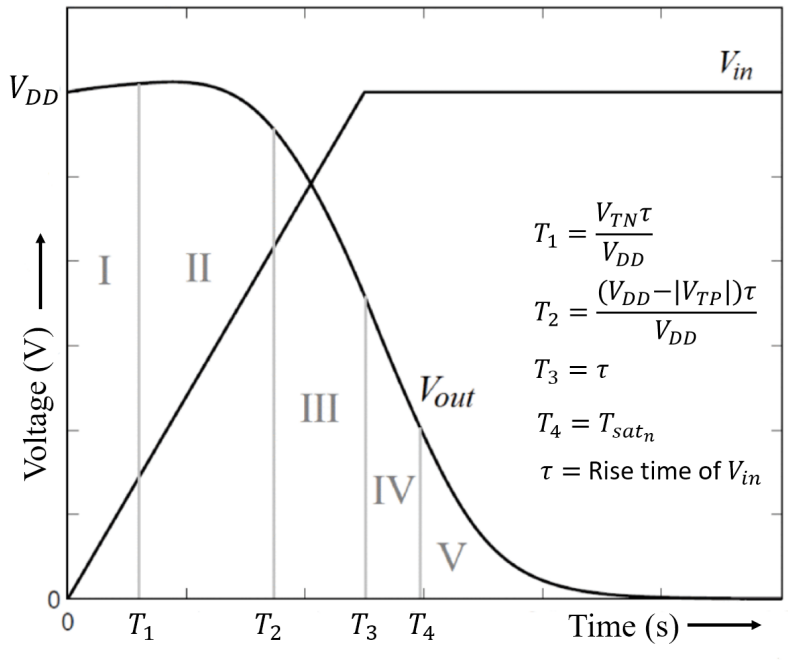


Figure 2.2.2: Depiction of different regions in the output response of CMOS inverter in the presence of fast input ramp signal.

2.2.1 Derivation of the Input-Output Relationship

This work considers only the rising ramp input for jitter analysis, and the corresponding falling edge of the output response is shown in Figure 2.2.2. The expression for the input ramp signal is given by

$$V_{in}(t) = \begin{cases} 0, & \text{if} \quad t < 0 \\ V_{DD}(t/\tau), & \text{if} \quad 0 \leq t < \tau \\ V_{DD}, & \text{if} \quad t \geq \tau \end{cases}. \tag{2.14}$$

where τ is the rise time of the input signal. To analytically model the output expression of the inverter, the entire falling edge of the output is divided into five different regions[1] as shown in Figure 2.2.2. The output in all the regions is affected by PSN, DN, and GBN accordingly. Since the midpoint ($V_{DD}/2$) of the output falls in Region-IV, the jitter analysis is done at this point. As every consecutive region is interlinked with the previous one, the complete analysis of all the regions becomes necessary for such a study.

The following subsections describe the Taylor series representation of ground noise and the input-output relationship for different regions, as shown in Figure 2.2.2, which is obtained by solving the differential equation for all the respective regions.

[1]It should be noted that these 'regions' from I to V are the regions of the output response of the inverter. The readers should not get confused with transistor operation 'region', e.g., linear, cutoff, and saturation. Therefore, 'mode' is used for the transistor operating region.

A: Taylor series Representation of Noise Source

The small-signal noise sources $v_s(t)$, $v_x(t)$, and $v_g(t)$ are inserted at the power supply, input data, and ground terminal of the inverter, as shown in Figure 2.2.1. For the case of single-tone noise source $v_s(t) = A_{s_1} \sin(\omega_{s_1} t + \phi_{s_1})$ (here only noise source at the supply terminal is given, rest of them follow the same representation) the Taylor series expansion of the noise can be represented as

$$v_s(t) = A_{s_1} \sin\phi_{s_1} + \sum_{k=1}^{\infty} s_{1_k} t^k, \tag{2.15}$$

where

$$s_{1_1} = A_{s_1} \omega_{s_1} \cos\phi_{s_1}, \tag{2.16}$$

$$s_{1_2} = -A_{s_1} \frac{\omega_{s_1}^2}{2} \sin\phi_{s_1}, \tag{2.17}$$

and

$$s_{1_k} = A_{s_1} \frac{\omega_{s_1}^k}{k!} \cdot sgn(s_{1_{k-1}}) \cdot \left(\frac{(1-(-1)^{k-1})}{2} \sin\phi_{s_1} + \frac{(1-(-1)^k)}{2} \cos\phi_{s_1} \right). \tag{2.18}$$

Now, let's consider a multi-tone sinusoidal noise source which can be represented as:

$$v_s(t) = A_{s_1} \sin(\omega_{s_1} t + \phi_{s_1}) + A_{s_2} \sin(\omega_{s_2} t + \phi_{s_2}) ..... + A_{s_n} \sin(\omega_{s_n} t + \phi_{s_n}), \tag{2.19}$$

where A_{s_n}, ω_{s_n} and, ϕ_{s_n} are the amplitude, fundamental frequency in radian and initial phase of the nth sinusoidal noise source, respectively. The Taylor series expression of the multi-tone noise source can be given as:

$$v_s(t) = \sum_{n=0}^{N} A_{s_n} \sin\phi_{s_n} + \sum_{n=0}^{N} \sum_{k=1}^{\infty} s_{n_k} t^k, \tag{2.20}$$

where,

$$s_{n_1} = A_{s_n} \omega_{s_n} \cos\phi_{s_n}, \tag{2.21}$$

$$s_{n_2} = -A_{s_n} \frac{\omega_{s_n}^2}{2} \sin\phi_{s_n}, \tag{2.22}$$

and

$$s_{n_k} = A_{s_n} \frac{\omega_{s_n}^k}{k!} \cdot sgn(s_{n_{k-1}}) \cdot \left(\frac{(1-(-1)^{k-1})}{2} \sin\phi_{s_n} + \frac{(1-(-1)^k)}{2} \cos\phi_{s_n} \right) \tag{2.23}$$

where $sgn(y)$ represents the sign of any real number y, and s_{n_k} is the coefficients of the kth harmonic of nth sinusoidal in the Taylor series expansion. However, the series representation of any signal only approximates the signal, and using this approximation, the signal generation may not converge after a time instant longer than its time period. As a result, the above Taylor series expression (2.20) must be repeated after every $2\pi/\omega$ interval for the kth harmonic to produce the original signal. The Taylor series expression of noise will be further considered to determine the input-output relationship for various regions.

B: Output in the presence of Supply, Data, and Ground-bounce noise

As previously stated, with the rising input signal, the biasing voltage of the transistors changes, causing the transistors to conduct in different modes. Therefore, for the purpose of analysis, the inverter output is divided into five distinct regions, as shown in Figure 2.2.2. Based on these re-

gions, a complete study of input-output relationships of the inverter is performed, considering the effect of all the noise sources.

The input-output relationship of the inverter is obtained by applying Kirchhoff's Current Law (KCL) at the output node as:

$$I_{C_M} + I_p - I_{C_L} - I_n = 0, \tag{2.24}$$

$$-(C_L + C_M)\frac{d}{dt}V_{out} + C_M\frac{d}{dt}(V_{in} + v_x(t)) + I_p - I_n = 0 \tag{2.25}$$

where I_{C_M}, I_{C_L}, I_p, and I_n are the currents through C_M, C_L, drain to source current of pMOS, and drain to source current of nMOS, respectively.

Output Response in Region-I:

In this region, the input is rising from 0 to V_{TN}. Here, V_{TN} is the threshold voltage of nMOS. As in this region, the output is at its level high, which makes the transistor M_p to operate in the linear mode and the transistor M_n to operate in the cutoff mode. Thus, the currents I_n and I_p are given as:

$$I_n = 0, \tag{2.26}$$

$$I_p = \beta_p\left[(V_{DD} + v_s(t) - V_{in} - v_x(t) - |V_{TP}|)\cdot(V_{DD} + v_s(t) - V_{out}) - \frac{(1+\delta_p)}{2}(V_{DD} + v_s(t) - V_{out})^2\right], \tag{2.27}$$

where β_p is the conduction parameter, μ_p is the mobility of holes, C_{ox} is the oxide capacitance and W_p/L_p is the aspect ratio, V_{TP} is the threshold voltage, and δ_p is the slope of first-order term in the Taylor series expansion of the bulk-charge equation of transistor M_p [Bisdounis *et al.*, 1998], [Tsividis, 2004]. Considering the effect of supply, data, and ground-bounce noise, the expression for input-output relationship is obtained by applying KCL at the output node of CMOS inverter and is given as:

$$\begin{aligned}\frac{d}{dt}(V_{out}) - \gamma\frac{d}{dt}(V_{in} + v_x(t)) + \eta\Big[&(V_{DD} + v_s(t) - V_{in} - v_x(t) - |V_{TP}|)\cdot(V_{DD} + v_s(t) - V_{out}) \\ &- \frac{(1+\delta_p)}{2}(V_{DD} + v_s(t) - V_{out})^2\Big] = 0,\end{aligned} \tag{2.28}$$

where,

$$\begin{aligned}\gamma &= \frac{C_M}{(C_L + C_M)}, \\ \text{and} \quad \eta &= \frac{\beta_p}{(C_L + C_M)}.\end{aligned} \tag{2.29}$$

Here, the differential equation (2.28) is a non-linear Riccati equation that can not be solved unless its particular solution is known. Therefore, to solve this equation, the power-series method is applied [Riley and Hobson., 2011]. The expression for output in this region can be written as

$$V_{out}(t) = V_{DD} + \sum_{n=1}^{N} A_{s_n}\sin\phi_{s_n} + \sum_{n=1}^{N}\sum_{k=1}^{\infty}(s_{n_k} - a_{n_k})t^k, \tag{2.30}$$

where a_{n_k} is the coefficient of t^kth term in the series. Substituting (2.30) in (2.28), these coefficients

are calculated as:

$$a_{n_1} = s_{n_1} - \gamma\left(\frac{V_{DD}}{\tau} + x_{n_1}\right), \tag{2.31}$$

$$a_{n_2} = s_{n_2} - \gamma x_{n_1} - \frac{a_{n_1}\eta}{2}(V_{DD} + A_{s_n}\sin\phi_{s_n} - A_{x_n}\sin\phi_{x_n} - V_{TP}), \tag{2.32}$$

$$\begin{aligned} a_{n_3} = s_{n_3} - \gamma x_{n_3} - \frac{\eta}{3}\Big[&(V_{DD} + A_{s_n}\sin\phi_{s_n} - A_{x_n}\sin\phi_{x_n} - |V_{TP}|)a_{n_2} - \frac{V_{DD}}{\tau}a_{n_1} \\ &+ (s_{n_1} - a_{n_1})a_{n_1} - \frac{(1+\delta_p)}{2}a_{n_1}^2\Big], \end{aligned} \tag{2.33}$$

and from mathematical indication, the kth coefficient can be given by:

$$\begin{aligned} a_{n_k} = s_{n_k} - \gamma x_{n_k} - \frac{\eta}{k}\Big[&(V_{DD} + A_{s_n}\sin\phi_{s_n} - A_{x_n}\sin\phi_{x_n} - |V_{TP}|)a_{n_{k-1}} - \frac{V_{DD}}{\tau}a_{n_{k-2}} \\ &+ \sum_{i=0}^{k-2}(s_{n_i} - x_{n_i})a_{n_{k-i-1}} - \frac{(1+\delta_p)}{2}\sum_{i=1}^{k-2}a_k a_{n_{k-i-1}}\Big]. \end{aligned} \tag{2.34}$$

Output Response in Region-II:

In this region, the input voltage will be rising from V_{TN} to $(V_{DD} - |V_{TP}|)$. Hence, the nMOS will start operating in saturation mode, and the pMOS will remain in linear mode. The M_n transistor will remain in saturation mode as long as $V_{out} \geq V_{sat_n}$. Equations for this region are as follows:

$$V_{sat_n} = \frac{(V_{in} - V_{TN})}{1+\delta_n},$$

$$I_n = \frac{\beta_n}{2(1+\delta_n)}(V_{in} + v_x(t) - v_g(t) - V_{TN})^2, \tag{2.35}$$

where β_n is the conduction parameter, μ_n is the mobility of electron, W_n/L_n is the aspect ratio, and δ_n is the slope of the first order term in the Taylor series expansion of the bulk-charge equation of transistor M_n [Bisdounis *et al.*, 1998] and [Tsividis, 2004].

$$I_p = \beta_p\left[(V_{DD} + v_s(t) - V_{in} - v_x(t) - |V_{TP}|)\cdot(V_{DD} + v_s(t) - V_{out}) - \frac{(1+\delta_p)}{2}(V_{DD} + v_s(t) - V_{out})^2\right]. \tag{2.36}$$

Thus, the differential equation in this region is written as:

$$\begin{aligned} \frac{d}{dt}(V_{out}) - \gamma\frac{d}{dt}(V_{in} + v_x(t)) - \eta\Big[&(V_{DD} + v_s(t) - V_{in} - v_x(t) - |V_{TP}|)\cdot(V_{DD} + v_s(t) - V_{out}) \\ &- \frac{(1+\delta_p)}{2}(V_{DD} + v_s(t) - V_{out})^2\Big] - \frac{\zeta}{2}(V_{in} + v_x(t) - v_g(t) - V_{TN})^2 = 0, \end{aligned} \tag{2.37}$$

where γ and η are same as in Region-I and,

$$\zeta = \frac{\beta_n}{(1+\delta_n)(C_L + C_M)}. \tag{2.38}$$

Here, the differential equation (2.37) is also a non-linear Riccati equation. Therefore, this equation is also solved using the power series method as:

$$V_{out}(t) = V_{DD} + \sum_{n=1}^{N} A_{s_n} \sin\phi_{s_n} + \sum_{n=1}^{N}\sum_{k=1}^{\infty}(s_{n_k} - b_{n_k})(t-T_1)^k + V_{12}, \tag{2.39}$$

where $V_{12} = \sum_{n=1}^{N}\sum_{k=1}^{\infty}(s_{n_k} - a_{n_k})T_1^k$ is a constant at time instance $T_1 = \tau(V_{TN}/V_{DD})$ and which needs to be added to the output to maintain the continuity between Region-I and Region-II. Here, b_{n_k} is the coefficient of t^kth term in power series solution of (2.37), and is given as:

$$b_{n_1} = s_{n_1} - \gamma\left(\frac{V_{DD}}{\tau} + x_{n_1}\right) + \frac{\zeta}{2}(A_{x_n}\sin\phi_{x_n} - A_{g_n}\sin\phi_{g_n})^2, \tag{2.40}$$

$$b_{n_2} = s_{n_2} - \gamma x_{n_2} - \frac{\eta}{2}Qb_{n_1} + \frac{\zeta}{2}\left(\frac{V_{DD}}{\tau} + x_{n_1} - g_{n_1}\right)\cdot(A_{x_n}\sin\phi_{x_n} - A_{g_n}\sin\phi_{g_n}), \tag{2.41}$$

$$\begin{aligned} b_{n_3} = s_{n_3} - \gamma x_{n_3} - \frac{\eta}{3}\left[Qb_{n_2} - \frac{V_{DD}}{\tau}b_{n_1} + (s_{n_1} - x_{n_1})b_{n_1} - \frac{1+\delta_p}{2}b_{n_1}^2\right] \\ + \frac{\zeta}{6}\left[\left(\frac{V_{DD}}{\tau} + x_{n_1} - g_{n_1}\right)^2 + 2(A_{x_n}\sin\phi_{x_n} - A_{g_n}\sin\phi_{g_n})(x_{n_1} - g_{n_1})\right], \end{aligned} \tag{2.42}$$

and

$$\begin{aligned} b_{n_k} = s_{n_k} - \gamma x_{n_k} - \frac{\eta}{k}\left[Qb_{n_{k-1}} + \sum_{i=1}^{k-2}(s_{n_i} - x_{n_i})b_{n_{k-i-1}} - \frac{V_{DD}}{\tau}b_{n_{k-2}} - \frac{1+\delta_p}{2}\sum_{i=1}^{k-2}b_{n_i}b_{n_{k-i-1}}\right] \\ + \frac{\zeta}{2k}\left[\frac{2V_{DD}}{\tau}(x_{n_{k-2}} - g_{n_{k-2}}) + 2(A_{x_n}\sin\phi_{x_n} - A_{g_n}\sin\phi_{g_n})(x_{n_{k-1}} - g_{n_{k-1}})\right. \\ \left. + \sum_{i=1}^{k-2}(x_{n_i} - g_{n_i})(x_{n_{k-i-1}} - g_{n_{k-i-1}})\right], \end{aligned} \tag{2.43}$$

where $Q = (V_{DD} + A_s\sin\phi_s - A_x\sin\phi_x - V_{TN} - |V_{TP}|)$.

Output Response in Region-III:

In this region, the input voltage is rising from $(V_{DD} - |V_{TP}|)$ to V_{DD}, nMOS will remain in the saturation mode, and pMOS will enter into the cutoff mode. The current equation can be given as:

$$I_n = \frac{\beta_n}{2(1+\delta_n)}(V_{in} + v_x(t) - v_g(t) - V_{TN})^2, \quad I_p = 0. \tag{2.44}$$

Thus, the input-output relationship for this region is written as:

$$\frac{d}{dt}(V_{out}) - \gamma\frac{d}{dt}(V_{in} + v_x(t)) + \frac{\zeta}{2}f_1(t) = 0, \tag{2.45}$$

where $f_1(t) = (V_{in} + v_x(t) - v_g(t) - V_{TN})^2$ and γ and ζ are same as in previous regions. Here, (2.45) is an ordinary linear differential equation. Thus, the solution of differential equation in (2.45) can

be obtained as:

$$V_{out}(t) = \frac{\gamma V_{DD}}{\tau}(t - T_2) + \gamma \sum_{n=1}^{N} \left(A_{x_n} \sin \phi_{x_n} + \sum_{k=1}^{\infty} x_{n_k} (t - T_2)^k \right) - \frac{\zeta}{2} \int f_1(t - T_2) dt + V_{23}, \tag{2.46}$$

where $T_2 = \tau(V_{DD} - V_{TP})/V_{DD}$ and

$$V_{23} = V_{DD} + \sum_{n=1}^{N} (A_{s_n} \sin \phi_{s_n} - \gamma A_{x_n} \sin \phi_{x_n}) + \sum_{n=1}^{N} \sum_{k=1}^{\infty} (s_{n_k} - b_{n_k})(T_2 - T_1)^2 + V_{12}.$$

It is the constant term (V_{23}) that needs to be added to maintain the continuity between Region-II and Region-III.

Output Response in Region-IV:

In this region, the input voltage becomes equal to V_{DD}, and similar to Region-III, the nMOS and pMOS stay in the saturation and cutoff modes, respectively. Thus, the input-output relationship for this region is expressed as:

$$\frac{d}{dt}(V_{out}) = \gamma \frac{d(V_{in}(t) + v_x(t))}{dt} - \frac{\zeta}{2}(V_{DD} + v_x(t) - v_g(t) - V_{TN})^2. \tag{2.47}$$

Here, (2.47) is also an ordinary differential equation, the solution of which can be given as:

$$V_{out}(t) = \gamma \left(V_{DD} + A_{x_n} sin\phi_{x_n} + \sum_{k=1}^{\infty} x_{n_k} (t - \tau)^k \right) - \frac{\zeta}{2} \int f_2(t - \tau) dt; \tag{2.48}$$

where ζ is same as in previous regions and $f_2(t) = (V_{DD} + v_x(t) - v_g(t) - V_{TN})^2$. Further, simplifying (2.48), the output expression can be written as:

$$\begin{aligned} V_{out}(t) = V_{34} + \gamma \left(V_{DD} + A_{x_n} sin\phi_{x_n} + \sum_{k=1}^{\infty} x_{n_k} (t - \tau)^k \right) - \frac{\zeta}{2} \sum_{n=1}^{N} \Bigg[\psi^2 (t - T_3) \\ + 2\psi \sum_{k=1}^{\infty} \frac{(x_{n_k} - g_{n_k})}{k+1} \cdot (t - T_3)^{k+1} + \sum_{k=2}^{\infty} \sum_{i=1}^{k-1} \frac{(x_{n_i} - g_{n_i})(x_{n_{k-i}} - g_{n_{k-i}})}{k+1} (t - T_3)^{k+1} \Bigg]; \end{aligned} \tag{2.49}$$

where $\psi = (V_{DD} - A_{x_n} \sin \phi_{x_n} - A_{x_n} \sin \phi_{x_n} - V_{TN})$, $T_3 = \tau$ is the rise time, and V_{34} is the constant term needs to added to maintain the continuity between Region-III and Region-IV, and obtained by subtracting the output of Region-III from output of Region-IV at $t = \tau$.

Output Response in Region-V:

The drain to source voltage across the nMOS transistor starts falling when the output voltage drops from Region-II to all the successive regions. Since, in this region, the input is fixed at V_{DD}, and when the continuously decreasing output voltage reaches below V_{sat_n}, it will make M_n to conduct in linear mode, and M_p transistor will still remain in cutoff mode. Therefore, the input-

output relationship for this region will be:

$$\frac{d}{dt}(V_{out}) - \gamma\frac{d}{dt}(V_{in}+v_x(t)) + \sigma\Big[(V_{in}+v_x(t)-v_g(t)-V_{TN})(V_{out}-v_g(t)) - \frac{(1+\delta_n)}{2}(V_{out}-v_g(t))^2\Big] = 0; \quad (2.50)$$

where,

$$\sigma = \frac{\beta_n}{C_L + C_M}, \quad (2.51)$$

and γ, and ψ are same as in previous regions. Here, (2.50) is also a non-linear Riccati differential equation similar to those in Region-I and Region-II. Therefore, the solution of this equation is also derived similarly. Thus, the output expression for this region can be expressed as:

$$V_{out}(t) = \sum_{n=1}^{N}\left[d_{n_0} + A_{g_n}\sin\phi_{g_n} + \sum_{k=1}^{\infty}(d_{n_k}+g_{n_k})(t-T_4)^k\right]; \quad (2.52)$$

where $T_4 = T_{sat_n}$ is the time instance when $V_{out} = V_{sat_n}$ obtained from (2.52), d_{n_0} is the constant term, d_{n_k} is the coefficient of t^kth term of power series solution are as follows:

$$d_{n_0} = \frac{V_{DD}-V_{TN}}{1+\delta_n} - A_{g_n}\sin\phi_{g_n}, \quad (2.53)$$

$$d_{n_1} = -g_{n_1} + \gamma x_{n_1} - \sigma\Big[\psi d_{n_0} - \frac{(1+\delta_n)}{2}d_{n_0}^2\Big], \quad (2.54)$$

$$d_{n_2} = -g_{n_2} + \gamma x_{n_2} - \frac{\sigma}{2}\Big[\psi d_{n_1} - (x_{n_1}-g_{n_1})d_{n_0} - \frac{(1+\delta_n)}{2}(2d_{n_0}d_{n_1})\Big]. \quad (2.55)$$

From the mathematical indication the kth term can be written as

$$d_{n_k} = -g_{n_k} + \gamma x_{n_k} - \frac{\sigma}{k}\Bigg[\psi d_{n_{k-1}} - (x_{n_{k-1}}-g_{n_{k-1}})d_{n_0} - \sum_{i=1}^{k-2}(x_{n_i}-g_{n_i})d_{n_{k-i-1}} - \frac{(1+\delta_n)}{2}\cdot \left(2d_{n_0}d_{n_{k-1}} + \sum_{i=1}^{k-2}d_{n_i}d_{n_{k-i-1}}\right)\Bigg]. \quad (2.56)$$

As the input-output relationships for all the regions are derived considering the noise (expression (2.20)) at the power supply, data, and ground terminal, the overall response can be achieved by concatenating these responses in time. The validation of the result is done using corner simulation. For this, an input signal (rising from 0 to 1.2 V) having a rise time of 50 psec is applied to the inverter. The inverter is designed in 40 nm UMC technology, and the load capacitance of 10 fF is connected to the output. To validate the analytical modeling, the process corners simulations are carried out using the analytical approach and SPICE-based simulator without considering the effect of any noise. A comparison has been made between the output voltages obtained from both methods for different device models of specific process corners, such as typical (TT), fast (FF), and slow (SS), provided by the technology file of the UMC for given corner conditions, respectively. A good match can be seen in the results of both analytical and simulation approaches, as shown in Figure 2.2.3, which validates the derived input-output relationships for all the regions.

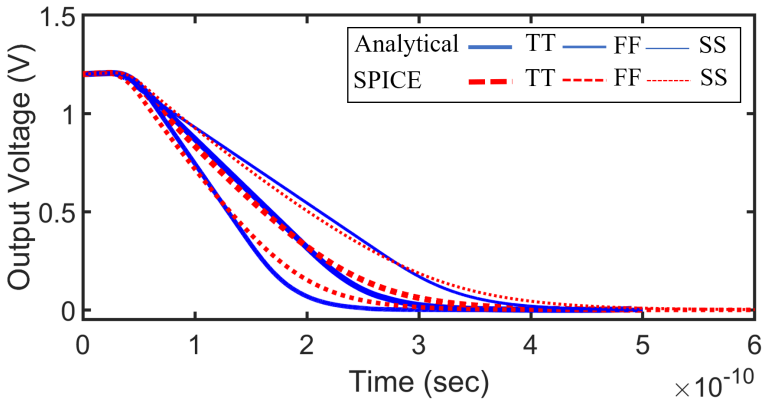


Figure 2.2.3: Output responses obtained at different corner simulations.

2.2.2 Modeling of Jitter

This section presents a mathematical modeling of the instantaneous shift in the transition edge of the output signal at $V_{DD}/2$ by considering all the deterministic noise sources. During the low-to-high transition of the fast-rising input signal, the output of the inverter transits from level-high to level-low state. During this transition state, at the midpoint of falling transition edge of the output signal (Region-IV in Figure 2.2.2), the transistor M_p operates in cutoff mode while the M_n transistor operates in saturation mode; therefore, the instantaneous noise from the ground will directly appear at the output at this point, which is directly reflected in (2.49). The effect of supply and data noise is transported from Region-I to all the successive regions through the constants V_{12}, V_{23}, and V_{34} (as all the successive regions are interlinked to the previous one). Hence, the noise from the supply, data, and ground terminal will be reflected in terms of jitter in the output response of the inverter. The output expression (2.49) is a polynomial that is a function of time. Due to the presence of various noise sources, the intercept of this polynomial at the mid-point (i.e., at $V_{DD}/2$) shifts in time for every falling edge. Therefore, the jitter estimation must be done at the mid-point of the output transition edge.

Until this point, the output expressions of the inverter for each region have been derived considering a constant value of phase (ϕ_{s_n}, ϕ_{x_n} and ϕ_{g_n}) for all the noise sources for a single output transition edge. These were the initial phase constants of all the noise sources PSN, DN, and GBN, respectively, at the initial stage when $V_{in}(t)$ started rising from 0. Depending upon the time period (T_d) of the input data signal, these initial phases would change from one transition edge to the next one. Hence, each transition edge will have a different phase value. Suppose, if $\phi_{s_{n_j}}$, $\phi_{x_{n_j}}$, and $\phi_{g_{n_j}}$ are the phase values for j^{th} transition edge with respect to PSN, DN, and GBN respectively, these values can be written as:

$$\begin{aligned}
\phi_{s_{n_j}} &= \phi_{s_n} + \omega_{s_n} T_d (j-1), \\
\phi_{x_{n_j}} &= \phi_{x_n} + \omega_{x_n} T_d (j-1), \\
\phi_{g_{n_j}} &= \phi_{g_n} + \omega_{g_n} T_d (j-1),
\end{aligned} \tag{2.57}$$

where ϕ_{s_n}, ϕ_{x_n}, and ϕ_{g_n} are the initial phase constants of noise sources PSN, DN, and GBN, respectively. And $\phi_{s_{n_j}}$, $\phi_{x_{n_j}}$ and $\phi_{g_{n_j}}$ are the instantaneous phase values corresponding to j^{th} transition edge with respect to PSN, DN, and GBN, respectively.

As (2.49) is a polynomial of $(k+1)^{\text{th}}$ order, the solution of it will have $(k+1)$ roots (corre-

sponding to the midpoint of each transition edge, i.e., at $V_{out} = V_{DD}/2$). The real root that falls within the temporal span of this region will be the most significant root of this polynomial. Thus, from equation (2.49), the midpoint of jth edge is denoted as t_j, and it is a function of the many parameters as given by:

$$t_j = F(\gamma, \eta, \zeta, \psi, \sigma, V_{DD}, V_{TN}, V_{TP}, \omega_{s_n}, \omega_{x_n}, \omega_{g_n}, A_{s_n}, A_{x_n}, A_{g_n}, \phi_{s_{n_j}}, \phi_{x_{n_j}}, \phi_{g_{n_j}}) \tag{2.58}$$

Deviation in time instance of a midpoint from the ideal edge (i.e., when there is no noise) will determine the time interval error (TIE). TIE expression of jth edge with respect to the ideal edge can be represented as:

$$TIE_j = t_j - T_0 \tag{2.59}$$

where T_0 is the time instance at the midpoint of the ideal edge (when $A = 0$). The jitter at the output is determined by the difference between the maximum and the minimum value of TIE and is stated as:

$$Jitter = \max(TIE)) - \min(TIE)). \tag{2.60}$$

Thus, (2.60) can be used to estimate the jitter analytically.

Table 2.2.1: Timing Deviation with respect to noise.

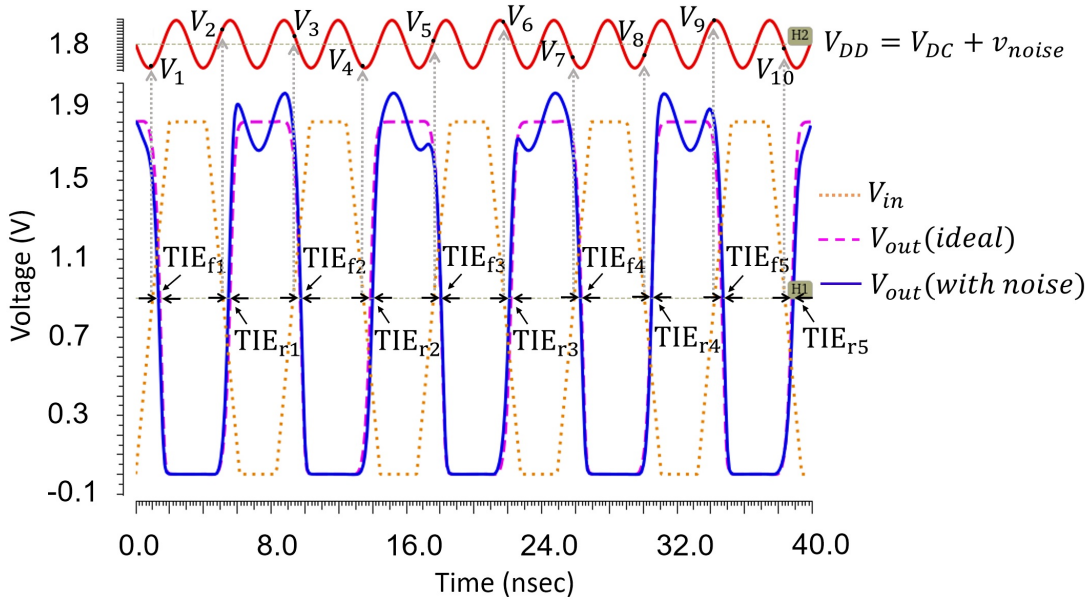
PSN is not in Harmonic with input data				PSN is in Harmonic with input data			
Supply Voltage (Volt)		Time Interval Error (psec)		Supply Voltage (Volt)		Time Interval Error (psec)	
V_1	1.6616	TIE_{f1}	-80.0180	V_1	1.6971	TIE_{f1}	-59.122
V_2	1.8993	TIE_{r1}	-91.8550	V_2	1.9028	TIE_{r1}	-88.8158
V_3	1.8746	TIE_{f2}	-32.7549	V_3	1.6971	TIE_{f2}	-59.122
V_4	1.6528	TIE_{r2}	116.3023	V_4	1.9028	TIE_{r2}	-88.8158
V_5	1.8200	TIE_{f3}	22.3416	V_5	1.6971	TIE_{f3}	-59.122
V_6	1.9343	TIE_{r3}	-93.00	V_6	1.9028	TIE_{r3}	-88.8158
V_7	1.6936	TIE_{f4}	-53.0566	V_7	1.6971	TIE_{f4}	-59.122
V_8	1.7340	TIE_{r4}	-9.0626	V_8	1.9028	TIE_{r4}	-88.8158
V_9	1.9488	TIE_{f5}	84.6431	V_9	1.6971	TIE_{f5}	-59.122
V_{10}	1.7703	TIE_{r5}	72.5120	V_{10}	1.9028	TIE_{r5}	-88.8158

Observations:

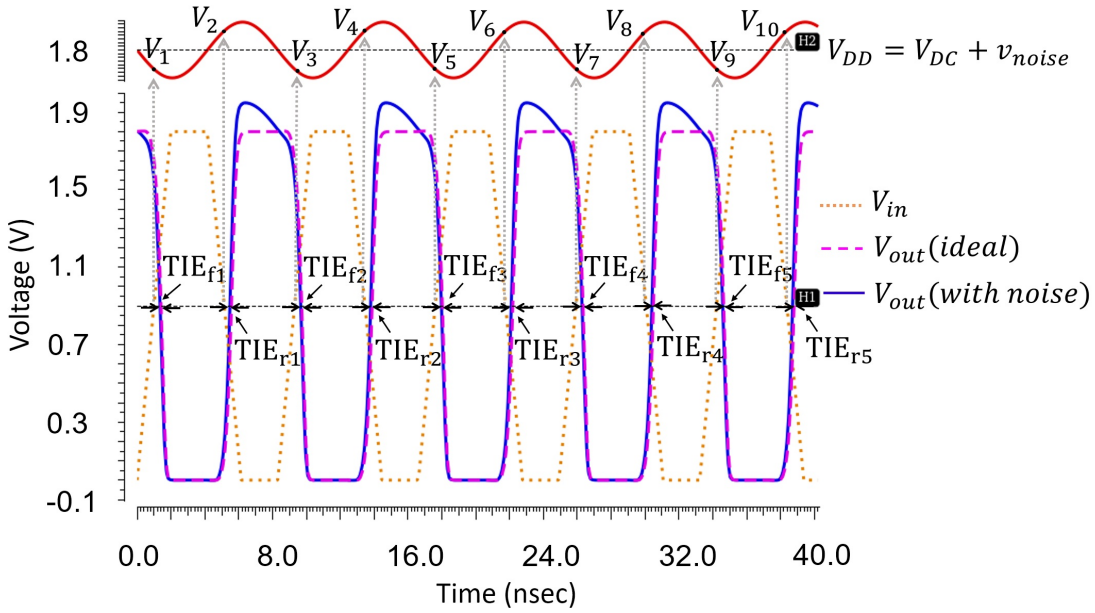
Since the proposed model uses device parameters, these are obtained from the process design kit (PDF) file for a particular technology node provided by the foundry; it would work for all the frequencies, depending upon the technology nodes. Let us do some analysis using equation (2.57), assuming that only PNS is present in the circuit and there are no DN, GBN, or random noise sources present in the circuit. It can be observed that to determine the instantaneous phase constant (ϕ_{n_j}), the time period ($T_d = 1/f_d$) of input data is multiplied with noise frequency ω_n, which can be written as:

$$\phi_{n_j} = \phi_n + \omega_n \cdot \frac{2\pi}{f_d} \cdot (j-1). \tag{2.61}$$

This expression highlights the direct dependence of the instantaneous phase constant on both the data frequency and the noise frequency, providing critical insights into how PSN affects timing in the circuit. Therefore, if noise frequency is in harmonic with the input data frequency,



(a)



(b)

Figure 2.2.4: Timing Deviation with respect to noise (a) PSN is not in harmonic with input data and (b) PSN is in harmonic with input data.

the equation (2.57) can be modified as:

$$\phi_{n_j} = \phi_n + 2\pi(j-1). \tag{2.62}$$

From (2.62), since $(j-1)$ is an integer value, the initial phase constant (ϕ_n) gets added with 2π time some integer value. Therefore, the instantaneous phase constant (ϕ_{n_j}) for j^{th} transition edges will always remain the same, i.e., the net phase shift for each transition edge will be the same. Therefore, each transition edge will be deviated by the same amount depending on the initial phase constant of noise, i.e., each transition edge will experience the same time interval error. Thus, if the noise frequency is in harmonic with the input data frequency, jitter (i.e., peak-to-peak timing deviation) at the output will be zero. This occurs because the periodicity of the noise aligns with the input data, leading to consistent and uniform phase shifts across all transition edges and eliminating any timing variations (i.e., the effective timing deviation for each transition edge is zero).

The above-discussed observations can be visualized using simulation results. An inverter circuit is designed at 180 nm UMC technology node. A small signal, single-tone sinusoidal noise source with an amplitude of 150 mV is inserted at the supply terminal. The input data having fundamental frequency of 120 MHz (i.e., the data rate is 240 Mbps) is considered and applied at the input terminal. Here, two different cases are considered. For Case-A, PSN is not in harmonic with the input data signal (noise frequency is 317 MHz and input data frequency 120 MHz). The input-output plot and the PSN source are shown in Figure 2.2.4(a). From the figure, it can be seen that every rising/falling transition edge is getting a different supply voltage. Therefore, the timing deviation experienced by each transition edge will be different. For Case-B, PSN is in harmonics with the input data signal (noise frequency is 120 MHz and input data frequency is also 120 MHz). The input-output plot and the PSN source are shown in Figure 2.2.4(b). From the figure, it can be seen that every rising transition edge of the input data is getting the same supply voltages, and so are falling transition edges. Therefore, the timing deviation experienced by a similar transition edge will be the same, i.e., it will be the same for all the rising edges and same for all the falling edges.

The corresponding instantaneous supply voltage corresponding to the midpoint of each transition edge of the input signal and the associated timing deviations for each transition edge of the output response are summarized in Table 2.2.1. These results clearly validate the theoretical observations and highlight how the harmonic relationship between noise and input data frequency impacts the timing deviation and jitter.

2.3 Results and Discussion

This section compares and validates the result obtained from the proposed analytical approach with the simulation results obtained using the SPICE-based simulator and with the measurement results using the hex inverter ICs. The various aspects of PSN, DN, and GBN are discussed by considering several numerical examples. Here, the noise coming from all three terminals (supply, data, and ground) can directly affect the transition edge of the output significantly. Therefore, it will encounter the worst-case shift to the output transition edge. Thus, it becomes necessary to perform the jitter analysis by including the effect of instantaneous fluctuation on these terminals. Therefore, to estimate jitter at the output, a test setup considering a multi-tone noise is prepared for the case of SPICE simulation and a single-tone noise source for the case of experimental results. This will mimic the effect of fluctuations of simultaneous switching noise at all three terminals. The results obtained from this analysis are compared with the simulations as well

as measurement results for a given technology node and hex inverter IC parameters, respectively. The comparison of analytical results with simulation and measurement results are presented in the following Sections-2.3.1 and Sections-2.3.2, respectively.

2.3.1 Comparison of Analytical Results with SPICE-based Simulation results

Since the proposed method relies on the device parameters. Therefore, the device parameters for different technology nodes are obtained from the process design kit (PDK) file from the United Microelectronics Corporation (UMC), as given in Table 2.3.1.

Table 2.3.1: Device Parameters used for Transistors

Technology Node (UMC)	40 nm	65 nm	180 nm
$V_{DD}\ (V)$	1.2	1.2	1.8
$\beta_p\ (mA/V^2)$	0.276698	0.757034	16.15
$\beta_n\ (mA/V^2)$	0.416052	0.641519	15.89
$C_{gd_p}\ (fF)$	0.0553191	0.115342	9.559
$C_{gd_n}\ (fF)$	0.054741	0.0973468	4.058
$V_{TP}\ (mV)$	-379.755	-272.852	-504.5
$V_{TN}\ (mV)$	431.979	470.952	490.8

Example-1:

In this example, the output transition edge is shown in the presence of ground-bounce noise. The output jitter has been calculated from the deviation of these transition edges. Here, 40 nm UMC technology node is considered to design the inverter, and the load capacitance of 10 fF is considered. First, the output response is obtained in the absence of noise in the circuit, and the falling edge of the output waveform is appended for every time period as shown in Figure 2.3.1(a). Here, the deviations in the transition edges of the output response are zero (i.e., no jitter at the output).

Next, a single-tone sinusoidal noise source with frequency of 133 MHz and amplitude of 40 mV is inserted at the ground terminal. Figure 2.3.1(b) shows the appended output response in the presence of GBN. From the figure, significant deviations in the falling edges of the output response can be seen as shown in Figure 2.3.1(b). With the noise, the obtained jitter from the analytical approach and simulation is 20.27 psec and 18.02 psec, respectively.

Example-2:

In this experiment, three different case studies are presented, considering different technology nodes.

Case-A: In this case, the CMOS inverter circuit is designed using a 40 nm UMC technology node having a power supply of 1.2 V and a load capacitance of 10 fF. Here, single-tone noise sources having frequency 133 MHz and initial phase constant 0 degree are connected at the ground terminals of the inverter.

Case-B: In this case, the CMOS inverter circuit was designed in a 65 nm UMC technology node having a power supply of 1.2 V and a load capacitance of 10 fF. Here, three single-tone noise sources having their frequencies and phase values as {537 MHz, 60°}, {133 MHz, 40°}, and {409 MHz, 0°} are applied at the supply and data and ground terminals of the inverter, respectively.

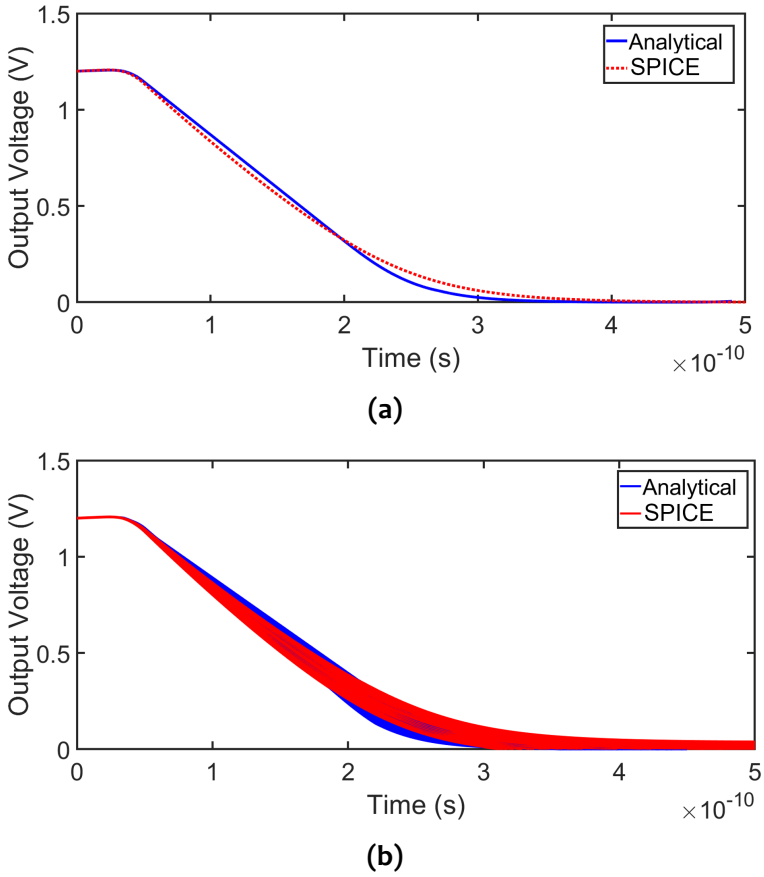


Figure 2.3.1: Appended waveform of the Output falling edge (a) without noise and (b) in the presence of GBN.

Case-C: The CMOS inverter circuit is designed in a 180 nm UMC technology node having a power supply of 1.8 V and a load capacitance of 1 pF. Here also, three single-tone noise sources having their frequencies and phase values as {409 MHz, 0°}, {133 MHz, 40°}, and {710 MHz, 60°} are applied at the supply and data and ground terminals of the inverter, respectively.

For all three cases, 100 bits of input data of time period $T_d = 4.16$ nsec are considered. The amplitude of all noise sources is varied, and the corresponding jitter values are obtained and compared with the results obtained from SPICE-based simulator as shown in Figure 2.3.2(a), Figure 2.3.2(b) and Figure 2.3.2(c), respectively.

Example-3:

This experiment has been done by considering two cases. This example also validates the previously discussed observations done based on equation (2.57). Two cases are considered in this example.

Case-A: The inverter circuit is designed using 40 nm UMC technology node, a single-tone sinusoidal noise source having a peak-to-peak amplitude of 40 mV is applied at the input data terminal of the inverter having supply voltage of $V_{DD} = 1.2$ V, and load capacitance of 5 fF. And, 100 bits of input data of time period $T_d = 4.16$ nsec has been taken. The experiment is done by varying the noise frequency from 15 MHz to 720 MHz, and the corresponding jitter value is ob-

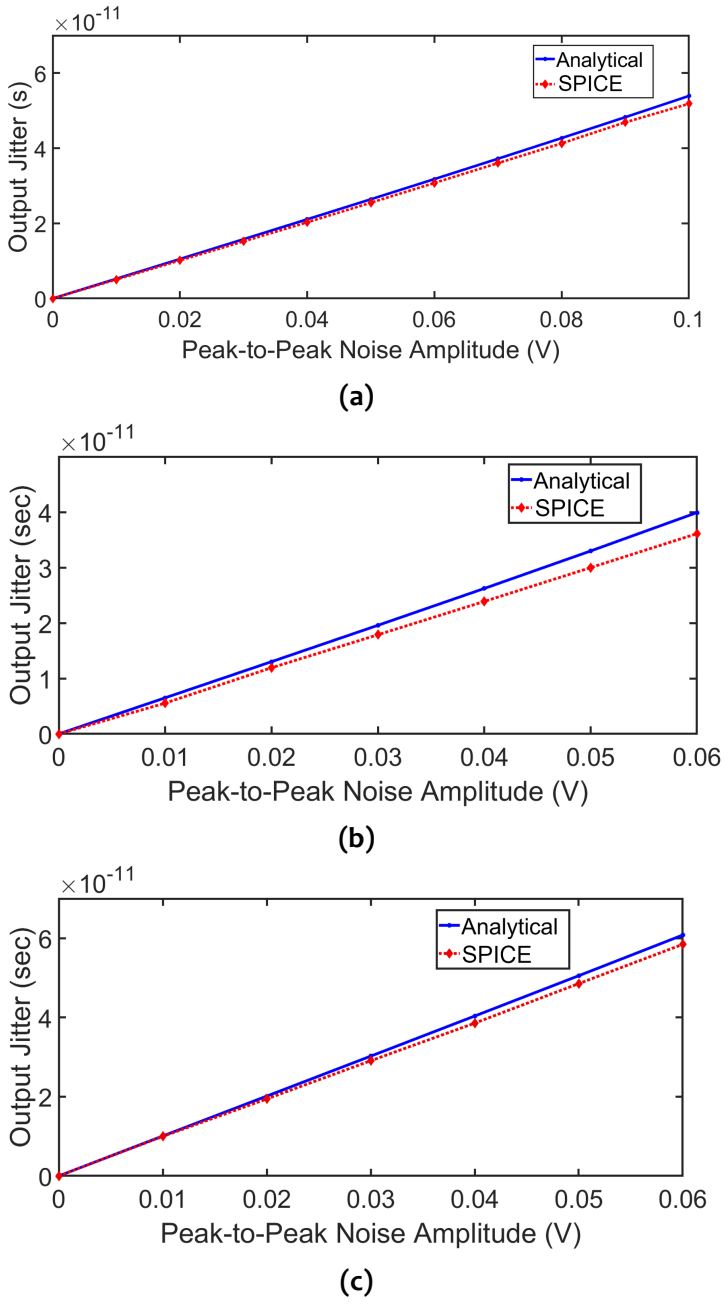


Figure 2.3.2: Output Jitter obtained from analytical approach and from SPICE-based simulation in (a) UMC 40 nm, (b) UMC 65 nm, and (c) 180 nm technology.

served. Figure 2.3.3(a) depicts the plot of the results obtained from the analytical approach and the same obtained from the simulations using a SPICE-based tool.

Case-B: The inverter circuit is designed using 65 nm UMC technology node, a single-tone sinusoidal noise source having peak-to-peak amplitude of 30 mV is applied at the input data terminal of the Inverter having supply voltage of ($V_{DD} = 1.2$ V), and load capacitance of 1 fF. And, 100 bits of input data with the time period $T_d = 4.16$ nsec is taken. The experiment is done by varying the noise frequency from 15 MHz to 720 MHz, and the corresponding jitter value is observed. Figure 2.3.3(b) depicts the plot of the results obtained from the analytical approach and

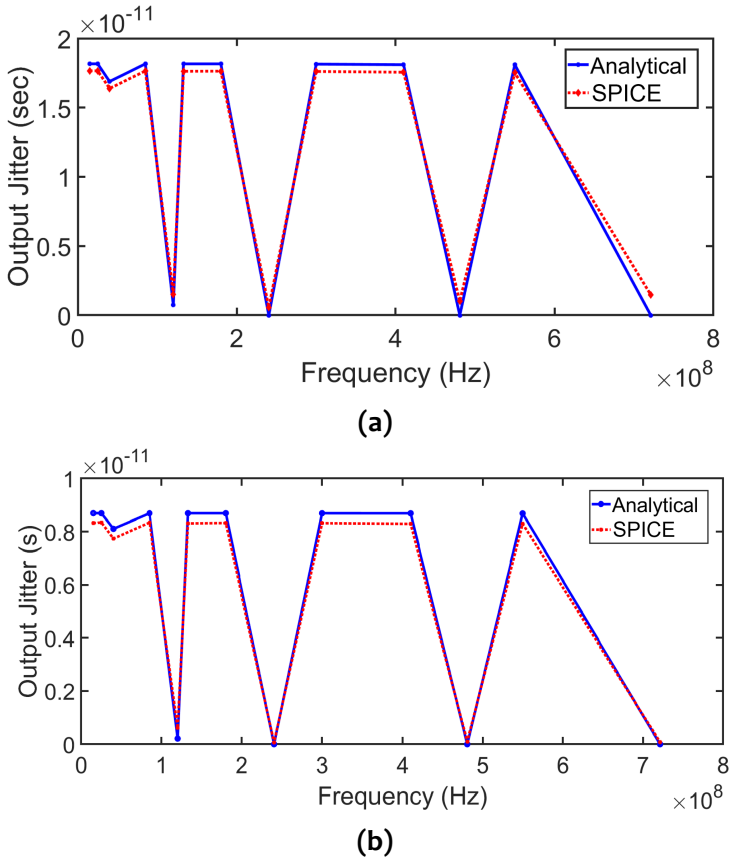


Figure 2.3.3: Output jitter with respect to noise frequency variation considering (a) 40 nm and (b) 65 nm UMC technology nodes.

the same obtained from the simulations in an SPICE-based tool.

From both figures, it can be observed that the frequency, which is an integer multiple of input data frequency, does not provide extra shift to the output transition edge. Such noise frequency gives nearly 0 psec of jitter, as shown in the Figure 2.3.3. The frequency other than harmonic frequency shows a finite amount of jitter greater than 0 psec.

Example-4:

In this experiment, TIE expression (2.59) is validated. Here, two case studies are considered, taking two different CMOS technology nodes; for *Case-A*, the inverter circuit is designed at a 40 nm UMC technology node, and for *Case-B*, at a 65 nm UMC technology node. For both the cases, the load capacitance of 10 fF and supply voltage $V_{DD} = 1.2$ V are considered.

Case-A: First, a single-tone noise source with a frequency of 710 MHz and amplitude of 40 mV is inserted at the ground terminal. The TIE plot is obtained for every transition edge of the output, as shown in Figure 2.3.4(a). The peak-to-peak amplitude of the curve measured represents jitter at the output, and its value is 20.27 psec from the proposed analytical method and 19.38 psec from the simulations. Next, a multi-tone noise source having three sinusoidal components with the amplitude, frequency and initial phase value of {5 mV, 136 MHz, 0°}, {20 mV, 409 MHz, 20°}, and {35 mV, 710 MHz, 40°} is considered at the ground terminal. The TIE plot is shown in Figure 2.3.4(b). The estimated jitter values are 31.26 psec and 31.11 pesc, from the proposed

analytical and SPICE-based simulation methods, respectively.

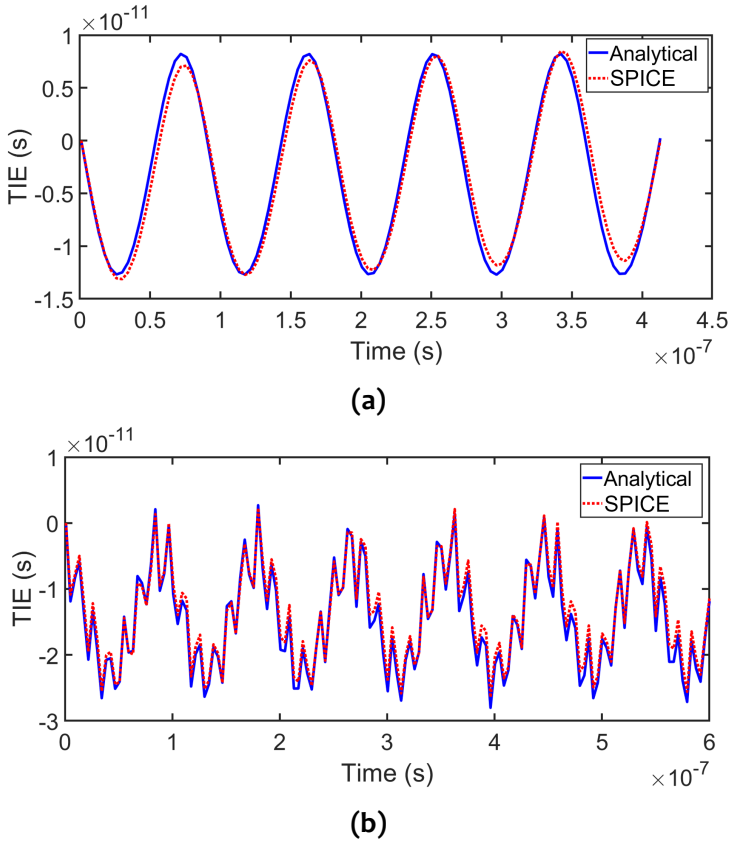


Figure 2.3.4: TIE at the output of inverter (a) single-tone and (b) multi-tone noise (both in 40 nm UMC technology node).

Case-B: First, a single-tone noise having a frequency of 710 MHz and an amplitude of 40 mV is considered at the data terminal. The TIE plot for every transition edge of the output is shown in Figure 2.3.5(a). The peak-to-peak amplitude of the curve is calculated, which represents the jitter at the output, and its value is 8.68 psec from the proposed method and 8.32 psec from the SPICE-based simulation. Next, a multi-tone noise source having three sinusoidal components with amplitude, frequency and initial phase of {10 mV, 409 MHz, 40°}, {20 mV, 133 MHz, 0°}, and {30 mV, 737 MHz, 60°} is considered at data terminal. The timing deviation is shown in plot Figure 2.3.5(b). The estimated jitter values using the proposed analytical and simulation techniques are 15.70 psec and 13.97 pesc, respectively.

Thus, from these TIE plots, it is clear that the proposed analytical method is in agreement with the SPICE-based simulation results.

Example-5:

In this example, the results of Monte Carlo (MC) simulations have been obtained considering the channel widths (W_p and W_n) of the transistors as random variables. The results obtained from the proposed analytical model and from the SPICE-based simulator are compared. The inverter circuit is designed using 40 nm UMC technology and a load of 10 fF, $V_{DD} = 1.2$ V, and 100 bits of input data having $T_d = 4.16$ nsec are considered. Here, two different cases are considered to

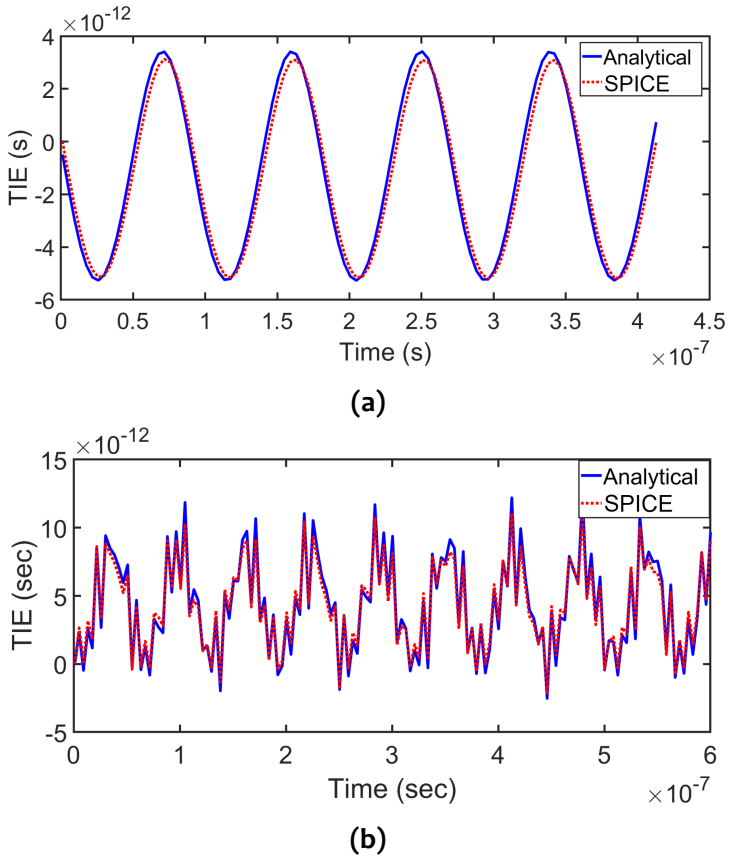


Figure 2.3.5: TIE at the output of inverter (a) single-tone and (b) multi-tone noise (both in 65 nm UMC technology node).

demonstrate the numerical example.

Case-A: A sinusoidal noise having peak-to-peak amplitude of 40 mV and frequency of 133 MHz is inserted at the ground terminal, and 2000 Jitter samples are obtained. Figure 2.3.6 shows the histograms of the results obtained by both methods. The comparison of the results is given in Table 2.3.2. The results obtained from both methods are in close consonance with the error of 3.68%.

Table 2.3.2: Comparison of MC simulation results for GBN

Parameters	Simulation	Analytical
Mean (μ) in sec	20.227×10^{-12}	20.972×10^{-12}
Standard Deviation (σ) in sec	2.2261×10^{-13}	4.2909×10^{-13}
CPU time in hours	12.25	3.11

Case-B: Three different noise sources having their amplitude, frequency, and phase values respectively as {30 mV, 537 MHz, and 60°}, {30 mV, 409 MHz, and 15°}, and {30 mV, 133 MHz, and 40°}, are connected at the power supply, data, and ground terminal, respectively. The jitter estimation is done by considering all the noise sources and the results are compared in Figure 2.3.7. Table 2.3.3 compares the statistical parameters obtained from both the methods. The results obtained from both methods match closely with each other, with an error of 9.72%.

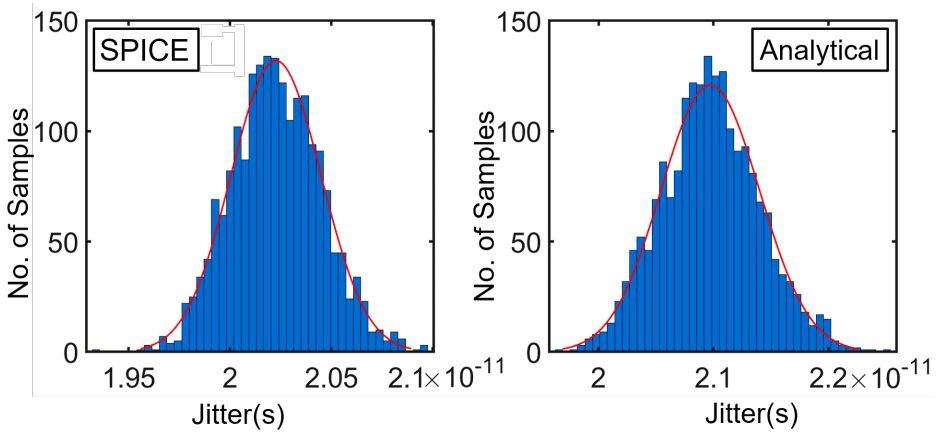


Figure 2.3.6: Monte Carlo (MC) simulation results obtained using SPICE base simulator and MATLAB for GBN.

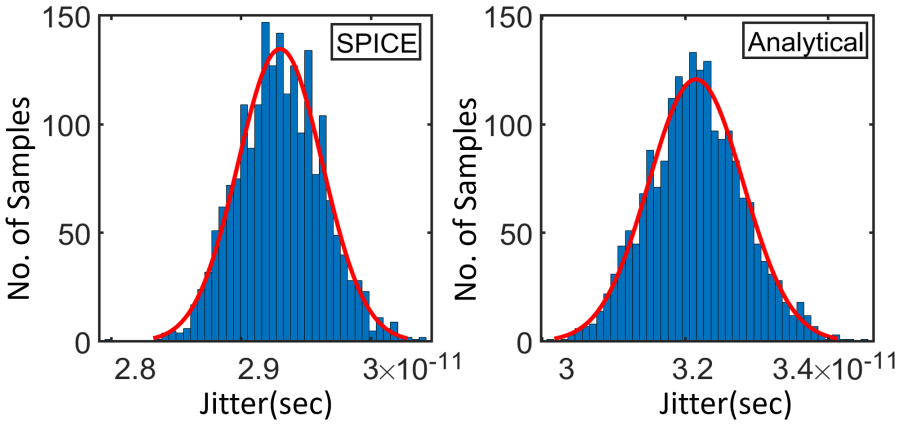


Figure 2.3.7: Monte Carlo (MC) simulation results obtained using SPICE base simulator and MATLAB for PSN, DN, and GBN.

Table 2.3.3: Comparison of MC simulation results for PSN, DN, and GBN.

Parameters	SPICE	Analytical
Mean (μ) in sec	29.30×10^{-12}	32.15×10^{-12}
Standard Deviation (σ) in sec	3.26×10^{-13}	6.61×10^{-13}
CPU time in hours	14.47	3.41

Example-6:

In this example, the inverter circuit is designed in 40 nm UMC technology node. All three noise sources are considered. The amplitude, frequency, and phase of supply and ground noise are kept the same and constant, and these are as 12 mV, 409 MHz, and 0°, respectively, for both the noise sources. Keeping the amplitude and frequency for the data noise constant to 12 mV and 409 MHz, respectively, its phase value is varied from 0° to 180°. The corresponding jitter value is estimated, and a comparison has been made between the analytical and SPICE-based results in Figure 2.3.8.

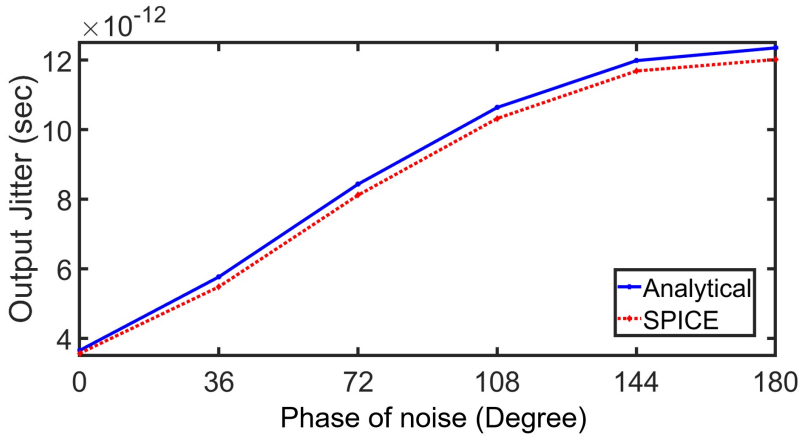


Figure 2.3.8: Jitter at various phase values of data noise keeping amplitude and frequency constant.

2.3.2 Comparison of Analytical Results with Measurements

In this section, the results obtained from the analytical expressions derived in the previous section are compared with the measurement results. Similar to Section-2.3.1, there are several diverse examples presented in this section also. The experiments are performed using two hex inverter ICs (M74HC04 and MC74AC04N), considering two different experimental setups, respectively. Here the required parameters to perform the analytical simulation are obtained from measurement with the help of data sheets provided by the IC manufacturers. The device parameters for the inverter ICs are given in Table 2.3.4.

Experimental Setup-I:

In this setup, a hex inverter IC M74HC04 (STMicroelectronics), one Oscilloscope (MSOX4054A 500 MHz 5 GSa/s), two function generators (Aplab DDS300 300 MHz dual channel, and Tektronix AFG3021B 25 MHz single channel), one regulated DC supply, one breadboard and some connecting probes are used. For the experiments, a 5 V DC supply is applied at the V_{DD} terminal of inverter IC and a square wave having amplitude of 5 V peak-to-peak and time period $T_d = 0.667$ μsec at the input terminal. A load capacitance of 100 pF is connected at the output. Figure 2.3.9 shows an

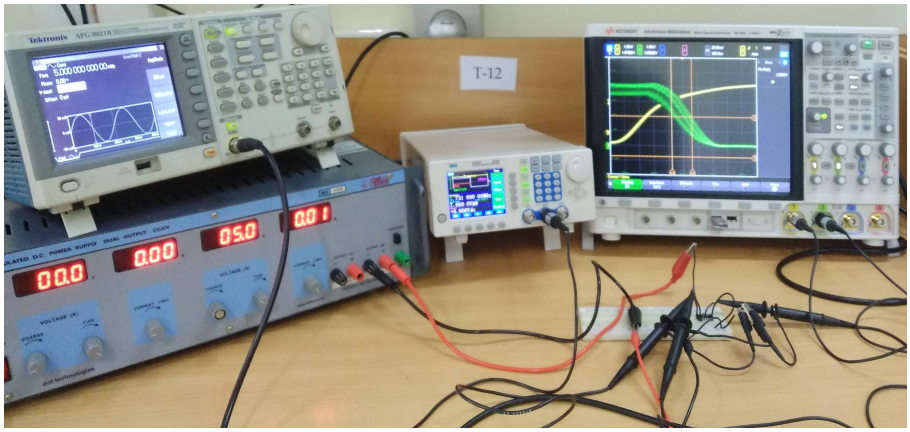


Figure 2.3.9: Experimental Setup-I.

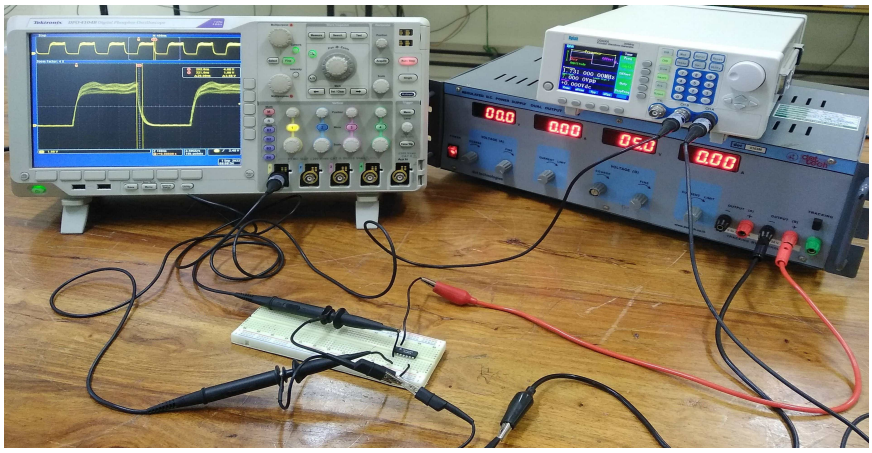


Figure 2.3.10: Experimental Setup-II.

image of the experimental setup. Further, jitter is measured at the first inverter stage of the IC.

Experimental Setup-II:

This setup uses a hex inverter IC (MC74AC04N) from On Semiconductor, one function waveform generator (DDS300 300 MHz) from Aplab, a Digital Phosphor Oscilloscope (DPO4104B 1 GHz) from Tektronix, one breadboard, and some connecting probes and wires. For the experiment, a 5 V DC supply is applied at the V_{DD} terminal of inverter IC and a square wave having amplitude of 5 V peak-to-peak and time period $T_d = 0.578$ μsec at the input terminal. A load capacitance of 100 pF is connected to the output. Further, jitter is measured at the first inverter stage of the IC. The experimental setup is shown in Figure 2.3.10.

In both the experimental setups, the small-signal noise was generated using these two function generators (either using Aplab or Tektronix or both). The output impedance was set to 50 Ω when it was connected to generate small signal noise, whereas while feeding input data signal, its output impedance was kept Hi-Z (i.e., approximately equal to 1 MΩ). Now, based on these two setups, five different examples are provided.

Table 2.3.4: Device Parameters used for Hex Inverter ICs.

Technology Node (UMC)	M74HC04B1R	MC74AC04N
β_p (mA/V^2)	2.78	2.67
β_n (mA/V^2)	6.36	6.12
$(C_{gd_p} + C_{gd_n})$ (pF)	5.52	4.5
V_{TP} (V)	-1.45	-1.32
V_{TN} (V)	1.68	1.54

Example-7:

From Setup-I, the output results obtained from the analytical method and from the measurement are compared in Figure 2.3.11. The device parameters of the IC are given in Table 2.3.4.

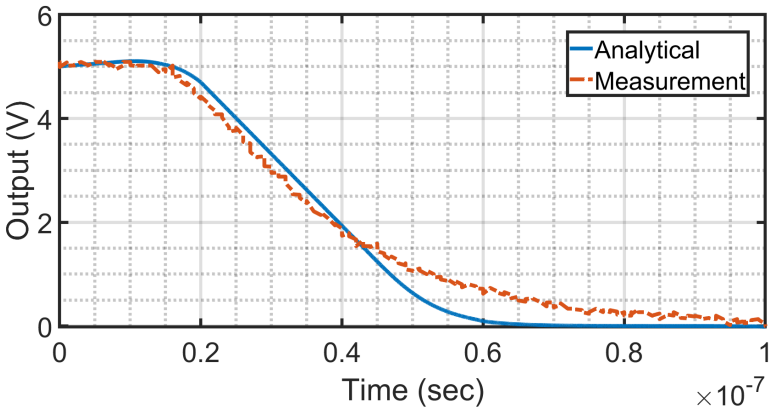


Figure 2.3.11: Output of the Inverter using IC M74HC04.

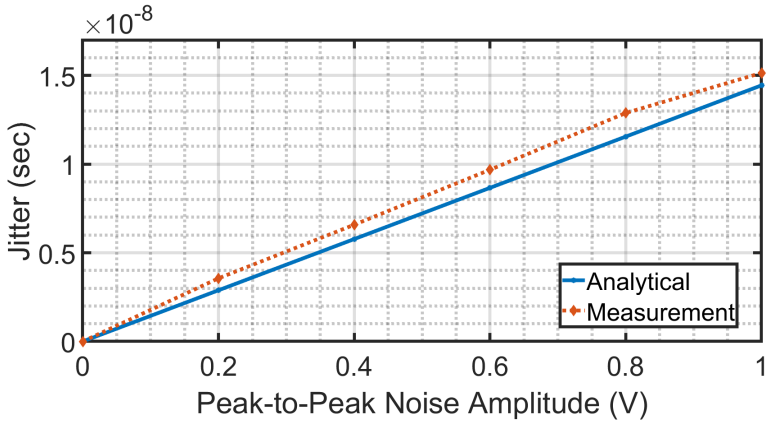


Figure 2.3.12: Jitter at the output with respect to amplitude variation of PSN.

Example-8:

This experiment is based on Setup-I. A noise source having frequency of 5.731 MHz is applied at the power supply terminal, and the peak-to-peak amplitude of the noise source is varied from 0 to 1 V, simultaneously. Based on this, jitter measurement has been done and is compared with the analytical results, as shown in Fig 2.3.12.

Example-9:

The measurement of jitter is done with respect to frequency variations of noise source. This experiment is based on Measurement Setup I. A noise source having peak-to-peak amplitude of 400 mV is applied at the ground terminal of the IC. The frequency of the noise source is varied from 2.321 MHz to 15 MHz. The measured jitter are in close match with jitter obtained from the analysis, as shown in Figure 2.3.13.

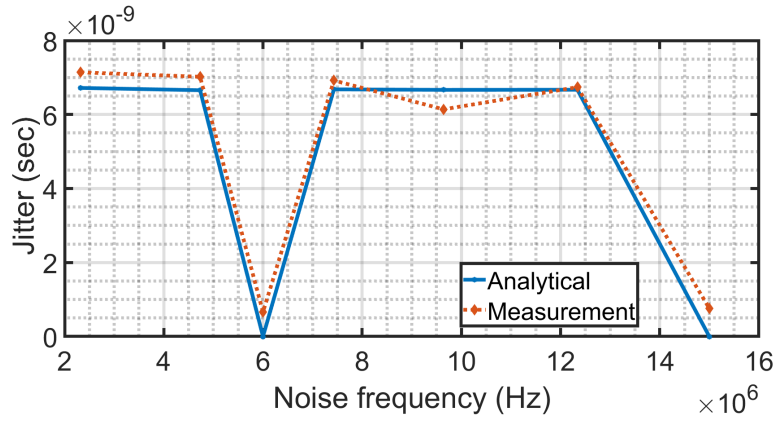


Figure 2.3.13: Jitter at the output with respect to frequency variation of GBN.

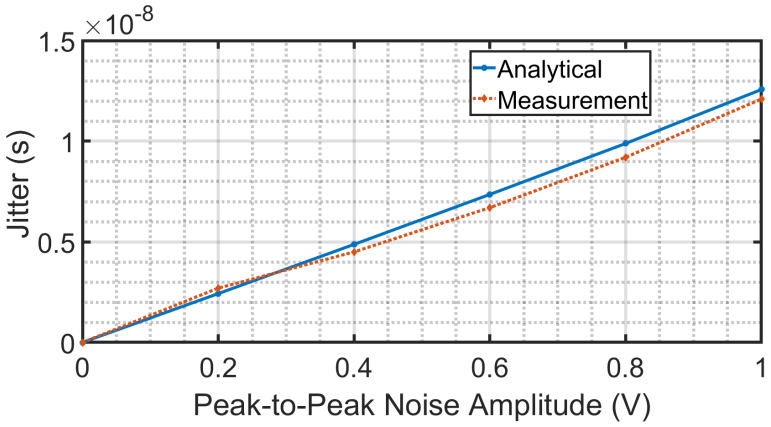


Figure 2.3.14: Jitter at the output with respect to peak-to-peak amplitude variation of GBN.

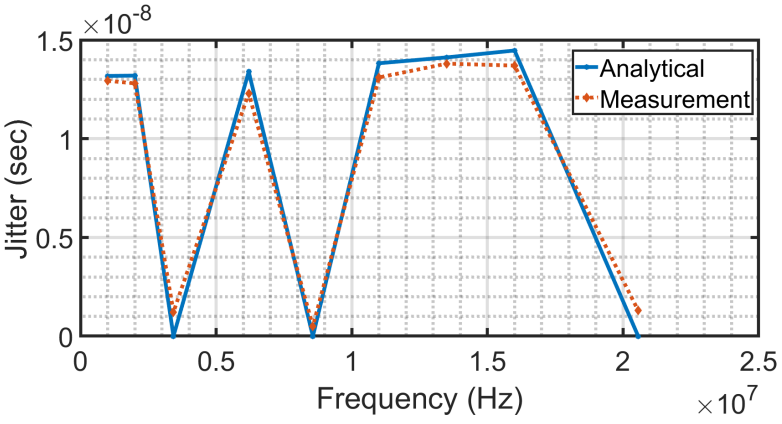


Figure 2.3.15: Jitter at the output with respect to frequency variation of PSN.

Example-10:

This experiment is performed over Setup-II with respect to amplitude variation of GBN from 0 to 1 V keeping the frequency constant at 5 MHz. The measured jitter values are compared with the

jitter values from analytical method as shown in Figure 2.3.14.

Example-11:

This experiment is based on Setup-II, and the frequency of PSN is varied from 1 MHz to 22 MHz, keeping the peak-to-peak amplitude constant at 1 V. An square wave with time period $T_d = 0.578$ μsec is applied at the input pin. The comparative plot of measurement result with the analytical results is shown in Figure 2.3.15.

2.4 Summary

A comprehensive analytical approach to model deterministic jitter at the output of CMOS inverters, considering various noise sources such as power supply noise (PSN), ground-bounce noise (GBN), and data noise (DN). The estimation of jitter is performed by calculating the peak-to-peak deviation in the transition edge of the output of the inverter, taking into account the impact of each noise source individually as well as in combination. To ensure the robustness and applicability of the proposed analytical model, the results are validated through a series of simulations and measurement results using multiple CMOS technology nodes, including 40 nm, 65 nm, and 180 nm, as well as measurement setups. The results obtained from the proposed analytical model are in strong agreement with those obtained from the SPICE-based simulator measurement setup. These multiple examples demonstrate that the proposed model is independent of various technology nodes and demonstrates its versatility in handling both single-tone and multi-tone noise sources. It makes the proposed model suitable for various operating conditions and noise sources. Overall, this work introduces a reliable and experimentally validated analytical method for estimating deterministic jitter in CMOS circuits. The consistency in results with both simulation and measurement confirms its utility as an effective tool for timing analysis and signal integrity evaluation in high-speed VLSI design.