4
Semi-Analytical Modeling of Deterministic Jitter

In Chapter 2 and Chapter 3, a detailed study of mathematical modeling of deterministic jitter and variability-aware modeling of deterministic jitter has been done, respectively, which considers an analytical modeling approach to estimate timing deviations in the transition edges of the output response. These chapters consider the CMOS inverter as a case study. However, the analytical modeling is not always viable option keeping in mind the complexity of circuits. This chapter presents a semi-analytical approach to estimate power supply-induced jitter (PSIJ). It considers a voltage mode driver (VMD) circuit driving long transmission lines (TLs) as a case study. Given the widespread use of VMDs in various serial communication applications, including D-PHY, MPHY, MIPI, DIGRF, and high-speed serial links like USB, MIPI, etc. [Tripathi *et al.*, 2017], the timing performance of these applications should be very accurate and precise, because of the stringent timing budget. Therefore, providing an accurate analysis of jitter in such drivers is critically important. The proposed approach addresses this need by providing an efficient and computationally less extensive method to estimate PSIJ, which directly impacts the reliability and performance of high-speed communication systems.

4.1 Introduction

A semi-analytical method is employed to estimate jitter at the differential output of the VMD circuit driving a load through long transmission lines. The output response of the VMD circuit is affected by PSN and GBN. In order to derive the noise response, the small-signal and large-signal components of the output response are separated. The proposed methodology considers the system response, both in time and frequency domains, to analyze jitter in the system. Based on the separation of small and large signal output responses and considering the spatial and temporal components of long transmission lines, a small signal noise response of the circuit is obtained. It uses a distributed model approach to model the long transmission lines. The method relies on a slope-based approach to model timing uncertainty, which requires only a one-bit simulation to estimate jitter [Tripathi *et al.*, 2017], [Sartori, 2023]. Using this approach, a significant reduction in computational complexity while maintaining accuracy is achieved, making it a practical solution for jitter estimation in high-speed VLSI circuits.

Several related works are available in the literature that present comprehensive studies on jitter analysis for differential drivers. A semi-analytical method has been introduced in [Tripathi *et al.*, 2017] and [Tripathi *et al.*, 2019b] to estimate the (PSIJ), using only a one-bit simulation. It considers a differential load without considering the impact of the transmission line on the differ-

ential output response. In [Achar and Nakhla, 2001], various high-speed interconnect effects are discussed using distributed modeling of the interconnects. It suggests that various effects of interconnects (such as signal delay, ringing, reflections, distortion, and crosstalk) at high-frequency operation cannot be ignored during the IC design. The work in [Singh *et al.*, 2021] presents the modeling of jitter for voltage-mode driver circuits with long transmission lines when only power supply noise is present in the circuit, which involves modeling of interconnects using a distributed modeling approach.

The specific contribution of this chapter is to model the PSN and GBN-induced jitter for a voltage-mode driver circuit driving a load through long transmission lines. This approach considers both spatial and temporal aspects of the long transmission lines. A semi-analytical method is employed to estimate jitter at the differential output of the VMD, offering an efficient and accurate means to analyze the impact of PSN and GBN on the performance of the VMD circuit.

4.2 Voltage-Mode Driver

This section describes the operation of the Voltage-Mode Driver (VMD) circuit. Figure 4.2.1 illustrates the schematic of a VMD circuit driving long transmission lines. The circuit is designed considering a regulated DC voltage inserted at the supply terminal of the circuit. The nMOS transistors M_1, M_2, M_3, and M_4 constitute an H-bridge driver configuration. This H-bridge network is responsible for differential signaling across the load. At the far-end of the transmission lines TL1 and TL2, an external load resistor (R_L) of 100 Ω is connected for termination. These transmission lines act as differential interconnects/traces and transmit a signal to the load. A regulated voltage of 400 mV is generated at the source terminal of M_0 with the help of a closed loop formed by the op-amp and M_0. It helps to produce the differential voltage of ±300 mV across the terminals DP and DN, representing logic '1' or '0' values, respectively. The H-bridge network has good noise rejection capability due to the use of op-amp at the regulated node. However, the inverter and buffer circuits share the same supply and ground terminals and can insert noise into the system. Both the signal A and B are complementary to each other. Noise at the supply and ground terminal of the inverter and buffer circuits can affect the differential output across the load. This work does not consider the impact of inter-symbol interference and coupling between the transmission lines on the output jitter. It only considers the effect of PSN and GBN in the circuit.

4.3 Estimation of Jitter in VMD Circuit with Distributed Transmission line

In this section, the noise transfer function for a differential output across the load (R_L) of the VMD circuit is derived while taking the distributed model of the transmission lines into account. A small-signal equivalent model of the VMD circuit is used to analyze the impact of PSN and GBN at the differential output, as illustrated in Figure 4.2.2. Due to the simultaneous switching activity of inverter and buffer, only one path {either the current flow through (M2, TL2, R_L, TL1, and M3) or (M1, TL1, R_L, TL2, and M4)} will be active at a point of time. Therefore, to perform the analysis, only one path of the current flow is considered to draw the small-signal equivalent circuit. For simplified analysis, first, the Thévenin equivalent model of the circuit is developed across nodes v_Q and v_P, as shown in Figure 4.3.1. This Thévenin equivalent model is further used to obtain the differential voltage ($v_{DP} - v_{DN}$) across R_L (i.e., v_{diff}). The return paths of transmission lines (TL1 and TL2) are connected at a common ground to avoid the complexity of analysis, and the equation for Thévenin equivalent voltage (v_{th}) and impedance (Z_{th}) are derived across the node v_P and v_Q, considering both noise sources [Tripathi *et al.*, 2019b]. The Thévenin equivalent voltage

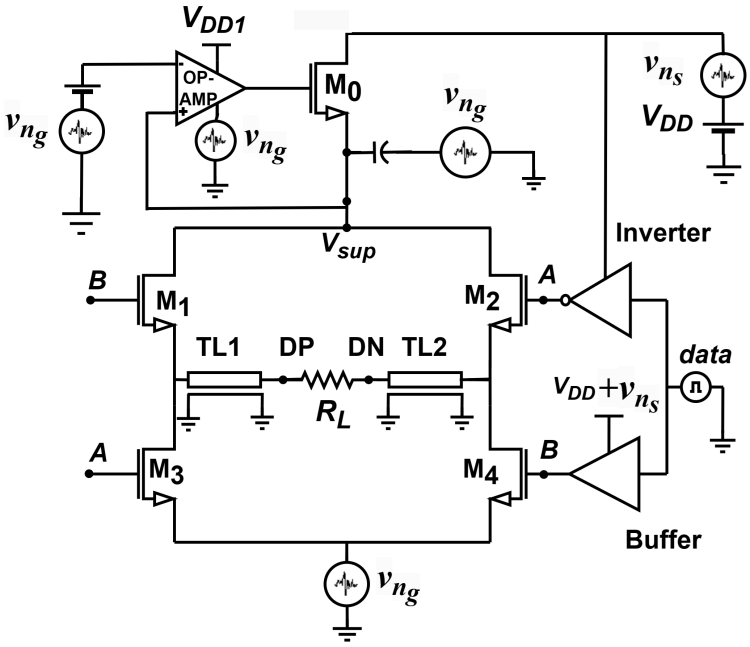

Figure 4.2.1: Voltage-Mode driver driving long transmission line in presence of power supply and ground-bounce noise [Tripathi *et al.*, 2019b].

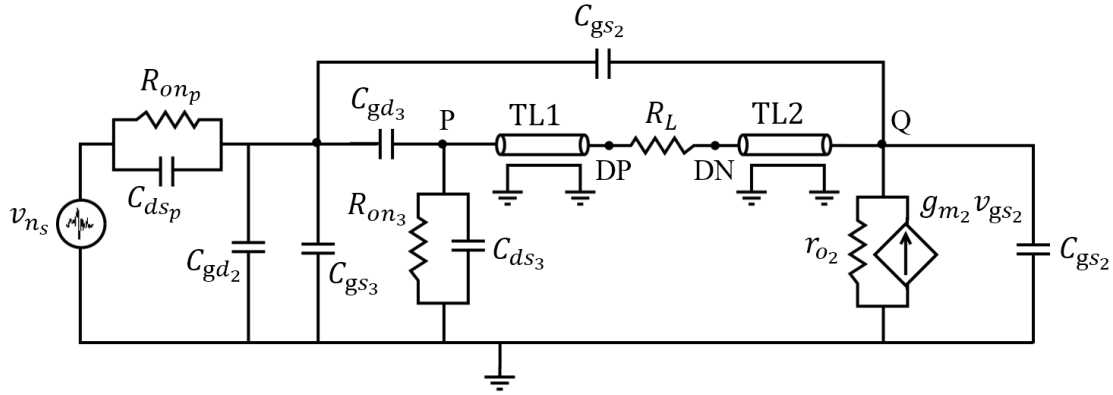

Figure 4.2.2: Small-signal model of voltage mode driver in the presence of power supply and ground-bounce noise with transmission media [Tripathi *et al.*, 2019b].

across the nodes v_P and v_Q can be obtained by estimating the open circuit voltage ($v_{OC} = v_P - v_Q$), the equivalent circuit is shown in Figure 4.3.2. The open circuit voltage can be written as:

$$v_{th} = v_{OC} = \eta_{n_s} v_{n_s} + \eta_{n_g} v_{n_g}, \tag{4.1}$$

where η_{n_s} and ηn_g are the noise transfer functions from noise source to the voltage v_{OC}. The Thévenin equivalent impedance is obtained by estimating short circuit current (i_{SC}) across the nodes v_P and v_Q, the equivalent circuit shown in Figure 4.3.3. The short circuit current (i_{SC}) can be written as:

$$i_{SC} = \gamma_{n_s} v_{n_s} - \gamma_{n_g} v_{n_g} \tag{4.2}$$

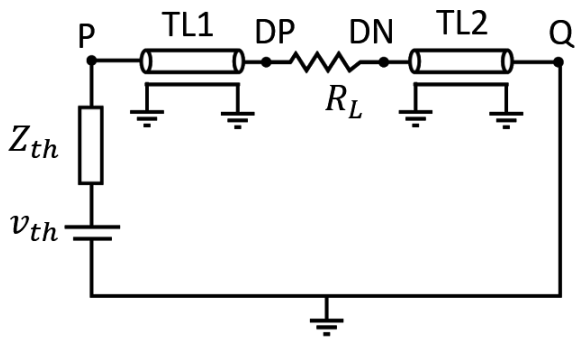

Figure 4.3.1: Thévenin equivalent circuit of Figure 4.2.2.

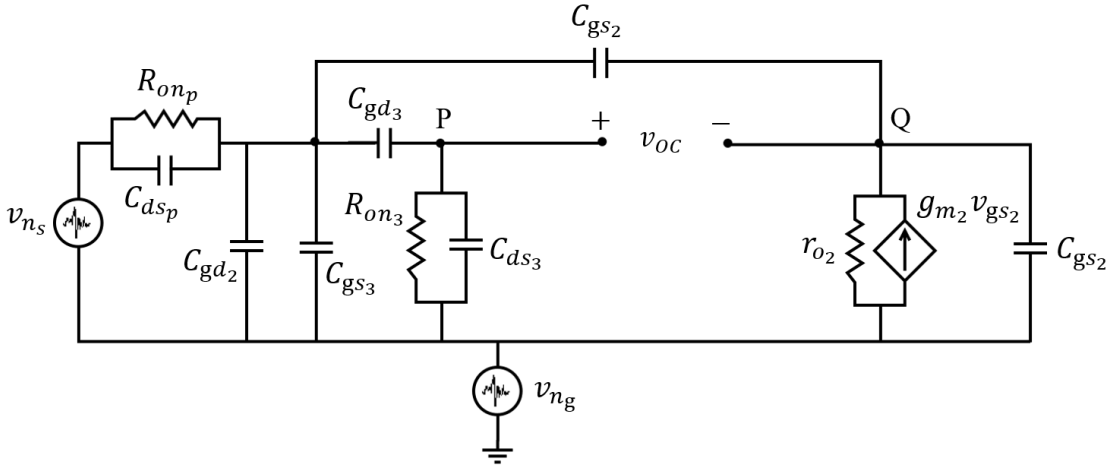

Figure 4.3.2: Equivalent circuit for deriving open circuit voltage across nodes v_P and v_Q.

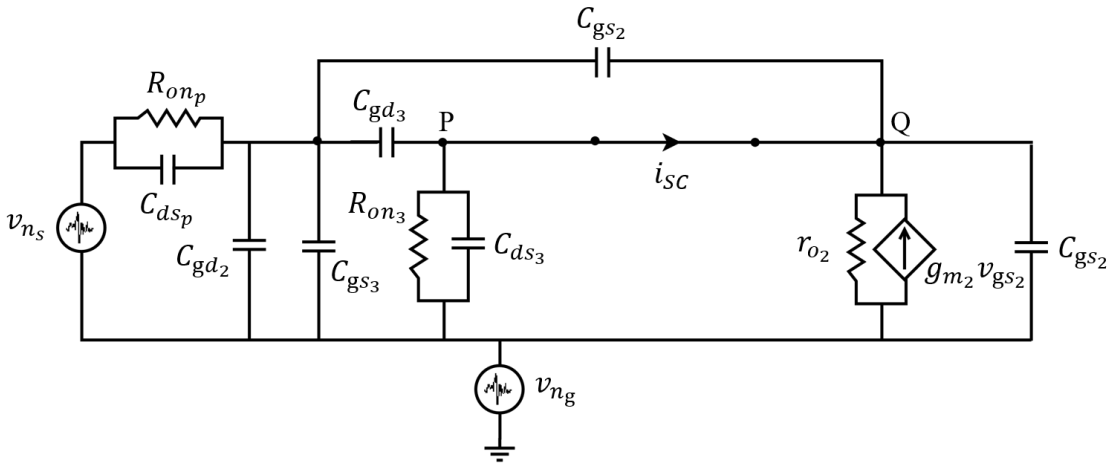

Figure 4.3.3: Equivalent circuit for deriving short circuit current across nodes v_P and v_Q.

Now, the expression for Thévenin equivalent impedance can be written as:

$$Z_{th} = \frac{v_{th}}{i_{SC}} \tag{4.3}$$

4.3.1 Distributed Modeling of Transmission Lines

Telegrapher's equations are used to express the characteristics of a distributed transmission line [Paul, 2011], [Anastasakis *et al.*, 1994]. Assuming that both transmission lines are lossless and identical, and the per-unit length (p.u.l) parameters of both the lines are inductance (L) and capacitance (C). Throughout the length of the line, infinite number of sections of size Δz are assumed [Paul, 2011]. The spatial axis of both lines TL1 and TL2 is z. The return paths of both the lines are grounded at a common node; therefore, they will share a single return path.

Multi-conductor transmission lines (MTL) are transmission lines having a shared/common return path. Here, two transmission lines are connected in series with a termination load resistor R_L in between the lines, both sharing a common return path. Therefore, both lines can be analyzed similarly to the analysis of MTL. The representative equations for MTL [Anastasakis *et al.*, 1994] are:

$$\frac{\partial}{\partial z}\begin{bmatrix} V(z,s) \\ I(z,s) \end{bmatrix} = (D+sE)\begin{bmatrix} V(z,s) \\ I(z,s) \end{bmatrix}, \tag{4.4}$$

where,

$$D = \begin{bmatrix} 0 & -R \\ -G & 0 \end{bmatrix} \qquad \text{and} \qquad E = \begin{bmatrix} 0 & -L \\ -C & 0 \end{bmatrix}. \tag{4.5}$$

As TL1 and TL2 are lossless, hence the stamp becomes:

$$\frac{\partial}{\partial z}\begin{bmatrix} V(z,s) \\ I(z,s) \end{bmatrix} = sE\begin{bmatrix} V(z,s) \\ I(z,s) \end{bmatrix}. \tag{4.6}$$

Now, the solution of (4.6) can be obtained using boundary conditions and is written as:

$$\begin{bmatrix} V(l,s) \\ I(l,s) \end{bmatrix} = e^{sEl}\begin{bmatrix} V(0,s) \\ I(0,s) \end{bmatrix}, \tag{4.7}$$

where e^{sEl} be the matrix of order 2×2 and it is expressed by matrix W, as:

$$e^{sEl} = W = \begin{bmatrix} W_{11} & W_{12} \\ W_{21} & W_{22} \end{bmatrix}. \tag{4.8}$$

The node potentials (v_P, v_{DN}, v_{DP} and v_Q) of the Terminals of lines TL1 and TL2 can be expressed as:

$$v_q = V_1(0,s) \quad \text{and} \quad v_{DP} = V_1(l,s), \tag{4.9}$$

$$v_{DN} = V_2(0,s) \quad \text{and} \quad v_Q = V_2(l,s). \tag{4.10}$$

Therefore, the differential voltage (v_{diff}) across the load resistor R_L can be written as:

$$v_{diff} = v_{DP} - v_{DN} = V_1(l,s) - V_2(0,s). \tag{4.11}$$

By using the exponential stamp [Anastasakis *et al.*, 1994] and [Singh *et al.*, 2021], the equations for

terminal voltages and terminal currents of transmission lines TL1 and TL2 are expressed as:

$$\begin{bmatrix} V_1(l,s) \\ I_1(l,s) \end{bmatrix} = e^{sEl} \begin{bmatrix} V_1(0,s) \\ I_1(0,s) \end{bmatrix}, \tag{4.12}$$

and

$$\begin{bmatrix} V_2(l,s) \\ I_2(l,s) \end{bmatrix} = e^{sEl} \begin{bmatrix} V_2(0,s) \\ I_2(0,s) \end{bmatrix}. \tag{4.13}$$

Further, using equation (4.8), the (4.12) can be represented as:

$$\begin{bmatrix} V_1(l,s) \\ I_1(l,s) \end{bmatrix} = \begin{bmatrix} W_{11} & W_{12} \\ W_{21} & W_{22} \end{bmatrix} \begin{bmatrix} V_1(0,s) \\ I_1(0,s) \end{bmatrix}, \tag{4.14}$$

and

$$\begin{bmatrix} V_2(l,s) \\ I_2(l,s) \end{bmatrix} = \begin{bmatrix} W_{11} & W_{12} \\ W_{21} & W_{22} \end{bmatrix} \begin{bmatrix} V_2(0,s) \\ I_2(0,s) \end{bmatrix}. \tag{4.15}$$

As in Figure 4.3.1, both the lines are in series connection the same amount of current will flow in both the lines TL1 and TL2,

$$I_1(l,s) = I_2(0,s). \tag{4.16}$$

Further, using (4.14) and (4.16), $I_2(0,s)$ is represented by:

$$I_2(0,s) = W_{21}V_1(0,s) + W_{22}I_1(0,s). \tag{4.17}$$

As in Figure 4.3.1, current entering the transmission line TL1 is $I_1(0,s)$, hence, current across Z_{th} in Figure 4.3.1 is also $I_1(0,s)$. Using equation (4.9), v_P can be written as:

$$v_P = V_1(0,s) = v_{th} - I_1(0,s)Z_{th}. \tag{4.18}$$

Further using equation (4.9) and (4.14), v_{DP} can be determined as:

$$\begin{aligned} v_{DP} = V_1(l,s) &= W_{11}V_1(0,s) + W_{12}I_1(0,s) \\ &= W_{11}v_{th} + I_1(0,s)(W_{12} - W_{11}Z_{th}). \end{aligned} \tag{4.19}$$

Using equations (4.10), (4.17) and (4.19), the expression of v_{DN} can be written as:

$$v_{DN} = v_{DP} - I_1(l,s)R_L, \tag{4.20}$$

$$\begin{aligned} v_x = v_{th}(W_{11} - W_{21}R_L) + I_1(0,s)(W_{12} - W_{11}Z_{th} + \\ W_{21}Z_{th}R_L + W_{22}R_L). \end{aligned} \tag{4.21}$$

From (4.10), the expression for v_Q can written as:

$$v_Q = V_2(l,s) = W_{11}V_2(0,s) + W_{12}I_2(0,s). \tag{4.22}$$

Since $V_2(0,s) = v_{DN}$ and $I_1(l,s) = I_2(0,s)$, the expression of v_Q can be modified as:

$$v_Q = k_1 v_{th} + I_1(0,s)k_2, \tag{4.23}$$

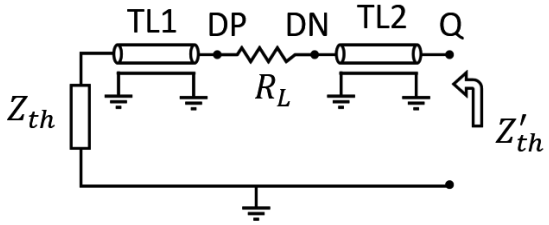

Figure 4.3.4: Thévenin equivalent circuit at endpoint of TL2 to determine $I_1(0,s)$.

where, k_1 and k_2 are given as:

$$k_1 = W_{11}(W_{11} - W_{21}) + W_{12}W_{21}, \tag{4.24}$$

$$\begin{aligned} k_2 = W_{11}(W_{12} - W_{11}Z_{th} + W_{21}Z_{th}R_L - W_{22}R_L) \\ -W_{12}W_{21}Z_{th} + W_{12}W_{22}. \end{aligned} \tag{4.25}$$

The equations of terminal voltages are reduced to the function of a single variable, $I_1(0,s)$. Since both the transmission lines TL1 and TL2 have a common return path (assumed as the ground) as shown in Figure 4.3.1, the current entering the line TL1 is the same as the current leaving the line TL2, i.e., $I_2(l,s) = I_1(0,s)$.

Assuming that both the lines TL1 and TL2 are lossless, another Thévenin circuit, as shown in Figure 4.3.4, is modeled at the end terminal of TL2 (i.e., at $z = l$) for determining the expression of $I_1(0,s)$. The Thévenin equivalent impedance at point Q is denoted by Z'_{th}, and can be written as:

$$Z'_{th} = Z_{th} + R_L, \tag{4.26}$$

and v_Q is the Thévenin voltage (v'_{th}) at point Q. Therefore the current $I_2(l,s)$ at this point can be expressed as:

$$I_2(l,s) = I_1(0,s) = \frac{v_Q}{Z'_{th}} = \frac{v_Q}{Z_{th} + R_L} \tag{4.27}$$

Further the expression for $I_1(0,s)$ is derived by substituting (4.23) in (4.27),

$$I_1(0,s) = \frac{k_1 v_{th} + k_2 I_1(0,s)}{Z_{th} + R_L}, \tag{4.28}$$

$$I_1(0,s) = \frac{k_1}{Z_{th} + R_L - k_2} v_{th}. \tag{4.29}$$

By substituting $I_1(0,s)$ in (4.18), (4.19), (4.21) and (4.23), the expression for node voltages v_P, v_{DP}, v_{DN} and v_Q can be derived. Now, the expression for differential voltage v_{diff} across the load R_L can be determined as:

$$v_{diff} = \left[W_{11} + (W_{22} - W_{21}Z_{th}) \left(\frac{k_1}{Z_{th} + R_L - k_2} \right) \right] R_L v_{th}, \tag{4.30}$$

where $v_{th} = \beta_1 v_{n_s} + \beta_2 v_{n_g}$, and β_1 and β_2 are the noise transfer functions from the noise sources to v_{th} for PSN and GBN, respectively. The expression for v_{diff} can be written as:

$$v_{diff} = \eta_1 v_{n_s} + \eta_2 v_{n_g}, \tag{4.31}$$

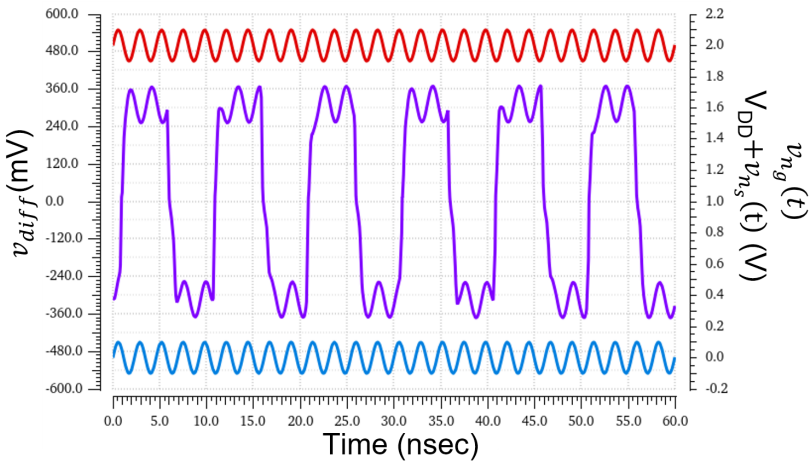

Figure 4.4.1: Differential response {left y-axis (middle), v_{diff}} in the presence of power supply {right y-axis (top), $v_{n_s}(t)$} and ground-bounce noise {right y-axis (bottom), $v_{n_g}(t)$}, along with the transmission line.

where η_1 and η_2 are the noise transfer functions from noise source to differential output v_{diff} with respect to power supply noise and ground-bounce noise.

4.3.2 Evaluation of Power Supply and Ground-Bounce induced Jitter

In this section, the estimation of jitter has been done by utilizing the EMPSIJ method proposed in. The jitter expression can be given as:

$$Jr = \frac{v_{diff}(t_m)}{\alpha}, \tag{4.32}$$

where α is the slope of the output when there is no noise present in the circuit and t_m is the time stamp of the midpoint ($V_{DD}/2$) of the differential output. Thus, the generalized jitter expression considering all the noise sources can be written as [Tripathi *et al.*, 2017]:

$$Jr = \frac{1}{\alpha}\sum_{i=1}^{N}\sum_{j=0}^{\infty}\eta_{ij}v_{n_{ij}}(t_m), \tag{4.33}$$

where η_{ij} is the generalized transfer function from i^{th} noise source to the output for a particular frequency j and N is the total number of noise sources. $v_{n_{ij}}$ is the jth frequency component of the ith noise source. A comparison is shown in the next section between the results obtained from the SPICE-based method and the proposed method for a thousand-bits.

4.4 Results and Discussion

In this section, various numerical examples are considered to validate the accuracy and applicability of the proposed methodology. The VMD circuit is designed at 180 nm CMOS technology node of United Microelectronic Corporation (UMC). The data signal of 100 MHz is applied at the input terminal, and the VMD circuit is operating with $V_{DD1} = 2.5V$ and $V_{DD} = 2V$. For analysis, the

distributed model of the transmission line is considered. The characteristic impedance and physical length of the line are 50 Ω and 100 mm. In the considered numerical example, the SPICE-based simulator takes around 900 seconds, whereas the proposed method takes only 0.65 seconds. The proposed method is faster than the SPICE-based simulator. Figure 4.4.1 shows the differential output along with power supply noise and ground-bounce noise. Both the noise sources have the same amplitude and frequency, 20 mV and 433 MHz.

Example-1:

In this example, jitter at the differential output is estimated by varying the amplitude of power supply and ground-bounce noise. Both the noise sources are assumed to be sinusoidal, having the same frequency of 433 MHz. The peak-to-peak amplitudes of both the noise sources are varied together from 0 to 100 mV, and jitter is estimated as shown in Figure 4.4.2. The results obtained from the proposed approach and from the SPICE-based simulator are compared; both results are in consonance with each other.

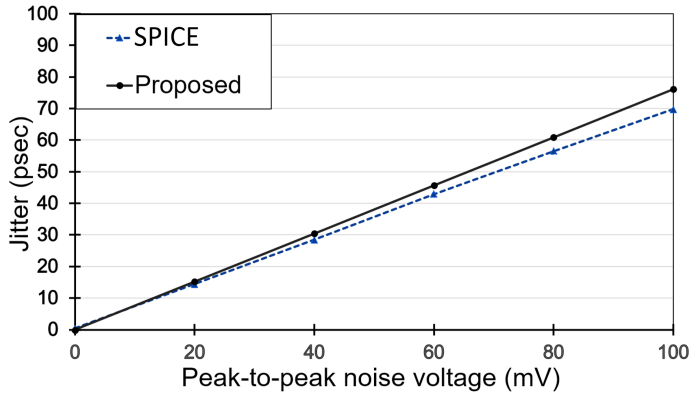

Figure 4.4.2: Jitter with respect to amplitude variation of noise source.

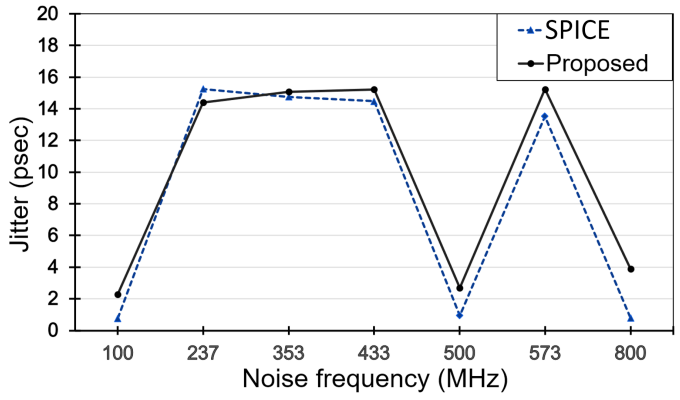

Figure 4.4.3: Jitter with respect to the frequency variation of noise source.

Example-2:

In this example, jitter is estimated considering the frequency variation of the power supply and ground-bounce noise. Both the noise sources are assumed to be sinusoidal, having the same am-

plitude of 20 mV. The frequencies of both the noise are varied from 100 MHz to 800 MHz as shown in Figure 4.4.3. The results obtained from the proposed approach are in close match with the results from the SPICE-based simulator. From the figure, it can be observed that when the noise frequencies are in harmonic with the input data frequency, the estimated jitter is very low, whereas at other frequencies, there is a significant amount of jitter.

4.5 Summary

As discussed earlier, the analytical approach for the estimation of jitter is more complex and computationally extensive; this chapter introduces a semi-analytical approach to estimate Power Supply Induced Jitter (PSIJ) for a Voltage-Mode Driver (VMD) circuit driving a load through long transmission lines (TLs). The semi-analytical method proposed in this chapter focuses on estimating jitter at the differential output of the VMD circuit in the presence of Power Supply Noise (PSN) and Ground-Bounce Noise (GBN). The proposed method uses a slope-based approach to estimate jitter in the circuit. The semi-analytical expressions are derived considering the distributed modeling for the transmission lines. The results obtained from the analytical method are compared with the results obtained from a SPICE-based simulator to validate the accuracy and efficacy of the proposed method. A significant speed-up in the estimation of jitter is observed using the proposed analytical method as compared to the SPICE-based simulator.