

Event-triggered Sliding Mode Control for Single-stage single-phase PFC application

In previous Chapter, Event-triggered sliding mode based loss-free resistor was presented for the PFC stage of a two-stage AC-DC-DC converter. The need for power factor correction in an electronic device was discussed. In light of the IEC 61000-3-2 guidelines, to keep the harmonic distortions in check, event-triggered implementation of the SLFR was justified. However, the aforementioned SLFR is a pre-defined constant and thus could be applied only for input current shaping application. Therefore, there was a need to introduce an adaptive emulated resistance such that it dynamically changes with the operating conditions, in order to serve the dual purpose of current shaping as well as voltage regulation.

In this Chapter, the concept of Adaptive Sliding mode based loss-free resistor (ASLFR) is proposed. This scheme gives a voltage regulation feature to the pre-regulator PFC, proposed using the existing SLFR technique, to accommodate any variations in the system parameters and still maintain the required performance. It serves as an ideal single stage PFC solution wherein, the two stage of PFC converter and DC/DC converter are combined in a single stage. The novel ASLFR for single-stage, single-phase PFC is then implemented using Event-triggered scheme.

Single-stage topologies trades-off between the power-factor correction and dynamic performance. In the literature considering single-stage active PFC, typically, a linear, two-loop PI controller is used to achieve the dual aim of PFC and voltage regulation. The inner control loop forces the input current to follow the sinusoidal supply voltage and the outer loop maintains the output voltage to its required value. The drawback of such conventional controller is the slow dynamic response [Nasirian *et al.*, 2013],[Fernandez *et al.*, 2005].

To enhance the dynamic response of the system and get tighter voltage regulation, another converter is suggested in cascade of the PFC. However, if the power level is low (e.g. less than 300 W), the fact of using two converters in cascade, with two control circuits, two protection systems, etc., makes this solution quite expensive [Lai and Su, 2015; Nasirian *et al.*, 2013]. On the other hand, single-stage solutions are preferred for low/medium power systems, as all the power does not need to be processed twice, thus giving better efficiency. Additionally, reduced components and control circuitry favour their usage [Chen *et al.*, 2016]. Irrespective of the methodology adopted and topology used, the fundamental principle behind PFC is to make the system, consisting of non-linear loads, emulate a pure resistive element at input terminals. That is the reason the notion of LFR makes an ideal and natural choice for this application as discussed in previous Chapter.

The work presented in this Chapter draws its inspiration from the seminal concept of Sliding mode based LFR (SLFR) which was introduced in [Cid-Pastor *et al.*, 2013] and extended in [Marcos-Pastor *et al.*, 2015]. The referred work uses SLFR scheme to achieve a pre-regulator PFC stage dedicated to power factor correction only. In this Chapter, however, a revamped version of the methodology in terms of *Adaptive SLFR* is proposed. That is, the emulated input resistance is made adaptive in nature, to accommodate any changes in power requirements brought about by line and load variation, without compromising the dynamic performance.

Application of ASLFR for PFC presents a single-stage solution, i.e., it will not only make the converter behave as a power factor correcting circuit but will also ensure voltage regulation over the wide spectrum of operational settings. Thus eliminating the need of an extra stage of converter. The proposed controller exhibits itself as an ideal single-stage PFC solution that provides near unity power factor with desired dynamic response, and is also robust to line and load variations. A generic model is presented in the Chapter, which can be implemented over a variety of converter topologies. A single-stage boost PFC topology operating in Continuous Conduction Mode (CCM) is chosen to implement the proposed controller. Unlike a boost converter working under DCM (in which the converter inherently exhibits resistive behaviour at the input), the chosen CCM operated boost converter requires a controller to achieve unity power factor.

The work proposes a first order sliding control surface that uses both the input current error and output voltage error terms. The reference inductor current, for the current error term, is made adaptive with the use of ASLFR. A tuning parameter α , in the surface, provides a trade-off between the two actions of pf correction and regulation. The proposed controller shows excellent dynamic performance with voltage recovery to its reference value within a single sinusoidal cycle of rectified AC, without any under/overshoot under load perturbations.

The rest of the Chapter is organized as follows. In Section 4.1, the concept of the proposed ASLFR is discussed. The process of realizing the controller is presented in Section 4.2. The in-depth stability analysis for the controller is covered in Section 4.3. Section 4.4 and 4.5 present the simulation and experimental results, respectively, for the ASLFR adoption. Section 4.6 presents the Event-triggered ASLFR for the Single stage application. Conclusion of the Chapter is provided in Section 4.7.

4.1 ADAPTIVE SLIDING MODE BASED LOSS FREE RESISTOR (ASLFR)

The working of the SLFR was thoroughly covered in the previous Chapter. The emulated resistance was a pre-defined constant and was fixed for the entire operating conditions. In the work carried out in this Chapter, the input power is allowed to vary in order to meet the load demand. This is accomplished by making, the LFR r adaptive; it is changed to accommodate load and line variations. In order to realize an ideal loss-less resistive input impedance r , the power balance equation ($\frac{V_1^2}{r} = \frac{V_2^2}{R}$) is re-written as

$$r = \frac{V_1^2}{V_2^2} R \quad (4.1)$$

As long as the load resistance R stays fixed, for the given input voltage and power, the emulated resistance r stays fixed.

This work uses (4.1), to adapt r for any changes sensed in line or load, to ensure that the system always keeps the output voltage to the required one.

Let δv_1 be the variation in RMS value of the input voltage, δR is the load variation and δr is the adapted change which occurs in the emulated input impedance. Here V_1 , R , r , and V_{ref} are the nominal values of the designated variables. Then,

$$r + \delta r = \frac{(V_1 + \delta v_1)^2 (R + \delta R)}{V_{ref}^2} \quad (4.2)$$

Expanding (4.2) and comparing the first order terms gives

$$\delta r = \frac{(V_1^2 \delta R + 2V_1 R \delta v_1)}{V_{ref}^2} \quad (4.3)$$

Thus r will adapt itself dynamically with the varying load, line and required output voltage, whenever a change in variables is detected. Hence, giving a robust behaviour.

As the load demand is increased/decreased, the input current increases/decreases in response, so as to regulate the output voltage to its reference value irrespective of any load variation. Since an ideal switching converters transfer the input power to the output port (in principle), without any loss, the notion of *POPI* (Power Out=Power In) stands true.

4.2 REALIZING ADAPTIVE SLIDING MODE BASED LOSS FREE RESISTOR (ASLFR)

This section gives a detailed procedure for realizing ASLFR in a generalized way such that the concept can be applied to a set of converters. As pointed out in [Cid-Pastor *et al.*, 2013], candidates for LFR operation using SMC have topological constraints that the input current used in the surface must be the current through an inductor or a sum of currents through inductors. Some of the converters fulfilling this criterion include boost converter, Ćuk, SEPIC etc.

Then on, the presented generic model is implemented to make the boost converter exhibit adaptive LFR behaviour.

4.2.1 General Model

A general non-linear model of a switching converter is considered in (4.4) .

$$\dot{x}_1 = f_1(x_1, x_2) + g_1(x_1, x_2)u(t) \quad (4.4a)$$

$$\dot{x}_2 = f_2(x_1, x_2) + g_2(x_1, x_2)u(t) \quad (4.4b)$$

Where, x_1, x_2 are the system states, $u(t)$ is the system control input. f_1, g_1, f_2 , and g_2 are Lipschitz functions.

The switching function is defined as:

$$s(x, t) = c^T(x - x_r) \quad (4.5)$$

Here, $c^T = [\alpha \ 1]$ is a vector containing sliding surface parameters, $x = [x_1 \ x_2]^T$ is the state vector and x_r is the reference vector for x . For this application, $x_1 = i_L$ is a linear combination of state variables which form the input current and $x_2 = v_o$ is the output voltage. Thereby, $c^T x = \alpha i_L + v_o$. The reference term of the surface is formed by $c^T x_r = \alpha i_{Lref} + V_{ref}$. The term i_{Lref} is replaced by $g(t)v_1$ to emulate LFR, where $g(t)$ is the proportionality constant equal to the inverse of the emulated input impedance $r(t)$.

Using (4.4), (4.5), the derivative of the switching function is given as:

$$\begin{aligned} \frac{ds}{dt} &= c^T \dot{x} - c^T \dot{x}_r \\ &= c^T (f_1(x_1, x_2) + f_2(x_1, x_2) + (g_1(x_1, x_2) + g_2(x_1, x_2))u(t)) - c^T \left(\frac{di_{Lref}}{dt} + \frac{dv_o}{dt} \right) \end{aligned} \quad (4.6)$$

The transversality condition [Serna-Garcés *et al.*, 2016], is a necessary condition to ensure the existence of sliding mode.

$$\frac{\partial}{\partial u} \left(\frac{ds(x(t), t)}{dt} \right) = c^T (g_1(x_1, x_2) + g_2(x_1, x_2)) \neq 0 \quad (4.7)$$

If (4.7) is satisfied, then the equivalent continuous control is obtained by substituting

$$\left. \frac{ds}{dt} \right|_{u=u_{eq}} = 0$$

Using (4.6),

$$u_{eq}(t) = \frac{c^T \left(\frac{di_{Lref}}{dt} + \frac{dv_o}{dt} \right) - c^T ((f_1(x_1, x_2) + f_2(x_1, x_2)))}{c^T (g_1(x_1, x_2) + g_2(x_1, x_2))} \quad (4.8)$$

If the value of the derivative in (4.7) is positive, and the derived equivalent control satisfies

$$0 < u_{eq}(t) < 1$$

then adopting the following switching law [Utkin *et al.*, 1999] will ensure the existence condition.

$$u = \begin{cases} 0, & \text{if } s > 0. \\ 1, & \text{if } s < 0. \end{cases} \quad (4.9)$$

If the value of (4.7) is < 0 , the inequalities of (4.9) must be reversed.

The principle of realizing adaptive LFR, using SMC on the switching converter, is represented in the block diagram Fig. 4.1.

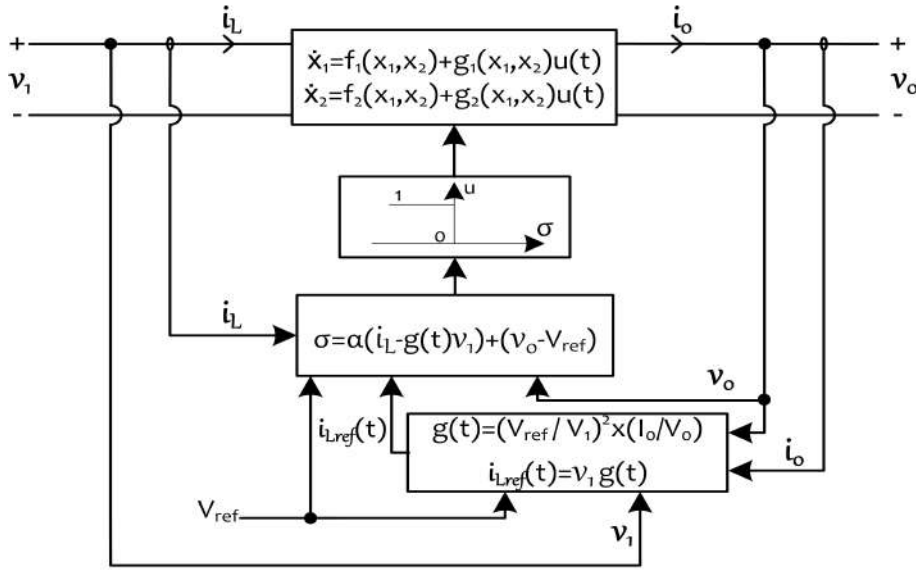


Figure 4.1 : Block diagram of switching converter emulated as ASLFR

4.2.2 System Description

A boost topology, working in CCM is used to implement the developed generic model. The system under consideration is depicted in Fig. 4.2. The bridge rectifier is fed by a sinusoidal AC voltage. At the output of which, a boost converter is connected. The converter dynamics can be represented mathematically using state-space averaging [Utkin *et al.*, 1999] as:

$$\dot{x}_1 = \frac{-x_2}{L_o}(1-u) + \frac{v_1}{L_o} \quad (4.10a)$$

$$\dot{x}_2 = \frac{x_1}{C_o}(1-u) + \frac{-x_2}{RC_o} \quad (4.10b)$$

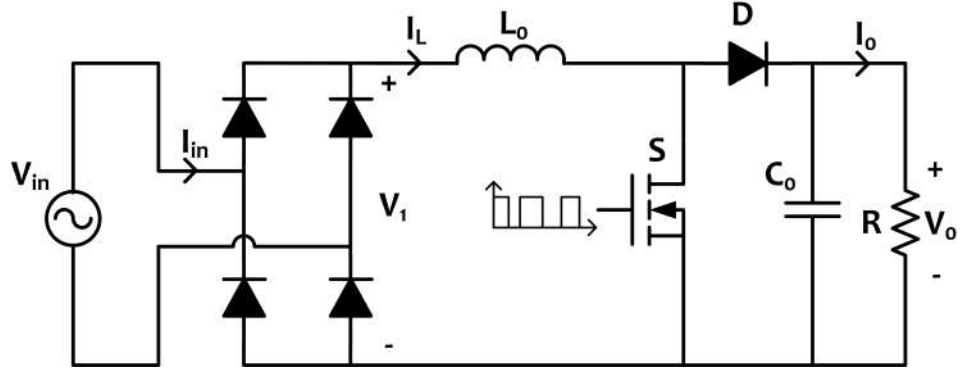


Figure 4.2 : PFC based on a boost converter

Where, v_1 is the rectified input voltage, inductor current x_1 and capacitor voltage x_2 are the states of the system. u is the control input and L_o , C_o , and R are the inductance, capacitance and load resistance respectively. The ESR of film capacitor is generally negligible. Thereby, the output capacitor voltage is also output voltage of the converter.

4.2.3 Proposed Switching function

Design of Sliding Mode Control to realize LFR involves design of the switching surface and a control law. The proposed switching surface has a voltage error term in addition to the current term. Moreover, a tuning parameter α augments the system dynamics to provide a trade-off between the precise regulation and the unity power factor. The proposed surface is:

$$s := \alpha(x_1 - x_{1r}(t)) + (x_2 - x_{2r}) \quad (4.11a)$$

$$= \alpha(x_1 - \frac{v_1}{r(t)}) + (x_2 - x_{2r}) \quad (4.11b)$$

$$= \alpha(x_1 - g(t)v_1) + (x_2 - x_{2r}) \quad (4.11c)$$

Here, the reference inductor current (x_{1r}) varies dynamically in shape (to follow the input AC voltage) and also in amplitude (to adapt to the desired operating conditions), x_{2r} is the reference output voltage, parameter $r(t)$ is the dynamically adaptive input resistance as given by (4.2) and $g(t) = r(t)^{-1}$. It allows to generate the reference inductor current as explained in the next sub-section.

4.2.4 Reference current generation

The evaluation of reference inductor current based on adaptive SLFR r , for the proposed surface, is discussed in this sub-section.

Note that for the boost topology, the inductor current is the same as the current supplied by the rectified AC voltage supply to the converter. Now, since the input of the SLFR is a voltage source v_1 and the output port behaves as a resistor, from the Ohm's law, the relation between the reference inductor current and the resistor, $r(t)$, value, is given as

$$\begin{aligned} I_{Lref}(t) &= v_1/r(t) \\ x_{1r}(t) &= v_1/r(t) \end{aligned} \quad (4.12)$$

In the present scope of work, the proportionality constant SLFR r changes dynamically, as

explained in earlier section of the Chapter. The emulated input resistance is calculated as per the operating conditions, following (4.2). Thus, the generated reference current varies not only with the input voltage but also with the load, to meet the load demands.

4.2.5 Control Law

The transversality condition evaluates the existence of the control input in the derivative of the sliding-surface. It is a necessary condition to ensure the ability of the sliding mode controller to modify the system behaviour. It requires

$$\frac{d}{du}\left(\frac{ds}{dt}\right) \neq 0$$

In this case, it can be seen that

$$\frac{d}{du}\left(\frac{ds}{dt}\right) = \alpha \frac{x_2}{L_o} - \frac{x_1}{C_o} > 0 \quad (4.13)$$

The design parameter α is chosen such that from (4.13), the transversality is positive for all the conditions. Since (4.13) is true, then the adopted switching law must follow

$$u = \begin{cases} 0, & \text{if } s > 0. \\ 1, & \text{if } s < 0. \end{cases} \quad (4.14)$$

Therefore, the control law is chosen in this work is given as:

$$u = \frac{1}{2}[1 - \text{sign}(s)] \quad (4.15)$$

4.2.6 Equivalent Control

As established from transversality condition

$$\frac{d}{du}\left(\frac{ds}{dt}\right) \neq 0$$

Then, the continuous equivalent of the control law (4.15) is derived by imposing

$$\left.\frac{ds}{dt}\right|_{u=u_{eq}} = 0$$

Using (4.10), the derivative of (4.11c) is obtained, assuming g to be constant for an operating condition, as

$$\dot{s} = \alpha \left(\frac{-x_2}{L_o} (1 - u) + \frac{v_1}{L_o} \right) - \alpha g \frac{dv_1}{dt} + \frac{x_1}{C_o} (1 - u) - \frac{x_2}{RC_o} \quad (4.16)$$

Replacing u by u_{eq} and equating it to 0, leads to the following expression for equivalent control.

$$u_{eq} = \frac{\alpha \left(\frac{x_2 - v_1}{L_o} \right) + \alpha g \frac{dv_1}{dt} - \frac{x_1}{C_o} + \frac{x_2}{RC_o}}{\alpha \frac{x_2}{L_o} - \frac{x_1}{C_o}} \quad (4.17)$$

4.3 ANALYSIS OF THE SLIDING MODE CONTROL

The present section deals with the analysis of the sliding mode to establish the existence of sliding mode and the stability of the proposed surface.

4.3.1 Reachability Condition

This condition ensures the existence of the sliding mode i.e. the chosen control law will make the system trajectories reach the designed sliding surface in finite time and will maintain sliding motion then on. It requires to satisfy the η -reachability condition, i.e.

$$s\dot{s} < -\eta|s| \quad (4.18)$$

for some $\eta > 0$.

Using (4.16), the following can be obtained

$$s\dot{s} = s\left\{\alpha\left(-\frac{x_2}{L_o}(1-u) + \frac{v_1}{L_o}\right) - \alpha g \frac{dv_1}{dt} + \frac{x_1}{C_o}(1-u) - \frac{x_2}{RC_o}\right\} \quad (4.19a)$$

$$= s\left\{(1-u)\left(-\frac{\alpha x_2}{L_o} + \frac{x_1}{C_o}\right) - \frac{x_2}{RC_o} + \Gamma\right\} \quad (4.19b)$$

$$= s\left\{\frac{1}{2}(1 + \text{sign}(s))\left(-\frac{\alpha x_2}{L_o} + \frac{x_1}{C_o}\right) - \frac{x_2}{RC_o} + \Gamma\right\} \quad (4.19c)$$

Where,

$$\Gamma := \alpha\left\{\frac{v_1}{L_o} - g \frac{dv_1}{dt}\right\} \quad (4.20a)$$

$$= \alpha\left\{\frac{V_p |\sin(\omega t)|}{L_o} - g V_p \omega |\sin(\omega t)| * \cot(\omega t)\right\} \quad (4.20b)$$

where, V_p is the peak input AC voltage, $\omega = 2\pi f$ is the supply frequency.

Remark: v_1 is a periodic function with a period of π . The derivative for v_1 exists for the entire period except at the corner point i.e. it exists for $(\omega t) \in \Re - n\pi$. Thus, Γ is also a bounded, periodical function with period π . It is analysed for a single period to find the maximum and minimum bounds. And they are given as

$$\Gamma_{max} = \alpha\left\{\frac{V_p}{L_o \sqrt{1 + (g\omega L_o)^2}} + \frac{V_p g^2 \omega^2 L_o}{\sqrt{1 + (g\omega L_o)^2}}\right\} \quad (4.21)$$

$$\Gamma_{min} = \alpha g \omega V_p \quad (4.22)$$

When $s > 0$, from (4.14) $u = 0$, thus, (4.19c) becomes

$$s\dot{s} = |s|\left(-\alpha \frac{x_2}{L_o} + \frac{x_1}{C_o} - \frac{x_2}{RC_o} + \Gamma\right) \quad (4.23)$$

In order to satisfy (4.18), the bounds obtained over Γ is used to get the following inequality

$$-\Gamma_{max} - \eta + \frac{x_2}{RC_o} + \alpha \frac{x_2}{L_o} > \frac{x_1}{C_o} \quad (4.24)$$

When $s < 0$, (4.19c) becomes

$$s\dot{s} = -|s|\left(-\frac{x_2}{RC_o} + \Gamma\right) \quad (4.25)$$

then, to fulfil (4.18)

$$\Gamma_{min} - \eta > \frac{x_2}{RC_o} \quad (4.26)$$

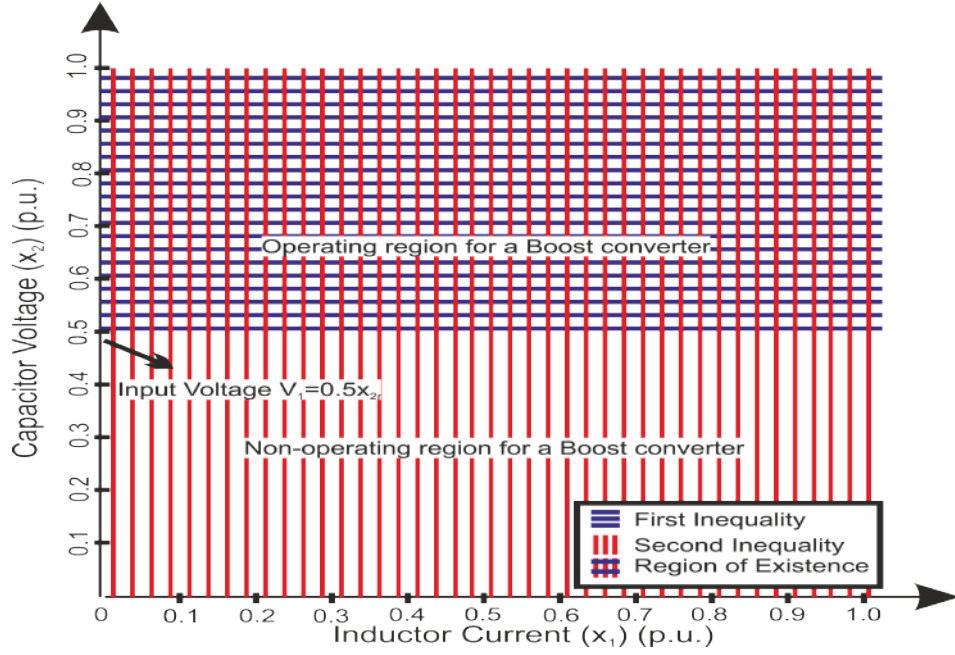


Figure 4.3 : Region of Existence

Therefore, as long as the states satisfy the inequalities given by (4.24) and (4.26), the system trajectory continuously moves towards the sliding manifold. Hence, the reachability condition is established. The region of existence of sliding mode for the normalized variables is shown in Fig. 4.3.

The intersection of the two inequality areas shows the region where both the conditions are satisfied. For a boost converter the initial capacitor voltage is equal to the input voltage (assumed as half of the rated output voltage) and the initial current is 0. Therefore, the boost converter capacitor voltage (x_2) will always be operating at or above the input voltage, thus, the entire operating region lies in the region of existence and which in turn ensures the reachability for states, as depicted.

4.3.2 Stability of the closed loop system during Sliding mode

Once the trajectories reach the sliding surface, it is to be ensured that the states converge to their equilibrium points.

For the ease of analysis, the system dynamics (4.10) is written in error co-ordinates as

$$\dot{e}_1 = \frac{1}{L_o}(v_1 - (1 - u_{eq})(e_2 + x_{2r})) - g \frac{dv_1}{dt} \quad (4.27a)$$

$$\dot{e}_2 = \frac{1}{C_o}((1 - u_{eq})(e_1 + x_{1r}) - \frac{(e_2 + x_{2r})}{R}) \quad (4.27b)$$

The state variables are the inductor current error (e_1) and output capacitor voltage error (e_2), such that $e_1 = x_1 - x_{1r}$ and $e_2 = x_2 - x_{2r}$. Here, x_1 is the inductor (or input) current and x_{1r} is its reference value. x_2 is the output capacitor voltage and x_{2r} is its reference value. The control input on the surface is given by its equivalent control u_{eq} .

Then (4.11c) can be written in error terms as:

$$s = \alpha e_1 + e_2 \quad (4.28)$$

During sliding mode, ($s = 0$),

$$\alpha e_1 + e_2 = 0 \quad \text{Or, } e_1 = \frac{-e_2}{\alpha} \quad (4.29)$$

From (4.29), it is clear that the convergence of e_2 ensures convergence of e_1 . Therefore, only convergence proof for e_2 is required.

Let the Lyapunov function be, $V = \frac{1}{2}e_2^2$. Then

$$\dot{V} = e_2 \dot{e}_2 \quad (4.30)$$

Using (4.27b) and (4.29), equation (4.30) becomes

$$\dot{V} = -\frac{e_2^2}{C_0} \left(\frac{(1-u_{eq})}{\alpha} + \frac{1}{R} \right) - e_2 \left(\frac{x_{2r}}{R} - (1-u_{eq})x_{1r} \right) \quad (4.31)$$

Now, using (4.1) and (4.12) the relation between the reference values is obtained as

$$x_{1r} = \frac{v_1}{r} = \frac{x_{2r}^2 v_1}{V_1^2 R} \quad (4.32)$$

Then, (4.31) is further simplified as

$$\dot{V} = -e_2^2 \left\{ \frac{(1-u_{eq})}{\alpha C_0} + \frac{1}{RC_0} \right\} - e_2 \frac{x_{2r}}{R} \left\{ 1 - (1-u_{eq}) \frac{x_{2r} v_1}{V_1^2} \right\} \quad (4.33a)$$

$$= -e_2^2 \kappa_1 - e_2 \beta \kappa_2 \quad (4.33b)$$

In order for the system to be stable, $\dot{V}$ must be negative. The first term in (4.33) ($-e_2^2 \kappa_1$) is always negative as $\kappa_1 = \left\{ \frac{(1-u_{eq})}{\alpha C_0} + \frac{1}{RC_0} \right\}$ is a positive quantity with $0 < 1-u_{eq} < 1$ and positive tuning parameter α . However, in the second term, $\kappa_2 = \left\{ 1 - (1-u_{eq}) \frac{x_{2r} v_1}{V_1^2} \right\}$ as well as e_2 can change their sign. Hence, the sign of $\dot{V}$ is subjected to the signs κ_2 and e_2 bear. Thus, (4.33) is analysed for these cases.

- Case 1: When e_2 and κ_2 have the same sign.
In this scenario, (4.33) can be written as

$$\dot{V} = -|e_2|^2 \kappa_1 - |e_2| |\beta| |\kappa_2|$$

Thus, $\dot{V}$ will always be negative and the system will move towards the equilibrium point.

- Case 2: When e_2 and κ_2 have different signs.
Then, (4.33) can be written as

$$\dot{V} = -|e_2|^2 \kappa_1 + |e_2| |\beta| |\kappa_2|$$

Here, $\dot{V}$ will be negative if

$$|e_2|^2 \kappa_1 > |e_2| |\beta| |\kappa_2| \quad (4.34a)$$

$$|e_2| > |\beta| \frac{|\kappa_2|}{|\kappa_1|} \quad (4.34b)$$

This implies that the trajectory will enter in a circle which has a center at origin and radius (4.35)

$$rad = |\beta| \frac{|\kappa_2|}{|\kappa_1|} + \varepsilon \quad (4.35)$$

where, ε is an arbitrarily small positive number. However, the radius is a function of system parameters and tuning parameter α and can be minimized by their careful selection.

Now, the constraints on $1 - u_{eq}$ to be limited within the minimum and maximum values of 0 and 1, leads to

$$0 < \alpha \frac{v_1}{L_o} - \alpha g \frac{dv_1}{dt} - \frac{x_2}{RC_o} < \alpha \frac{x_2}{L_o} - \frac{x_1}{C_o} \quad (4.36)$$

The inequalities derived from (4.36) are same as given in (4.24) and (4.26). This implies that $\dot{V} < 0$ and the system states will converge to enter in a circle around the origin with the radius given by (4.35), once it reaches the surface.

4.4 SIMULATION STUDIES

The proposed control scheme is validated through simulation. Table 4.1 shows the specific values of the design parameters for the boost PFC and nominal operating conditions. The system is simulated using MATLAB-Simulink tool.

The simulation results are categorized into two sections. The first section illustrates the adaptive nature of the SLFR r . A comparative analysis is shown in the second section, between the proposed work, the SLFR based work presented in [Cid-Pastor *et al.*, 2013] and a dual loop PI controller performance.

Table 4.1 : System Parameters

Parameter	Value
Boost converter	
Input Voltage Supply	100 V, 50 Hz
Nominal Output voltage	150 V
Inductance (L_o)	1.6 mH
Output capacitor (C_o)	220 μ F
Tuning parameter α	100

4.4.1 Adaptive nature of proposed SLFR

This section is further divided into different subsections to explore the adaptive nature of SLFR r with respect to variation in load resistance R , input voltage V_{in} and reference output voltage V_{ref} . Furthermore, the adaptivity is also discussed for a combinational load of CPL and resistance. The nominal values of the system operating conditions are taken as: $V_{in} = 100$ V, 50 Hz, $V_{ref} = 150$ V, load resistance $R = 300 \Omega$. The output voltage V_o , generated reference inductor current I_{Lref} and emulated input resistance r are shown for all the undertaken cases.

- **Load Change:** The system response to the load resistance change from 300Ω to 150Ω at $t=0.25$ sec, i.e. (75 W to 150 W), while keeping the other parameters to their nominal values, is shown in Fig. 4.4.

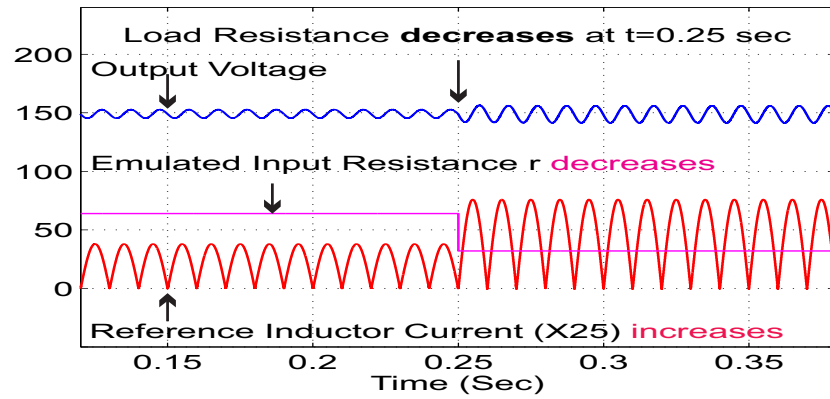


Figure 4.4 : Adaptivity of r to load resistance variation

- **Input voltage Change:** A change in the input voltage from 80 V to 100 V is brought about at $t=0.25$ sec with no change in other parameters. The response is shown in Fig. 4.5.

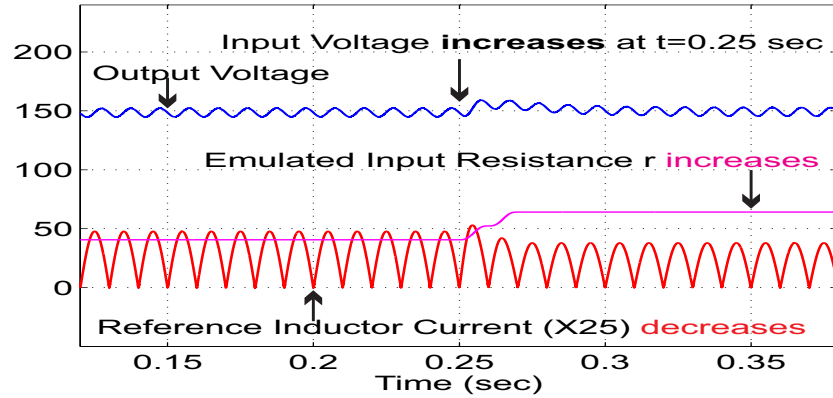


Figure 4.5 : Adaptivity of r to input voltage variation

- **Reference Voltage Change:** Fig. 4.6 shows the system response when the reference output voltage is changed from 150 V to 120 V at $t=0.25$ sec with other parameters kept to their nominal values.

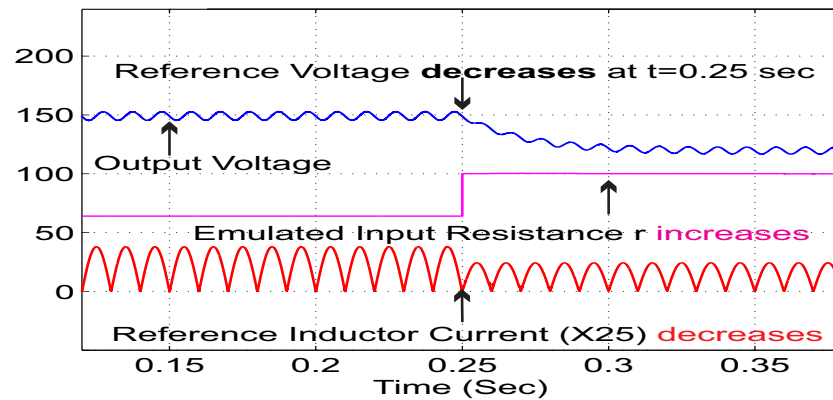


Figure 4.6 : Adaptivity of r to reference voltage variation

A power factor > 0.999 is observed for all the undertaken cases. Also, it is noticed that r adapts itself to the changes in the operating power brought about by varying either the line or load conditions. This variation in r causes the inductor reference current to change, in order to meet the performance requirement at the new point of operation. The system response, for all the cases, is in line with the theoretical claims made in the above section.

Moreover, in the presented work, sensors are used to measure output voltage and current continuously and therefore, the power demand at every instant is known. And since the calculation of the emulated resistor is based on the power balance equation, any load, whether resistive or not, can be represented using an equivalent resistor $R_{eq} = \frac{V_o}{I_o}$, as shown in Fig. 4.7. And, therefore, the analysis which has been carried out considering the load to be purely resistive still stands true.

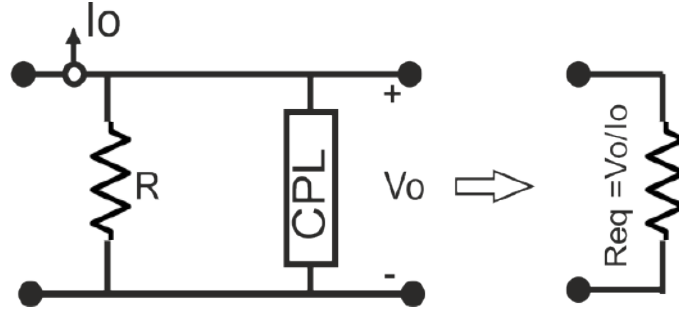


Figure 4.7 : Representing a combination load as equivalent resistive load $R_{eq} = \frac{V_o}{I_o}$

In support of the above claim, the system with the combinational load of $CPL = 100\text{ W}$ and $R = 100\ \Omega$ is simulated and the response is presented in Fig. 4.8. The figure gives Inductor current, output voltage, equivalent resistance and emulated resistance profile. Please note that the Equivalent resistance profile is not linear but still the controller is able to make the inductor current follow the reference inductor signal and regulate the output voltage.

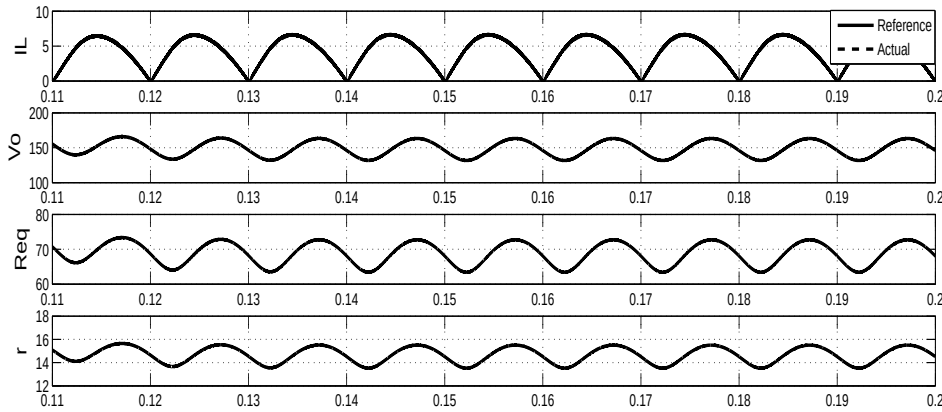


Figure 4.8 : System response and R_{eq} profile for a CPL load

4.4.2 Comparative Analysis

The present section compares the system response, in the event of load change. The comparison is carried out between the proposed controller, the SLFR based controller and the most commonly adopted dual PI controllers. Since the existing SLFR based work [Cid-Pastor *et al.*, 2013], is designed as a PFC pre-regulator only, it does not provide any compensation to change in load

conditions (as discussed in previous sections), therefore the system operating point changes with load variation. The third controller under assessment is the dual loop PI controller which uses PI control for both the inner control loop and outer voltage loop. The comparison with PI controller is done to quantize the dynamic performance of the presented controller.

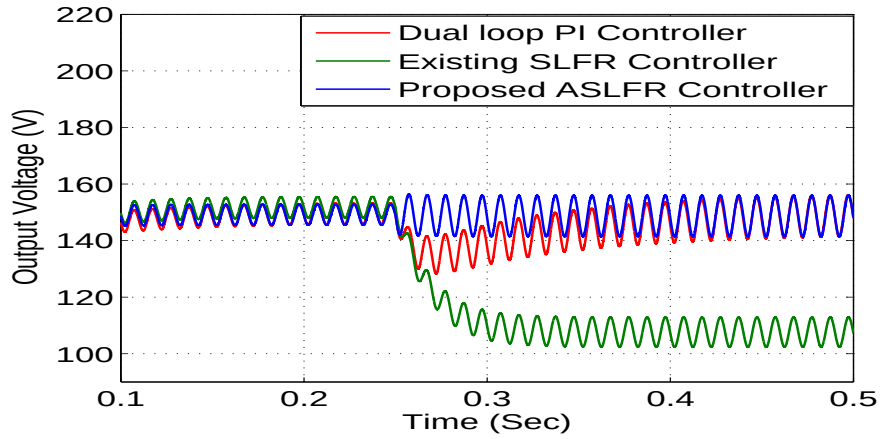


Figure 4.9 : Output Voltage waveform under load change

In Fig 4.9, at $t=0.25$ sec, the load is changed from $300\ \Omega$ to $150\ \Omega$. PI controller shows a voltage undershoot from 150 V to 130 V of -13.33% . The output voltage takes 150 ms to comeback to the reference value. The existing SLFR based controller does not provide any voltage regulation and the voltage drops from 150 V(Avg) to 110 V(Avg). The proposed controller, on the other hand, provides the voltage regulation within one cycle itself with no observed undershoot.

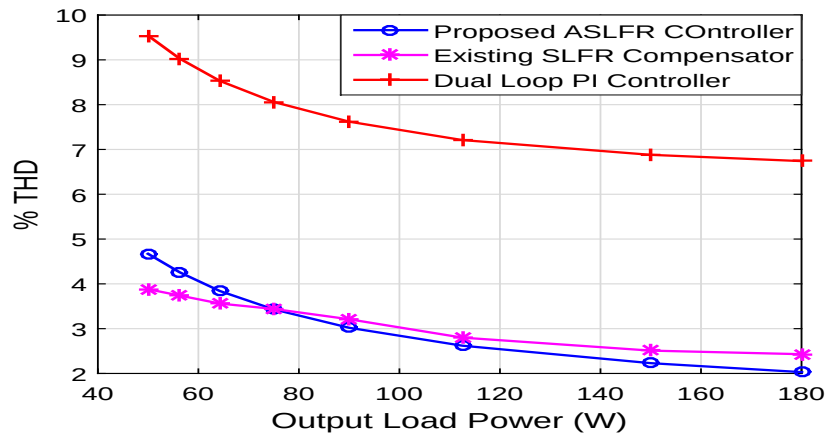


Figure 4.10 : %THD in input current for the three controllers.

Additionally, %THD in the input current is plotted for the PI controller, existing SLFR compensator and the proposed ASLFR controller, for different output power in Fig. 4.10. It can be seen that the PI controller response has the highest distortion, while for the proposed controller and the existing SLFR compensator the THD values are comparable. Furthermore, the proposed controller provides better result than the existing PFC pre-regulator as the load increases.

The simulation results of PI, the existing SLFR controller [Cid-Pastor *et al.*, 2013] and proposed controller are summarized in Table 4.2. From the comparison table, it can be concluded that

the performance of the proposed controller is better than the other controllers, in terms of better and faster voltage regulation and power factor correction, both. Secondly, for this topology, the input power pulsation is absorbed by the output capacitor, thereby reducing the output voltage ripple. Presently, output capacitor used is $220\text{ }\mu\text{F}$ which can be increased to reduce the ripple in voltage, however, bulkier capacitor increases the distortion in the input current.

Table 4.2 : Comparison of simulation results

Parameter	Dual loop PI controller	Existing SLFR Cid-Pastor <i>et al.</i> [2013]	Proposed ASLFR Controller
Inductor	1.6 mH	1.6 mH	1.6 mH
Output capacitor	220 μF	220 μF	220 μF
Input voltage	100 V, 50 Hz	100 V, 50 Hz	100 V, 50 Hz
Reference output voltage	150 V	150 V	150 V
Load Transients	75 W to 150 W	75 W to 150 W	75 W to 150 W
Peak to Peak ripple in voltage	7V, 14V	7V,11V	7V, 14V
Output voltage undershoot	-13.33%	Drops to 110V (Avg.)	No undershoot
Voltage recovery time	150 ms	No compensation	Within a cycle
% THD	8.09%, 6.83%	3.44%, 2.53%	3.42%, 2.23%
Emulated Input Resistance	-	66.67 Ω	66.67 Ω , 33.33 Ω

4.5 EXPERIMENTAL STUDIES

An experimental validation, of the proposed theory analogous to simulation study, is presented using a 200 W laboratory prototype of the converter. Fig. 4.11 shows the set-up for experimentation consisting of the designed converter, with the specifications provided in Table 4.1. In

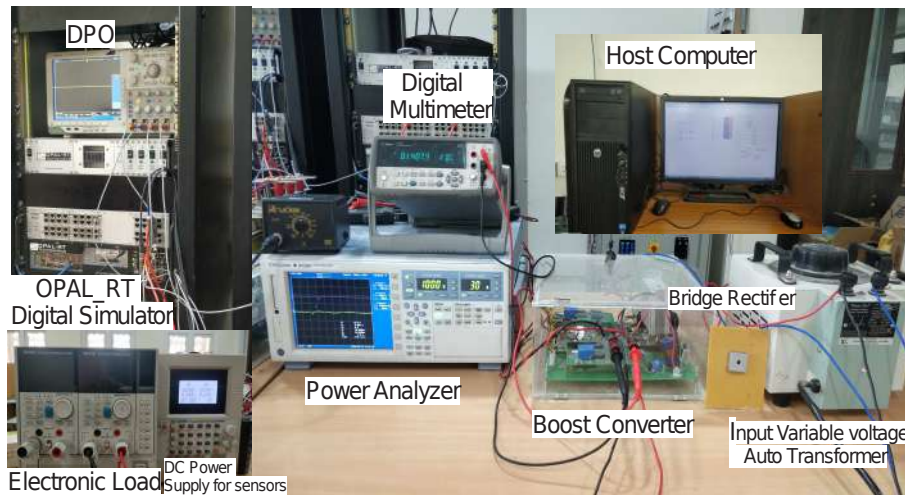


Figure 4.11 : Experimental setup

Fig. 4.11, a boost converter, a bridge rectifier, electronic load, power analyser, digital multimeter, DC power supply for sensors, DPO and control platform (OPAL-Real Time Digital Simulator) are shown. The Isolation transformer takes power from the 230 V, 50 HZ mains and then on a variac is used to vary the input ac voltage fed to the converter. Experimental parameters are kept same as the simulation parameters. The tuning parameter, α is also kept same as for the simulation i.e. , $\alpha = 100$.

In the section, the experimental results showing the system response to three different cases are presented. The cases involve (I) Response to Load transients, (II) Response to Line or input voltage variation and, (III) Response to change in reference output voltage. Additionally, the experimental distortion data at different load conditions is presented and compared against the regulatory requirements.

4.5.1 Test Case-I: Response to Load Transient

In order to highlight the adaptive nature of the proposed controller to load change, a transition in load resistance, from $300\ \Omega$ to $150\ \Omega$ is made and the system response is presented in Fig. 4.12. The oscilloscope capture demonstrates the Rectified AC voltage V_1 , Inductor current I_L , and the output voltage V_o regulation, under variable load conditions. The channels have been set to $100\ \text{V/div}$ for V_o , $500\ \text{mA/div}$ for I_L and $40\ \text{V/div}$ for V_1 . Time base is set to $10\ \text{ms/div}$.

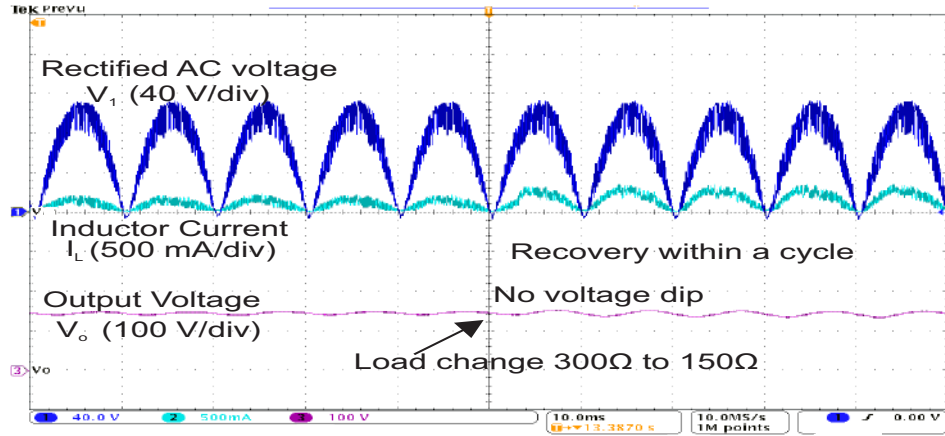
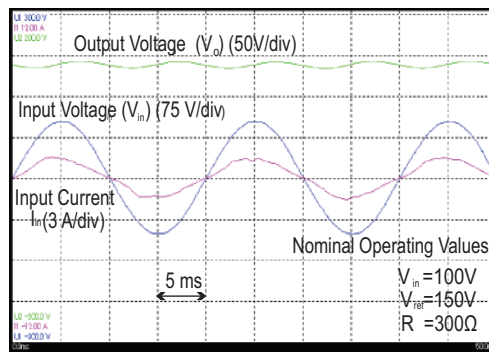
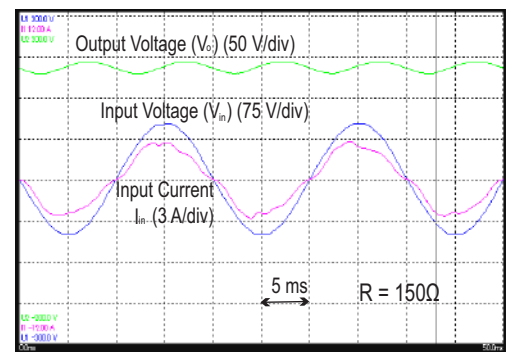


Figure 4.12 : Response of ASLFR based controller to Test Case-I. CH1: Rectified AC Input Voltage V_1 ($40\ \text{V/div}$). CH2: Inductor Current I_L ($500\ \text{mA/div}$). CH3: output capacitor voltage V_o ($100\ \text{V/div}$). Time base $10\ \text{ms/div}$.

The next Fig. 4.13 presents the corresponding Input AC voltage V_{in} , Input AC current I_{in} and the regulated Output voltage V_o waveform for the two load cases. The capture has been made using Yokogawa WT3000 Precision Power Analyser. In the captured screen the output voltage V_o is set to $50\ \text{V/div}$, input voltage V_{in} is $75\ \text{V/div}$ and the input current I_{in} is set to $3\ \text{A/div}$. The time base is $5\ \text{ms/div}$.



(a) Load Resistance $300\ \Omega$



(b) Load Resistance $150\ \Omega$

Figure 4.13 : Input Current, Input Voltage and Output Voltage waveform for Test Case-I

The above results shows that the proposed controller reacts sufficiently fast to the load transients. The output voltage is regulated to its reference value with in a single cycle with no undershoots. The voltage ripple magnitude seems to have increased with the increase in load which is in congruence with the theory.

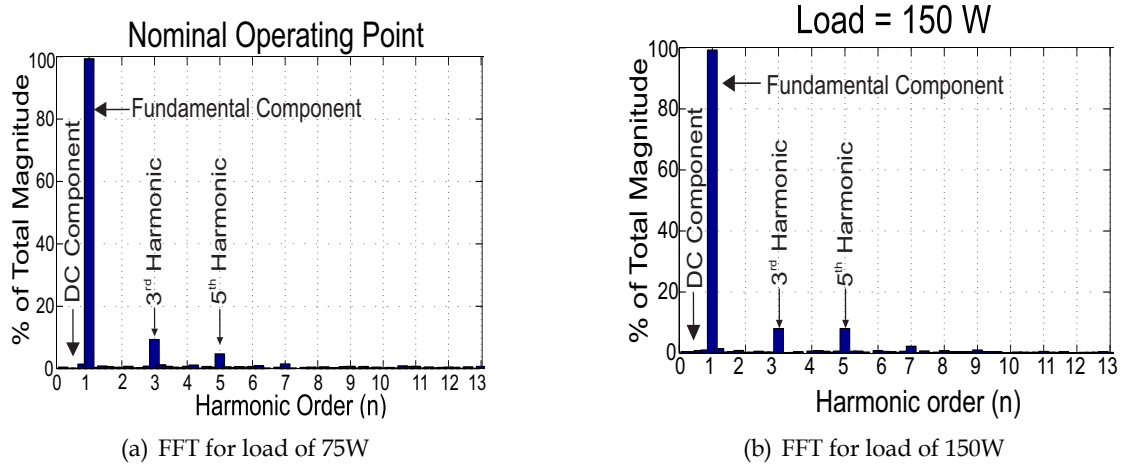


Figure 4.14 : Harmonic spectrum of the input current for the two loads of Test Case-I

4.5.2 Test Case-II: Response to Line Variation

The robustness of the proposed controller to line variation is shown in Fig. 4.15. A transition in input voltage, from 100 V to 80 V is made using variac, with all other parameters kept to their nominal values. The aforementioned oscilloscope capture presents the waveform for V_1 , I_L , and V_o over the time it took to change the voltage manually. The zoomed in waveform are also shown in the same figure, for the before and after case of the variation. The channels have been set to 100 V/div for V_o , 40 V/div for V_{in} , and 200 mA/div for I_L .

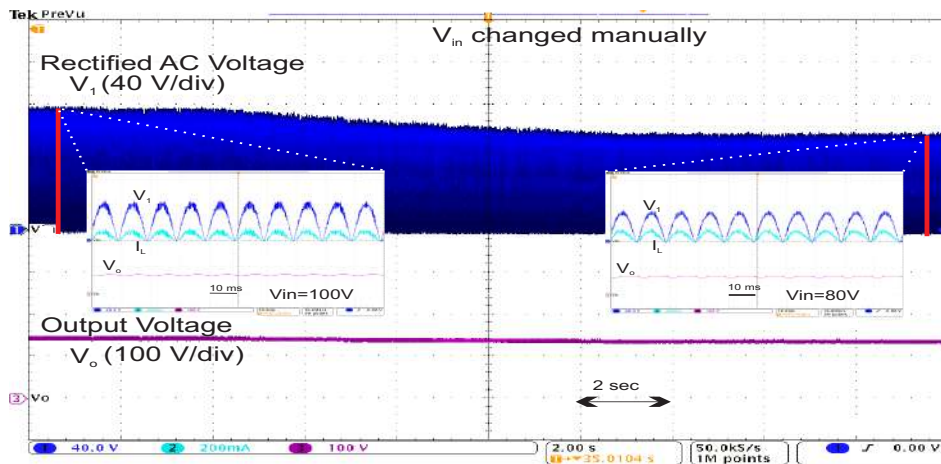
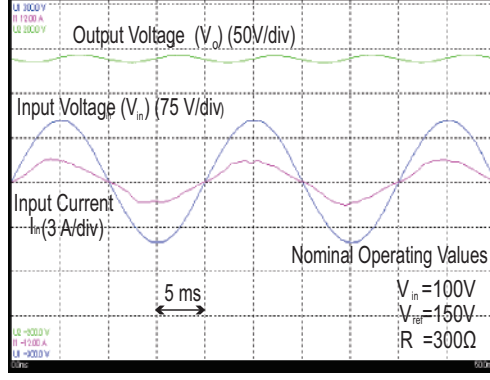
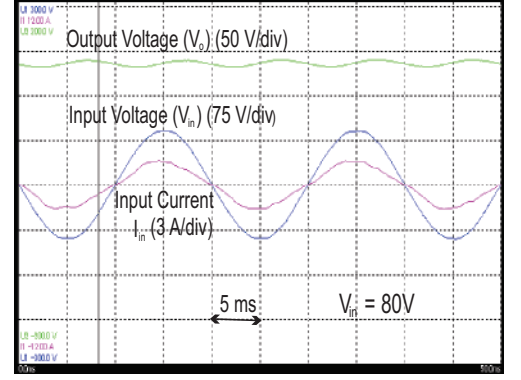


Figure 4.15 : Response of ASLFR based controller to Test Case-II. CH1: Rectified AC Input Voltage V_1 (40 V/div). CH2: Inductor Current I_L (200 mA/div). CH3: output capacitor voltage V_o (100 V/div). Load Resistance 300Ω and V_{ref} 150 V.

The corresponding waveform for V_{in} , I_{in} , and V_o are presented in Fig. 4.16, for the nominal case of $V_{in} = 100$ V and for $V_{in} = 80$ V. The captured screen settings are same as that for Test Case-I.



(a) Input Voltage 100V



(b) Input Voltage 80V

Figure 4.16 : Input Current, Input Voltage and Output Voltage waveform for Test Case-II

From the above results it can be seen that, for a decrement in the input voltage, the controller responds by changing its emulated input resistance, causing a rise in input current, so as to meet the required power demand while maintaining the voltage regulation.

4.5.3 Test Case-III: Response to change in Reference Output Voltage

The system response to a change in reference output voltage, from 150 V to 120 V, is demonstrated in Fig. 4.17. The oscilloscope capture shows the waveform for V_1 , I_L , and V_o . The channels have been set to 100 V/div for V_o , 40 V/div for V_1 , and 200 mA/div for I_L .

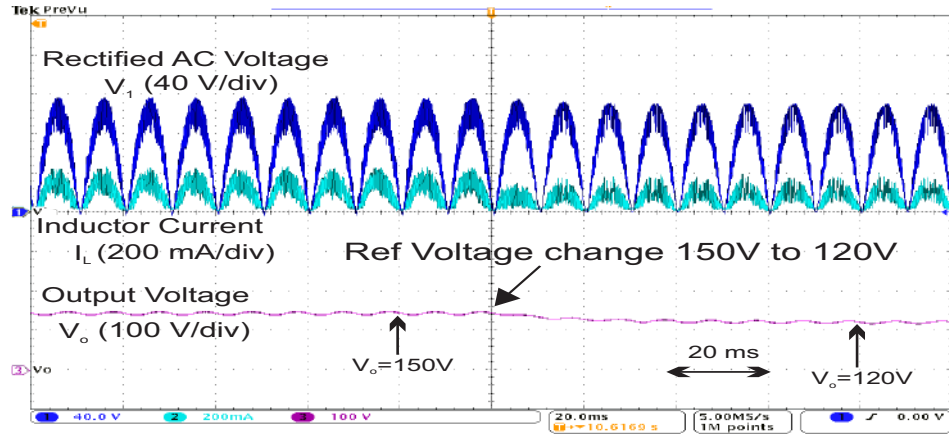
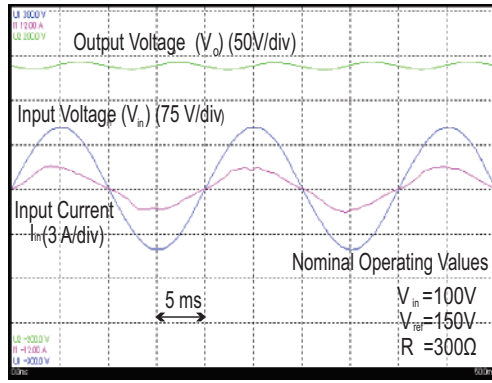


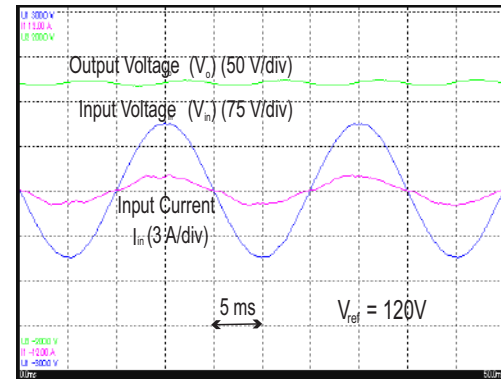
Figure 4.17 : Response of ASLFR based controller to Test Case-III. CH1: Rectified AC Input Voltage V_1 (40 V/div). CH2: Inductor Current I_L (200 mA/div). CH3: output capacitor voltage V_o (100 V/div). Time base 20 ms/div. Load Resistance 300 Ω and V_{in} 100 V.

The corresponding waveform for V_{in} , I_{in} , and V_o are presented, in Fig. 4.18, for the nominal case of $V_{ref} = 150V$ and for $V_{ref} = 120V$. The captured screen settings are same as that for Test Case-I. The proposed ASLFR based controller reacts to the new output voltage demand fast and reaches the new operating point while fulfilling the goal of PFC.

Thus, from the variety of test cases conducted experimentally, the effectiveness of the pro-



(a) Reference Voltage 150V



(b) Reference Voltage 120V

Figure 4.18 : Input Current, Input Voltage and Output Voltage waveform for Test Case-III

posed ASLFR based controller is established. It is robust to the load and line variations and provides excellent dynamic performance in maintaining output voltage as well in providing better quality power.

4.5.4 Harmonic Analysis

This section provides the distortion data for input current, in form of 3^{rd} harmonic, under various operating conditions during the experiment. Please note that the work in this Chapter has been proposed in light of IEC 61000-3-2:2014 [IECLimits, 2014]. The aforementioned regulation deals with the equipment working with input power exceeding 75 W and categorizes them into 4 classes. Each class is assigned different limits for harmonics ranging from 2^{nd} to 39^{th} . Amongst all the classes the regulatory limits are the strictest for Class D. Therefore, if the measured current harmonics of any equipment (irrespective of the class) falls within these limits then the system will surely comply with the regulation. In line with the above aim, a comparative bar graph showing the observed and the permissible 3^{rd} harmonic content for Class D equipment as per IEC 61000-3-2:2014 [IECLimits, 2014] is given in Fig. 4.19.

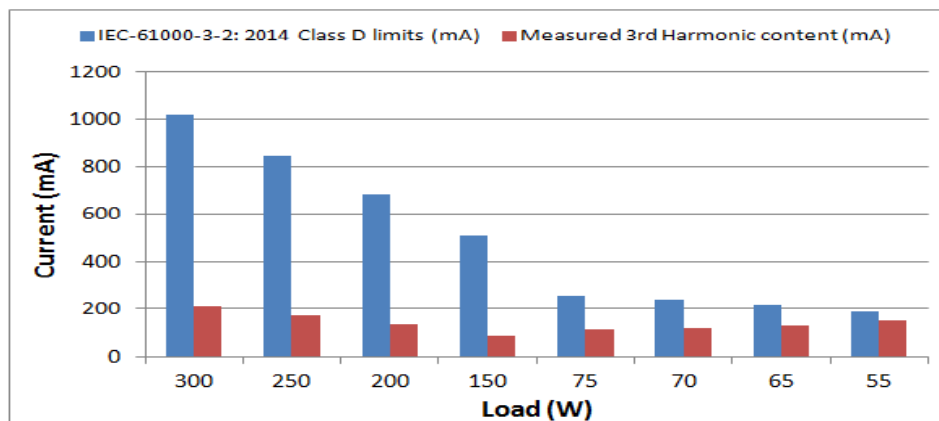


Figure 4.19 : Permissible and measured 3^{rd} Harmonic current at different load operating points.

It is shown that the currents are well within limits and thus comply with the set regulatory standards as per IEC 61000-3-2:2014. Moreover, these regulatory standards deal with system

working at or above 75 W, as the distortion current magnitudes are small enough to be neglected. Thus, the distortion at low loads is not paid special attention. However, please note that even though the distortions are within limit, it was noted that the current was forced to follow the input voltage which itself was distorted due to the use of an isolation transformer followed by an autotransformer, connected to the grid, for the input AC voltage. The high inductances of these transformers make the supplied input voltage wave flat at the top. Secondly, they are also higher due to the sampling and computational delay introduced in the digital implementation and could be improved by using a first order predictor on computed control [Rao *et al.*, 2008].

4.6 EVENT-TRIGGERED IMPLEMENTATION OF ASLFR

The ASLFR discussed in the earlier sections of the chapter has been implemented using the event-triggered scheme. The proposed ASLFR scheme has a tuning parameter α which directs the trade-off between the dual aims of power factor correction and voltage regulation. Furthermore, the event-based implementation of ASLFR allows the flexible wave shaping of the input current as per the IEC 61000-3-2 guidelines, at reduced switching actions.

The memory based triggering condition for the PFC application is

$$|e| \leq \sigma|x| \quad (4.37)$$

Here, the error term is defined as $e = x(t_i) - x(t)$, wherein $x(t) = i_L(t)$. Until the condition (4.37) is breached, the states are not updated to their current values and thereby, the switching surface (4.11c) is not updated and hence, the control law given in (4.15), is held, to its previous value. The results pertaining to the adoption of Event-triggered ASLFR is presented in this section.

4.6.1 Classical v/s ETSMC

This section draws comparison between the Classical implementation of ASLFR and Event-triggered ASLFR. The system specification are kept same as in Table 4.1. For a nominal load of 150W, a switch is made in σ value from 0 to 0.2. The corresponding system response waveforms are shown below.

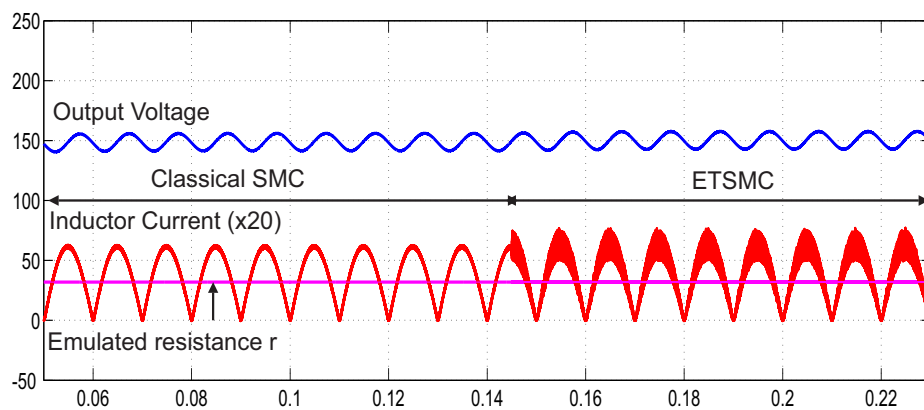


Figure 4.20 : Single stage Power factor correction for Classical and Event-triggered ASLFR.

In Fig. 4.20, when a switch is made from 0 to 0.2, the input current for the ETSMC case gets distorted. In both the cases, output voltage stays regulated to its reference value of 150 V. The corresponding Switching pulses zoomed in for the two cases is presented in Fig. 4.21. As shown,

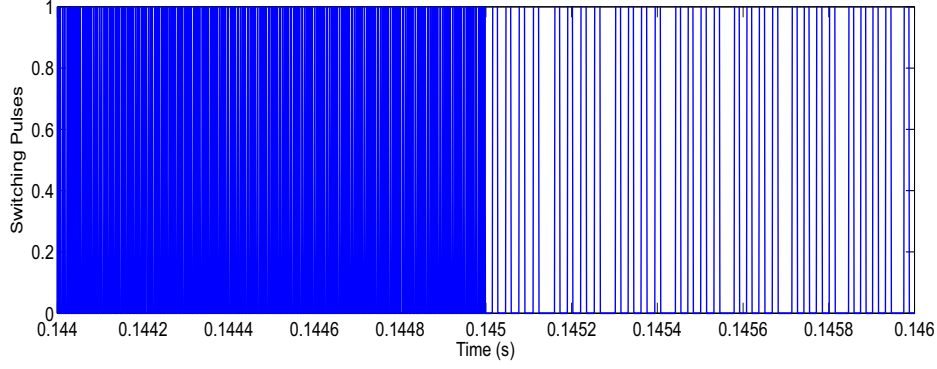


Figure 4.21 : Switching Pulses corresponding to σ change.

in ETSMC the switching is reduced by a great extent, for a "degradation" in the current quality. This trade-off between the performance and efficiency is made possible by the user defined design parameter σ .

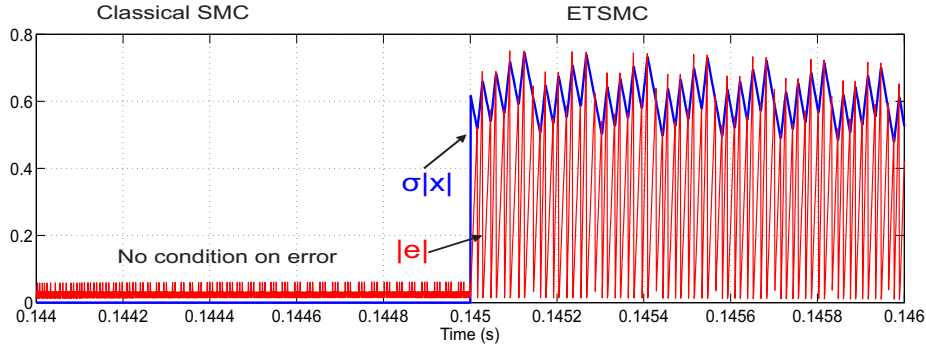


Figure 4.22 : Evolution of error for Classical and Event-triggered ASLFR.

In Fig. 4.22, the evolution of error dynamics for the two cases is presented. As $\sigma = 0$ implies $|e| \leq 0$ means there is no condition for error dynamics in Classical implementation of ASLFR and every sampling instant is an event. However, due to non-ideality of the SMC, the error is not zero for this case. For the ETSMC case, the crossing of the bound $\sigma|X|$ (in blue) by the error (in red) is marked by an event. For the time taken by the error dynamics to cross the boundary of $\sigma|x|$, the control is held to its previous state.

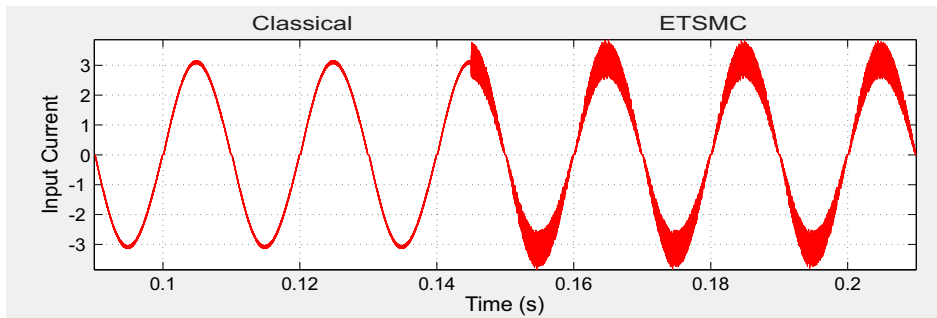


Figure 4.23 : Input Current for the two cases.

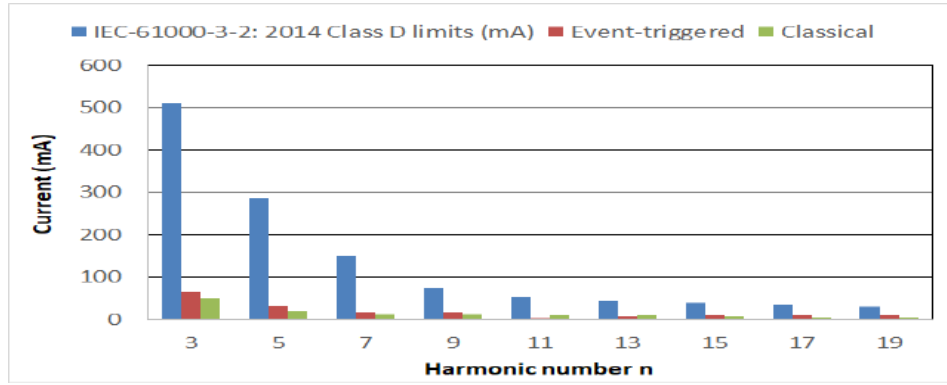


Figure 4.24 : Permissible and measured Harmonic current for 150 W load.

The input current for the two cases is presented in Fig. 4.23. The current quality for the event-triggered case is "degraded", depending on the choice of σ . The parameter σ is chosen such that the harmonic content of the "degraded" current still remains within the permissible limits as per the IEC 61000-3-2 guidelines for Class D equipments. The permissible and measured currents at different harmonic orders for 150 W load is presented in Fig. 4.24. The measured values are way below the permissible limits for all harmonic orders in both the cases.

4.6.2 ETSMC and Load Variation

In this section, the event-triggered implementation of the ASLFR is discussed under load variation. In Fig. 4.25, system response for a load change from 150 W to 75 W with $\sigma = 0.2$ is presented.

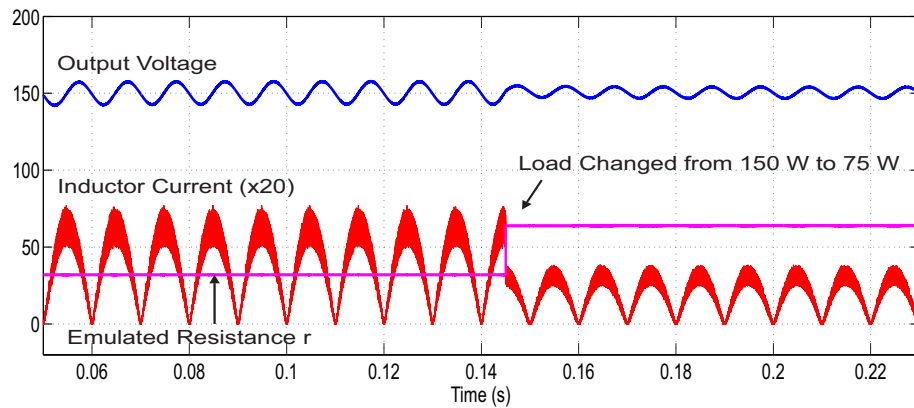


Figure 4.25 : Event-triggered ASLFR adoption at different load levels.

As seen in Fig. 4.25, even with the load change, the voltage stays regulated to its reference value and the system maintains the performance instantly. At all load levels, the distortion is within limits. Fig. 4.26 presents the measured 3rd harmonic and the permissible limits under IEC 61000-3-2:2014 Class D regulations.

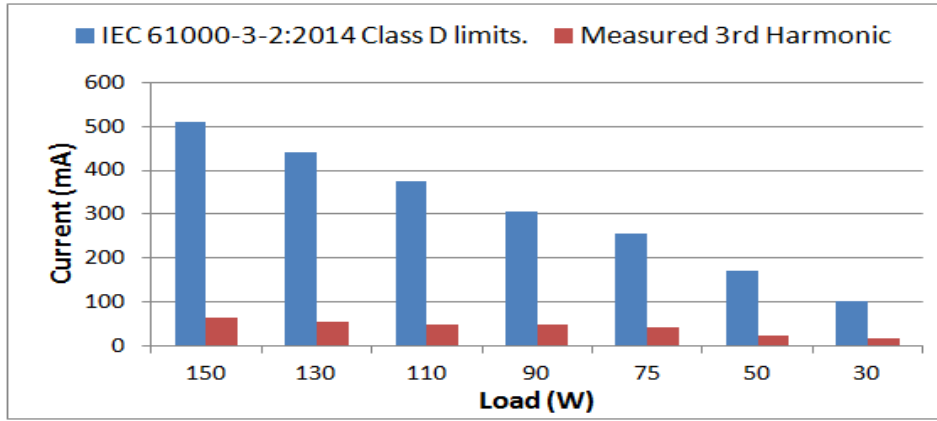


Figure 4.26 : Permissible and measured 3rd harmonic at different load conditions.

4.7 SUMMARY

In this Chapter, a novel concept of adaptive LFR controller for current shaping at the front end of a single-stage single phase PFC with high dynamic performance is proposed. The scheme gives a voltage regulation feature to the pre-regulator PFC, proposed using the existing SLFR technique in Chapter 3, to accommodate any variations in the system parameters and still maintain the required performance. The emulated input resistance adapts itself dynamically to any change in line or load conditions and the controller ensures the system performance recovery within a single sinusoidal cycle. A collection of simulation results are provided to validate the effectiveness of the adopted novel scheme over the existing SLFR based controller and the most commonly adopted dual-loop PI control for single-stage PFC solution. For a 50% load change, the PI controller takes 150 ms for voltage recovery with about -13% undershoot, on the other hand the proposed controller recovers the voltage within a single cycle with effectively no undershoot. The quality of input current for the proposed controller is better than the SLFR based work at higher loads and is quite high as compared to the PI one. Experimental results replicate the simulation outcomes, confirming the accuracy and efficacy of the proposal, under various operational settings. Then on, Event triggered implementation of the scheme was discussed. The ETSMC allowed for the flexible wave shaping of the input current, while regulating the output voltage. The harmonic content was always within the prescribed limits for Class D regulations for a reduced switching actions.

In this Chapter, the application was for single-phase appliances falling under Class D category. However, all high power equipment derive power from three-phase mains, hence active three-phase PFC converter is required to reduce line current harmonics. In the next Chapter, the concept of ASLFR is explored for three-phase balanced applications, categorized as Class A equipments. Loss free resistor emulation for a modular three-phase power-factor correction circuit (PFC) using isolated single-phase Ćuk converters, operating in continuous-current mode, will be discussed in the next Chapter.