Abstract

Advancements in very large-scale integration (VLSI) technologies across the generations have made it possible to develop high-performance, multifunctional, low-power, and compact electronic systems to cater to the increasing demands of the present-day market. A high performance electronic system consists of various components; apart from different Integrated Circuits (ICs) (on-chip circuits) and interconnects, it contains various off-chip components, such as power supply modules, boards, packages, etc. An IC may contain millions of transistors per unit area, which has been possible due to the continuous downscaling of the size of transistors. This downscaling has resulted in a substantial decrease in voltage levels, which in turn has led to a considerable reduction in noise margins. With narrower noise margins, transistors have become more susceptible to noise. Also, in modern high-speed systems, operating frequencies can attain values up to tens of GHz. Considering this reduction in voltage levels, reduction of noise margins, and higher switching speeds, one of the most challenging tasks for the system designers is to ensure the integrity of signal and power at nano-scale technologies. Moreover, the large amount of current flowing through the interconnects, along with reduced voltage levels, may cause a substantial impact on signal integrity (SI) and power integrity (PI). SI focuses on maintaining the quality of the signal, ensuring that the data transmitted from the sender end are accurately received at the receiver end. On the other hand, PI is concerned with maintaining the quality of power supply, ensuring that sufficient current is provided to all the components and enabling them to perform reliably. Any noise source in the circuit or poor signal quality creates various issues related to SI and PI, such as jitter, crosstalk, variations in transition levels (high and low) of signal at the output, and intersymbol interference (ISI) that can further impact the performance of the entire system severely.

The mismatch in the drain current of switching devices of same dimensions also increases with continuous reduction in the size of transistors. The leading cause of this mismatch is due to the inaccuracies in fabrication process. These limitations can result in mismatch between the intended and the measured dimensions of the semiconductor devices. Such a scenario creates significant variability concerns for VLSI circuit designers, and consequently, the performance of the ICs degrades at high frequencies. The performance of an IC is mainly influenced by two factors: one is environmental factors (such as temperature and humidity) and another one is physical limitations during the fabrication process (such as variations in oxide thickness and variations in length and width of the transistors). The combination of these environmental factors and physical limitations of the fabrication process introduces variability-related problems in ICs. That can further lead to stochastic variations in the output response, such as timing deviations in the transition edges and change in the voltage levels (high and low) of the output response of the IC.

In addition to these variability issues, presence of various noise sources can seriously affect the performance of the system. Problems arising due to variability can become even worse due to the presence of various noise sources, such as power supply noise (PSN) and ground-bounce noise (GBN), leading to poor performance of the system. Therefore, it is imperative to thoroughly investigate and analyse the performance of circuits during pre-silicon analysis so that potential risks can be identified and mitigated before they impact the performance of the entire system. Considering the above-stated challenges, this work performs a comprehensive study on the analysis of jitter in VLSI circuits. It employs both analytical and semi-analytical modeling approaches for analyzing deterministic jitter, considering several case studies.

Initially, an analytical approach to estimate deterministic jitter is proposed. Considering a CMOS inverter as a case study, the relationship between input and output is derived considering the effect of deterministic noise sources such as PSN, Data Noise (DN), and GBN in the circuit.

The expression for jitter is obtained analytically by evaluating the deviation of each transition edge from its ideal position.

Next, variability-aware modeling of jitter has been proposed. It performs a comprehensive study on the impact of variability on jitter in CMOS integrated circuits. The analytical expressions are further advanced, and the input-output relationship is derived considering the effect of PSN, variations in design parameters due to variability issues, and temperature. These parameters are considered as random variables, and the timing deviation in the transition edges of the output response is evaluated analytically. Several examples (simulations as well as measurements) are presented to validate the proposed model. These examples include comparison of the analytical results with the simulation results obtained using an Electronic Design Automation (EDA) tool and the same with the experimental results using two different commercially available CMOS inverter ICs.

Next, semi-analytical approach has been proposed to estimate PSN and GBN-induced jitter for a voltage-mode driver (VMD) circuit driving long transmission lines. Considering the spatial and temporal components of long transmission lines, a semi-analytical expression of the differential output response of VMD is obtained. Slope-based method is used to estimate jitter at the differential output of VMD. This method requires only one-bit simulation for the estimation of jitter. Furthermore, a comprehensive study on variability-aware modeling of PSN-induced jitter (PSIJ) in VMD circuit driving long transmission lines is presented.

The final part of this work, presents a novel observation on PSN and GBN-induced jitter in a chain of CMOS inverters. The proposed approach uses semi-analytical expressions to estimate jitter based on small-signal noise transfer function for Nth inverter stage. This work also uses slope-based jitter estimation techniques. The total estimated jitter exhibits a zig-zag pattern with the number of stages. When only one noise source, either PSN or GBN, is present in the circuit, this pattern resembles an increasing or decreasing staircase-like trend as the number of stages increases. However, when PSN and GBN are simultaneously present, the jitter maintains a uniform zig-zag pattern across stages. These observations are validated by comparing the results obtained from the semi-analytical approach and EDA tool, as well as the measurement setup.