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Hot Injection-Based Synthesized Colloidal CdSe Quantum Dots Embedded in Poly(4-vinyl pyridine) (PVP) Matrix Form a Nanoscale Heterostructure for a High On–Off Ratio Memory-Switching Device

Chalcogenide-based quantum dots are useful for the application of memory-switching devices because of the control in the trap states in the materials. The control in the trap states can be achieved using a hot-injection colloidal synthesis method that produces temperature-dependent size-variable quantum dots. In addition to this, the formation of a nanoscale heterostructure with an insulating material adds to the charge-trapped switching mechanism. This work shows that the colloidal monodispersed CdSe quantum dots and poly(4-vinyl pyridine) (PVP) formed a nanoscale heterostructure between themselves when taken in a suitable ratio to fabricate a device. This heterostructure helps realize memory-switching in the device with a maximum I_{ON}/I_{OFF} of 10^5. The switching in the device is mainly due to the trap states in the CdSe quantum dots. The conduction in the off state is due to thermal charge injection and space charge limited conduction and in the on state, due to the Ohmic conduction mechanism. The current chapter describes the synthesis and characterization of colloidal CdSe QDs and the fabrication of a high-performance resistive memory switching device using QDs-PVP nanocomposite sandwiched between Al and ITO electrodes.

3.1 Introduction

The demand for a huge amount of space for storing information leads to the development of new technology. Another factor that adds to this is the demand for increased processing speed of computer processors [Geer, 2005]. Traditionally, computer processors are built using silicon technology, but the bottleneck of scaling down the device further halts development [Schulz, 1999]. There are various alternate technologies that challenge the development of silicon-based memory devices. Some of these technologies are based on oxide materials [Chen et al., 2013], organic molecules [Li et al., 2010a], polymers [Liu et al., 2012b], and quantum dots (QDs) (Geller et al. 2008), to name a few. All of these materials have positive and negative implications. For example, oxide material-based devices have shown a high on−off ratio, but the oxides are grown using the atomic layer deposition (ALD) growth method, which is not economically viable. Also, oxide-based memristors lack control over the filament formation and external switching voltages [Han et al., 2017; Sangwan et al., 2015]. Similarly, organic molecule and polymer-based devices are cost-effective and substrate-independent, which means that the devices can be fabricated on flexible substrates as well. But the devices are relatively less stable as they are prone to various environmental factors [Selzer et al., 2005]. Quantum dot-based devices are a middle ground in which the quantum dots have a more inorganic part than organic molecules, as the organic molecules are used only to stabilize the quantum dots and can be removed using a liquid- or solid-state transfer process. Moreover, their small size leads to changes in physical properties, which are essential in tuning the electrical parameters of the device [Alivisatos, 1996].

Quantum dots are used nowadays for many different types of device applications such as optoelectronic devices, namely, solar cells [Nozik, 2002], LEDs [Caruge et al., 2008], photodetectors [Konstantatos et al., 2006], thin-film transistors [Kang et al., 2009], and sensors [Liu et al., 2014]. Memory-switching devices are no exceptions. These devices have been fabricated using different types of semiconductor quantum dots [Kannan et al., 2013, 2016b; Kouklin et al., 2000; Sahu et al., 2007], quantum dots and polymer composites [Chen et al., 2008; Son et al., 2009] semiconductor nanoparticles [Mohanta et al., 2006], metallic nanoparticles [Chang et al., 2013; Prakash et al., 2006], transition metal dichalcogenides (TMDCs) [Bok et al., 2017; Han et al., 2017; Kim et al., 2017; Mao et al., 2020; Qi et al., 2018; Tan et al., 2015; Wang et al., 2017], and perovskite quantum dots and nanoparticles [An et al. 2018; Chen et al. 2019b, a; Ercan et al. 2017] Among the chalcogenide quantum dots, CdSe is the most widely used quantum dot in memory-switching devices. It has been used in a transistor configuration and has shown memory effects both electrically and optically [Fischbein et al., 2005]. Charge confinement in CdSe nanoparticles leads to the switching behavior, and the conduction mechanism during the operation of the device changes from injection limited to bulk conduction [Mohanta et al., 2006]. Charge trapping in the CdSe quantum dot along with a Coulomb blockade due to the presence of various types of metal oxide layers gives rise to high speed [Kannan et al., 2016a], consistent switching but with a smaller on−off ratio [Kannan et al., 2011b][Kannan et al., 2012]. This has shown negative differential resistance as well. In a QD, the metal−metal oxide and the QD device configuration increased the on−off ratio by one order and the devices worked fast [Kannan et al., 2011a, 2011c]. A combination of conducting small organic molecules and polymer with CdSe or a core−shell quantum dot formed a heterojunction that led to switching in the device [Shin et al., 2012][Kannan et al., 2010][Ma et al., 2016]. These composites on a flexible surface form a synaptic device architecture that can work as a neural network [Koo et al., 2019], and this is mainly due to the charge trapping in the quantum dots [Chen et al., 2020b]. Here, in this work, we have used a composite of poly(4-vinyl pyridine) (PVP) along with colloidal CdSe quantum dots synthesized using the hot-injection method to fabricate the memory-switching device. In this way, we have created a nanoscale heterostructure that shows switching behavior due to the trapping of charge carriers and because of which a maximum I_{ON}/I_{OFF} of 10^5 is obtained from the switching device. It is interesting that a nanoscale heterostructure is the reason for the switching in the devices under test.

3.2 Experimental Section

In this section, the detailed synthesis procedure of materials with the used chemical list and the device fabrication process have been discussed.

3.2.1 List of Chemicals Used

Cadmium oxide (CdO) (≥ 99.99% trace metal basis, Sigma Aldrich), Selenium powder (Se) (99.99% trace metal basis, Sigma Aldrich), 1-octadecene (ODE) (technical grade, 90%, Sigma Aldrich), oleic acid (OA) (≥ 99%, Sigma Aldrich), Poly(4-vinyl pyridine) (PVP, M.W. ~ 60,000, Sigma Aldrich), hydrochloric acid (HCl) (ACS reagent 37%, Sigma Aldrich), zinc dust (≥ 99.99%, Sigma Aldrich), acetone, toluene, octane and chloroform were used. All the chemicals were used without further purification.

3.2.2 Synthesis of the CdSe Quantum Dots

For the synthesis of CdSe QDs, we followed the colloidal hot injection-based method [Nozik, 2002]. For this, two precursor solutions were prepared, i.e., cadmium oleate and selenium (Se) precursors. For the preparation of the cadmium oleate precursor, 0.5 mmol of CdO was taken in a three-neck round-bottom flask in which 3.2 mL of OA and 20 mL of ODE were added. A temperature probe is inserted through the septa cap inside the flask to continuously monitor the reaction temperature. The reaction flask was then evacuated using a vacuum pump in a standard schlenk line for 30 minutes. It is important to check carefully such that there is no leakage. If any leakage is present in the septa cap, the CdO will not be completely dissolved in the ODE and OA solution. The flask was then heated with continuous stirring using a magnetic stirrer hotplate at

95 °C in a vacuum for 1 h while continuously stirring the solution. After 1 h, the reaction flask was purged with dry N_2 gas using the schlenk line setup. The reaction was then carried out in an N_2 environment at 140 °C and kept at this temperature for 16 h to obtain a clear yellowish cadmium oleate solution. The clear solution indicates the complete dissolution of CdO in ODE in the presence of OA and the formation of cadmium oleate solution. For the Se precursor, a solution of selenium powder (21.7 mg), ODE (2 mL), and oleic acid (1.2 mL) was prepared and sonicated for 2 h to obtain a homogeneous solution. The temperature of the cadmium oleate solution was further increased to 225 °C. When the temperature reached the desired set value and became stable for a few minutes, the Se precursor was injected rapidly within 2−3 s. Immediately, the temperature of the source was turned off and was left to cool to RT. A change in the color of the solution was noticed. The yellow transparent solution became reddish just after the injection. This process is known as nucleation, which results in the formation of CdSe quantum dots. But, for monodispersed and uniform size distribution of the quantum dots, there should be control over the rapid growth of quantum dots, and for this reason, long-chain hydrocarbons are used as a capping agent. In our case, oleic acid is used as a surfactant molecule. When the reaction bath is cooled to 27 °C, 10 mL of acetone was added to the reaction bath to precipitate the quantum dots. The crude solution was then transferred equally into eight test tubes and acetone was added to each test tube. The test tubes were then shaken in a vortex shaker for better mixing. This solution was then transferred into the centrifuge tubes and centrifuged at 4500 rpm for 5 min to obtain a reddish CdSe powder. After drying under a nitrogen flow, the reddish oleic acid-capped CdSe quantum dots were redispersed in octane for various characterizations and some amount was dispersed in toluene for further use in device fabrication. The synthesis process used in this work is shown in Figure 3.1.

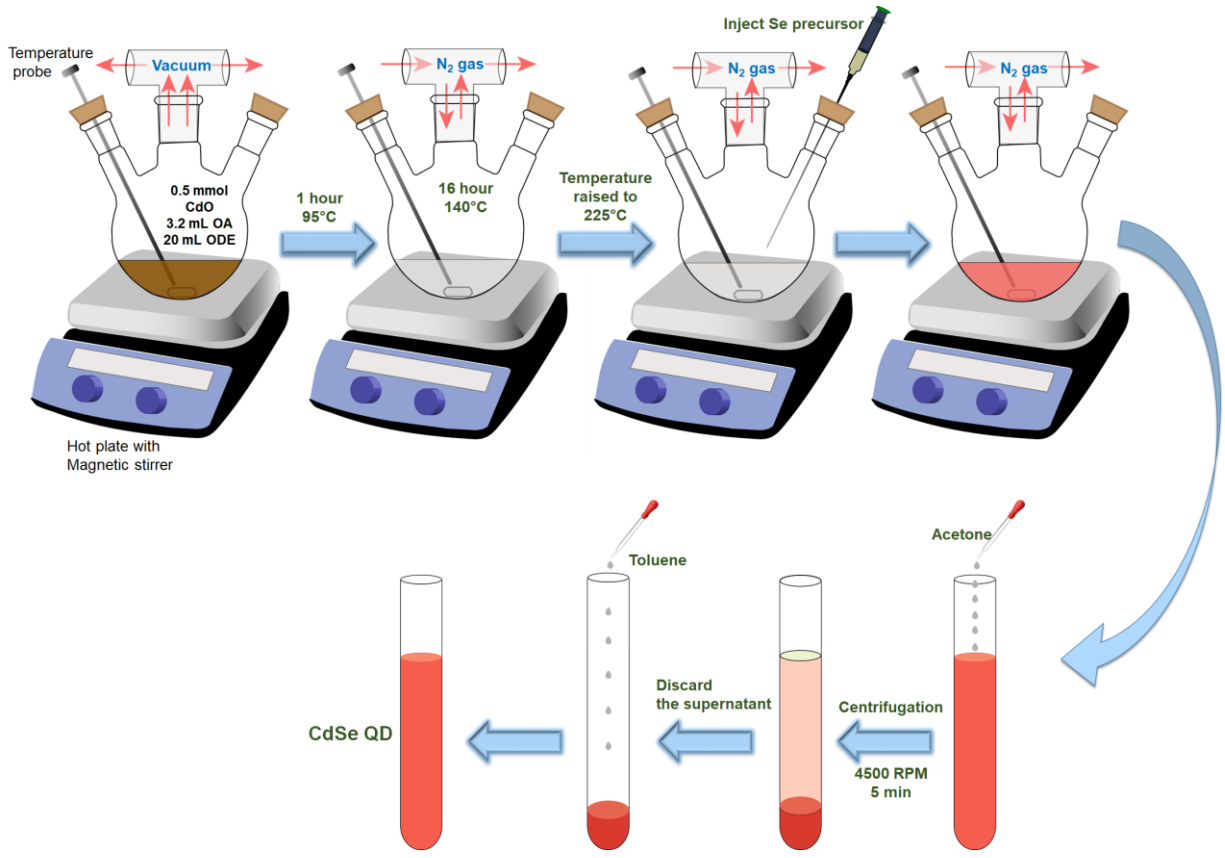

Figure 3.1: Synthesis procedure of colloidal CdSe QDs using the hot injection method. The injection temperature was 225 °C. The CdSe QDs were precipitated using acetone.

3.2.3 Device Fabrication

To fabricate the device, at first, ITOs were etched from an ITO-coated glass substrate using Zn dust and concentrated HCl to make a sharp strip of ITO in the middle of the substrate, which

acts as the bottom electrode. The thickness of the ITO strip used for the device fabrication is 150 nm. The etched substrates were cleaned by ultrasonication using acetone and methanol each for 20 min and then thoroughly cleaned using deionized water. Then, the cleaned ITOs were dried in an inert atmosphere. For device fabrication, acetone was added to the stock solution of CdSe QD in toluene to precipitate the QDs and redispersed in chloroform. For preparing the CdSe-PVP composite, PVP was added to the CdSe QD solution in chloroform by a weight ratio of PVP and CdSe of 3:4, where PVP acts as a matrix for CdSe QDs. The CdSe-PVP composite in chloroform was spin-coated at 2000 rpm onto the ITO-coated glass substrates and kept on a hotplate at 70 °C for 30 minutes prior to the top Al electrode deposition. Briefly, 70 nm thick aluminum was deposited as the top electrode through a shadow mask by thermal evaporation at a pressure of 5×10^{-6} Torr. This constitutes a device having an effective area of 5 mm^2. The schematic of the device structure is shown in Figure 3.2a (only QDs without PVP) and Figure 3.2b (QDs-PVP composite).

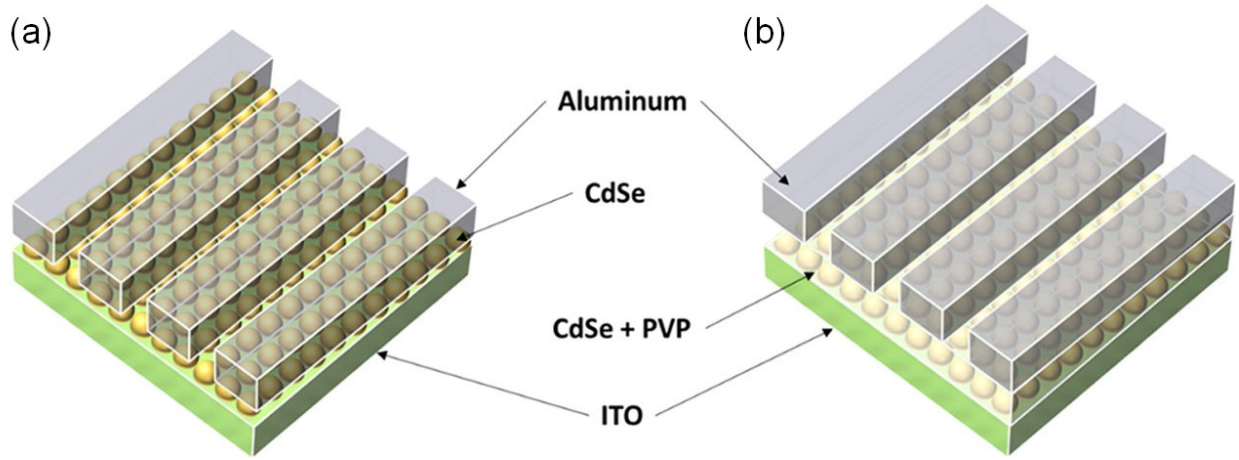

Figure 3.2: (a) Device architecture of only CdSe-based device where CdSe is sandwiched between the top aluminum and bottom ITO contacts. (b) The architecture of the device where the active material is a composite of CdSe QDs and PVP sandwiched between the upper Al and lower ITO contacts.

3.3 Results and Discussion

In this section, the results from materials characterizations and device characterizations have been discussed and analyzed.

3.3.1 Characterizations of Materials

The absorption spectra were recorded using a Varian Cary 4000 UV−vis spectrophotometer. The CdSe QDs dispersed in octane were filled in a quartz cuvette and another cuvette filled with pure octane for absorption spectra measurement. The absorption spectra of the quantum dot synthesized at 225 °C are shown in Figure 3.3a. A sharp absorption peak is observed at 523 nm, indicating the high-quality monodispersed nature of CdSe QDs. Using the Tauc plot, we have extracted information about the direct band gap [Muhammad et al., 2020; Pankove, 1975] of the quantum dot. In Figure 3.3a inset figure shows the $(\alpha h\nu)^2$ vs $h\nu$ graph and when we extrapolated the tangent to the peak, the band gap was found to be 2.28 eV.

The X-ray diffraction (XRD) study for the quantum dots is performed using a Bruker AXS model (D8 Advance) X-ray diffractometer. For XRD measurement, the CdSe QDs dispersed in octane were dropped and cast on a clean glass substrate. When the solvent evaporated at room temperature, the substrate was heated at 70 °C on a hotplate for 30 min. Thus a thin film of CdSe Qds on a glass substrate is formed. The smoothened X-ray diffraction image in Figure 3.3b shows the three peaks for (111), (220), and (311) planes, which confirms the zinc blend structure of the

CdSe quantum dots, according to JCPDS file No. 19-0191. It shows much wider peaks as the quantum dots are periodic on a small scale.

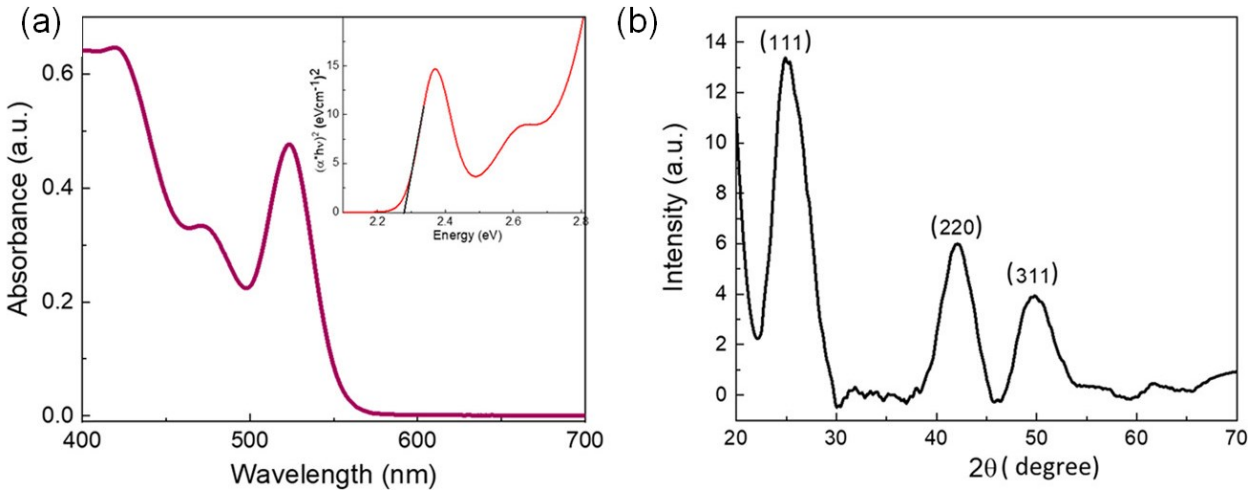

Figure 3.3: (a) Absorption spectra of CdSe quantum dot synthesized at 225 °C. A sharp absorption peak was observed at 523 nm. The inset shows the Tauc plot where the slope to the first peak and the band gap is the value corresponding to the intersection of the tangent (black line) and energy axis. (b) XRD pattern of the CdSe sample with peaks corresponding to (111), (220), and (311) planes.

The TEM images were collected using FEI Tecnai G2 20 S-Twin with a filament operating voltage of 200kV. For HRTEM measurement, a dilute solution of CdSe QDs in toluene is dropped cast on the copper TEM grid. The HRTEM images of the quantum dots are shown in Figures 3.4a, b, and c. The images show that the quantum dots are monodispersed. The particle size distribution has been plotted and fitted by Gaussian fitting, as shown in Figure 3.4d. The average size of the quantum dots is 3.39 nm with a standard deviation of 0.52 nm. The particle size distribution perfectly follows the Gaussian distribution, as can be seen from Figure 3.4d. The energy-dispersed (EDX) spectra of the quantum dots show that the composition of the quantum dots mainly consists of elements such as Cd and Se, as shown in Figure 3.4e.

The AFM images were taken using a Park Systems XE-70 microscope in non-contact mode. The AFM image with the line profile of the quantum dots on a glass surface is shown in Figure 3.5a. This shows that the surface is fairly uniform, with a RMS roughness of 7.67 nm. As can be seen from the image, the particles are close to each other, but in some places, there are gaps between the particles and even big cracks in a few places, as shown by the white circle in Figure 3.5a. On the other hand, the surface of the film due to the composite of PVP and CdSe QDs is uniform with an RMS roughness of 1.07 nm, as shown in Figure 3.5b. Therefore, it is clearly seen that when CdSe QDs have blended with PVP, the RMS roughness decreases. Also, from the line profile of two AFM images, it can be seen that the CdSe QDs-PVP composite film has better smoothness than that of pure CdSe QDs film.

3.3.2 Device Characterizations

The synthesized QDs were used for the fabrication of two devices, as mentioned earlier. In one device, pure CdSe QDs were used and in another device, CdSe QDs-PVP composite was used as an active layer. The schematic of device structures with pure CdSe QDs and CdSe QDs-PVP composite is shown in Figure 3.2. The device characterization was performed in a vacuum using a two-probe measurement technique interfaced with a Keithley 6430 femtoampere source meter. The electrical study of the only CdSe quantum dot-based device produced I−V curves that were short and are shown in the lower inset of Figure 3.6a. This was expected as there are gaps between quantum dots that would be the percolating path for the metallic channel formed between the top and the bottom contacts after the deposition of the top metal contact. The second device with Al/CdSe QDs-PVP/ITO structure was also studied electrically.

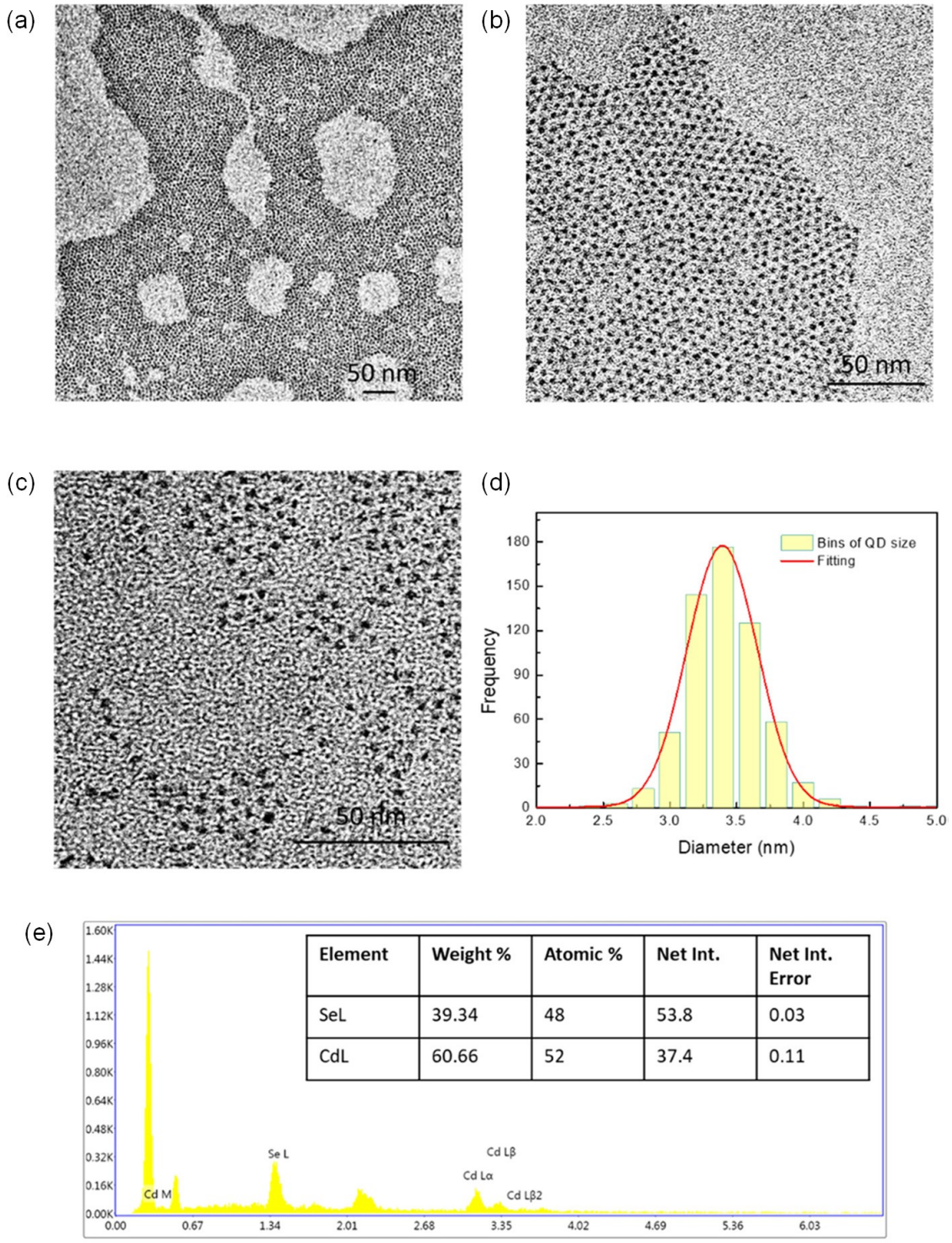

Figure 3.4: HR-TEM images of the quantum dots synthesized at 225 °C. (a), (b), and (c) represent the images for quantum dots synthesized at 225 °C. The corresponding scale bar is 50 nm. (d) Particle size distribution of the quantum dots, which fits the Gaussian distribution. (e) EDX spectra of the quantum dots show the presence of Cd and Se elements and the corresponding weight and atomic percentages.

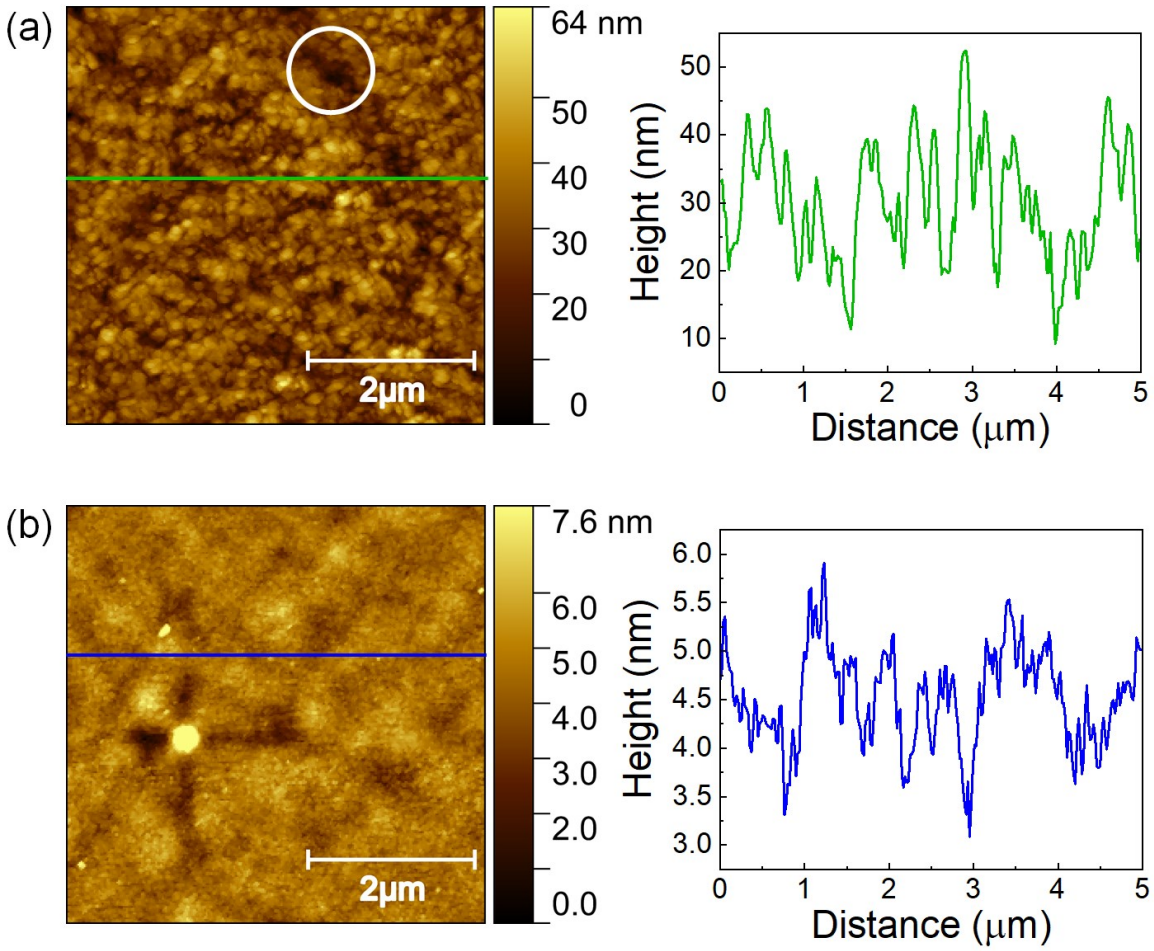

Figure 3.5: (a) AFM image of CdSe quantum dot film prepared by dispersing in toluene with a concentration of 5 mg/mL over a glass slide. The scan area is 5 μm × 5 μm with a scale bar of 2 μm. The RMS roughness from the surface is 7.67 nm. The line profile is shown on the right side. (b) AFM image of the CdSe QDs- PVP nanocomposite film over the glass surface. The scan area is 5 μm × 5 μm. The scale bar represents 2 μm. The RMS roughness from the surface is 1.07 nm. The line profile is shown on the right side.

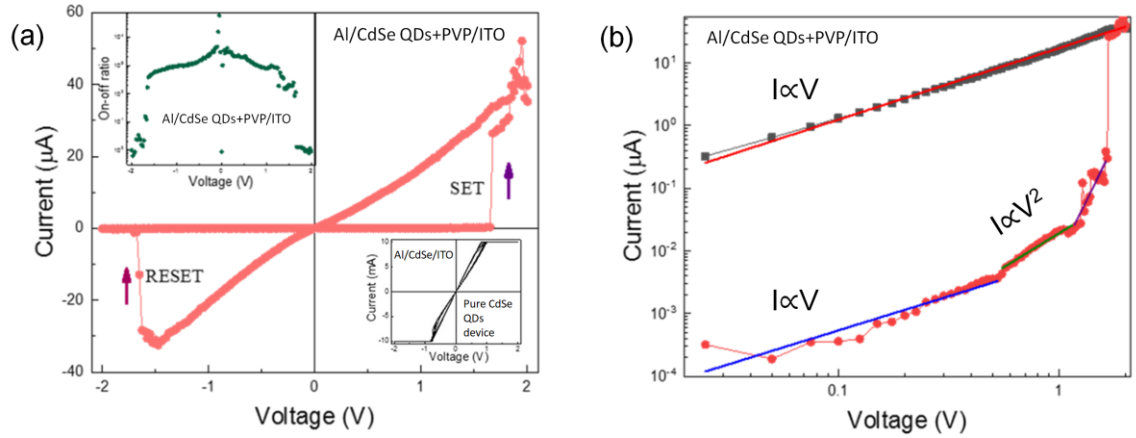

Figure 3.6: (a) *I–V* characteristic curve for the CdSe+PVP composites device scanned between −2 and 2 V in successive loops. The threshold where the current jumps from the low current to the high current state is shown by an upward arrow in the first quadrant and is called the SET condition, whereas the threshold where the current jumps from the high conducting state to the low conducting state is shown by the upward arrow in the third quadrant and is called the RESET condition. The inset shows the I_{ON}/I_{OFF} of the CdSe+PVP composites device with the highest I_{ON}/I_{OFF} of 10^5. The lower inset shows the *I–V* characteristic of the only CdSe-based device without PVP (b) The low and high conducting states of the CdSe+PVP composites device in the forward

bias plotted with both the axis in log scale are fitted. In the high conducting state, the current varies linearly, whereas the low conducting state current has multiple slopes.

For this, the device was scanned between −2 V and +2 V, as shown in Figure 3.6a, and the corresponding current values were traced out. It was observed that while scanning in the positive direction, the current jumps from a HRS to a LRS at around 1.6 V and stays in the low resistance state when the voltage was reduced and brought toward 0 V. After crossing 0 V when it was traced in the negative direction, it stayed in the LRS and at −1.7 V, it jumped to the HRS. Therefore, in the positive and negative bias direction, there is a threshold above which the conductance jumps from low to high and high to low states, respectively. The transition from the high to low resistance state is called SET (on) and the low to high resistance state is called RESET (off), which are observed in the positive and negative voltages, respectively. The highest on−off ratio for the device is 10^5 at −0.2 V, as can be seen from the figure in the upper inset of Figure 3.6a.

The I−V curve in the log scale has been fitted by a straight line, as shown in Figure 3.6b, on the positive side to obtain an idea about the transport mechanism that plays a role in the conduction of the carriers. Here, we have chosen the logarithmic scale for both axes. In the on state (high conducting state), the current varies linearly with the voltage, but for the off state, the current variation with respect to the voltage varies polynomially. Initially, it varies linearly ($I \propto V$) till 0.52 V, which suggests that the transport is due to the thermally excited free electrons that are few in number and hence the current is less. After 0.52 V, it varies with the square of the voltage ($I \propto V^2$), which implies SCLC conduction which can be expressed [SCHRYER 1989] as

$$J = \frac{9\mu\varepsilon_0\varepsilon V^2}{8d^3}$$

where μ is the charge carrier's mobility, ε is the dielectric constant of the material, ε_0 is the permittivity of free space, V is the applied voltage, and d is the sample thickness. Similar type of SCLC conduction mechanism was observed in other QDs+polymer composites based RS devices[Ma et al., 2016; Shim et al., 2011]. In the end, just before the threshold, the current varies almost exponentially for a brief period of time. After switching to the on state, the current again varies linearly with the applied voltage, which implies ohmic conduction.

To study the performance of the device and to understand the SET and RESET conditions better, we performed the random-access memory (RAM) test. Here, we studied the device current under periodic erase, read, write, and read voltage pulses. The write, read, and erase pulses are 3, 0.5, and −3 V, respectively, for 6 s each. The applied pulse variation with respect to time is shown in the bottom panel of Figure 3.7a. The current from the device at these voltages is also shown in the upper panel of the same figure. The maximum current due to the write and erase voltage varies between +6.5 and −6.5 μA, respectively. The current from the device suggests that the write and read states are stable states with less fluctuation in the read current. There is a significant difference between the read current after erase and read current after write for all the cycles. The device was studied for more than 1000 s and the figure shows a complete response. Thus, the device can be used for RAM applications. To check the retention time of the device, it was first written or erased by 3 or −3 V for 10 s and then probed by a small voltage of 0.5 V for a long time. We observed the on and off state currents without any overlay for more than 3500 s and found that the device is stable for ROM application and is shown in Figure 3.7b. To understand the operation speed of the device, a square wave of 4 Vp−p (peak to peak) and a width of 500 ns were used as an input signal, and the corresponding output across the device was observed, as shown in Figure 3.7c [Kannan et al., 2011c]. The input signal takes 12 ns to reach from 0 to 4 V, whereas the output signal took 60 ns to achieve the maximum voltage across it. Thus, it can be said that the response speed of the device is 48 ns, which is marginally less than the pristine CdSe quantum dot-based devices due to the presence of the organic insulating matrix. The endurance test was performed by applying repetitive write, read and erase cycles and recording the corresponding current in on and off state for a read voltage of 0.5 V. The stability

of the on and off state currents in more than 4000 cycles shows the excellent durability of the device, which is presented in Figure 3.7d.

3.3.3 Analysis of the Result

To understand the process of switching in the device, we need to consider the band diagram of the device, as shown in Figure 3.8a. Here, the CdSe quantum dot is embedded in the PVP layer. We assume the sandwich situation when we consider the quantum dots in the matrix of PVP, which surrounds the quantum dots from all sides. The HOMO and LUMO of PVP are known to be −5.66 and −2.42 eV, respectively, and the corresponding band gaps suggest that it is an insulator. The band gap of the CdSe quantum dot is 2.28 eV. Therefore, PVP and CdSe quantum dots form a type of nanoscale heterostructure. The work functions of ITO and Al are −4.7 and −4.3 eV, respectively. When the device was scanned in the positive bias, ITO was at a higher potential than the Al contact, and hence the Fermi levels aligned accordingly in such a way that at a particular voltage, a few electrons on the ITO side would have sufficient thermal energy to cross the potential barrier of PVP. Several studies [Ma et al., 2016; Pal et al., 2020; Wang et al., 2017] revealed that QDs act as charge trapping and de-trapping centers when they are embedded in a polymer or insulating matrix.

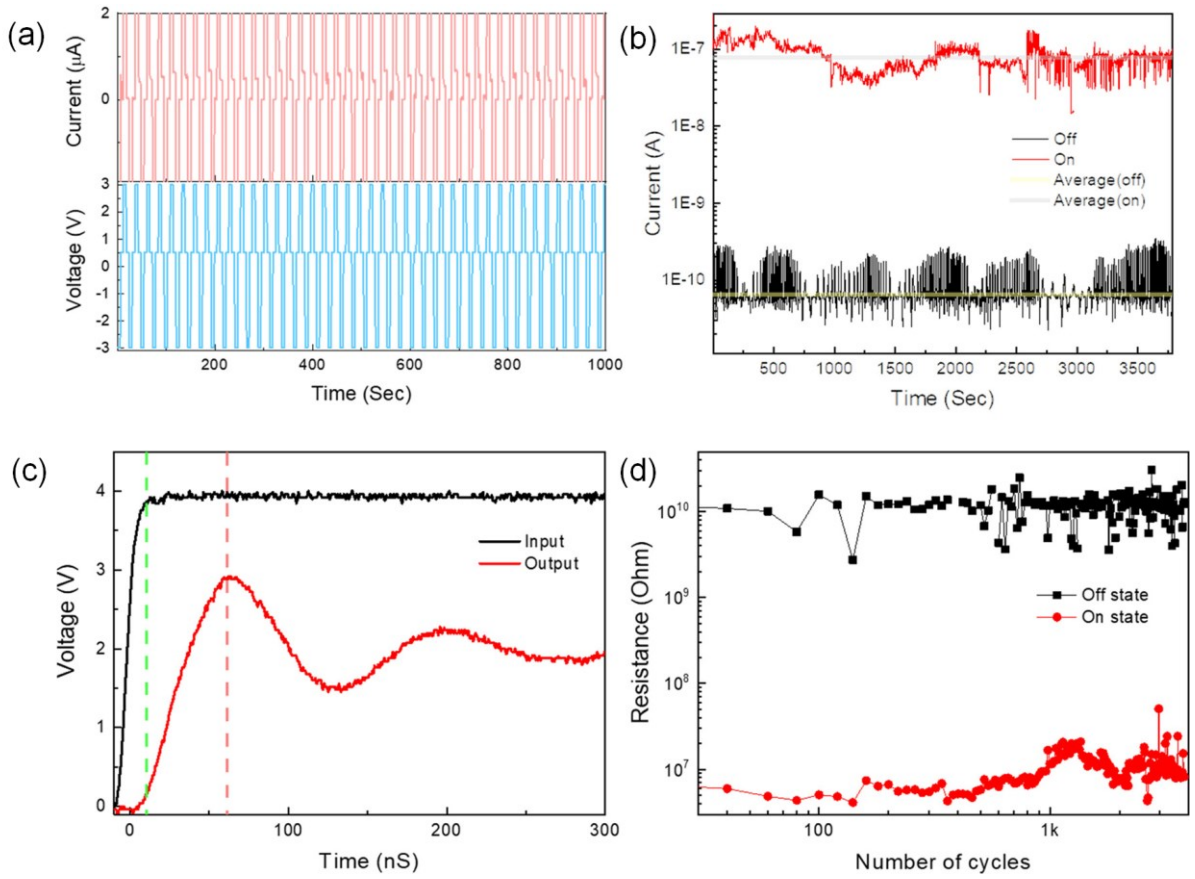

Figure 3.7: (a) Random-access memory (RAM) study was performed by writing at 3 V and erasing at −3 V and then reading the states at 0.5 V. The write, erase and read voltages were applied for 6 s each. (b) Read-only memory study of the device with the average on (grey) and off (yellow) state currents. (c) The response speed of the device was tested by applying a square wave pulse of 4 V_{p-p}. (d) Endurance of the device was tested by observing the stability of the on and off state currents for more than 1000 *I–V* cycles.

These injected electrons then get accumulated on the quantum dots as the quantum dots act as trapping centers for electrons. Only a few electrons from there would go to the Al contact; hence, the current is initially very small, as shown in Figure 3.8b. As the voltage increases, the number of trapped electrons increases and induces SCLC conduction. After some time, when the voltage is high, all of the trapping centers are filled and the number of injected charge carriers is more

than the space charge and thus, space charge limited transport takes over. At the threshold voltage, the alignment of the Fermi level allows for free flow of charge carriers, leading to a negative gradient for the injected charge carriers and some of the trap free charge carriers as they rush from the ITO side to the Al side, as shown in Figure 3.8c. At this point, all of the trapping centers are almost occupied by the electrons and they can generate an internal field to form a conductive path through the insulating PVP. This resulted in rapid increases in current after SET voltage. When the voltage is gradually decreased from 2 V, the current remains high as the injected carriers along with trapped carriers in the quantum dots would be released. This continues till the Fermi level of the metal allows for the injection of carriers and then the conduction is due to the trapped charge only because of the relatively less positive voltage. The current continues to be in the high state even after 0 V in the negative bias as the trapped carriers are still released from the quantum dots till it reaches the negative threshold, as indicated in Figure 3.8d. When all of the trapped electrons are released from the quantum dots, the conductive path through the PVP is destroyed and the Fermi level of the metal would have aligned with that of PVP such that few high energetic charge carriers can cross the barrier and hence the current flows after the threshold voltage, albeit less current at −2 V in the negative side, and is shown in Figure 3.8e. When the voltage is traced back from −2 to 0 V, the current flow decreases drastically as the Fermi level of Al reduces and allows for only very few energetic charge carriers to cross the barrier. This cycle continues, and this leads to the reproduced behavior of the I−V characteristic.

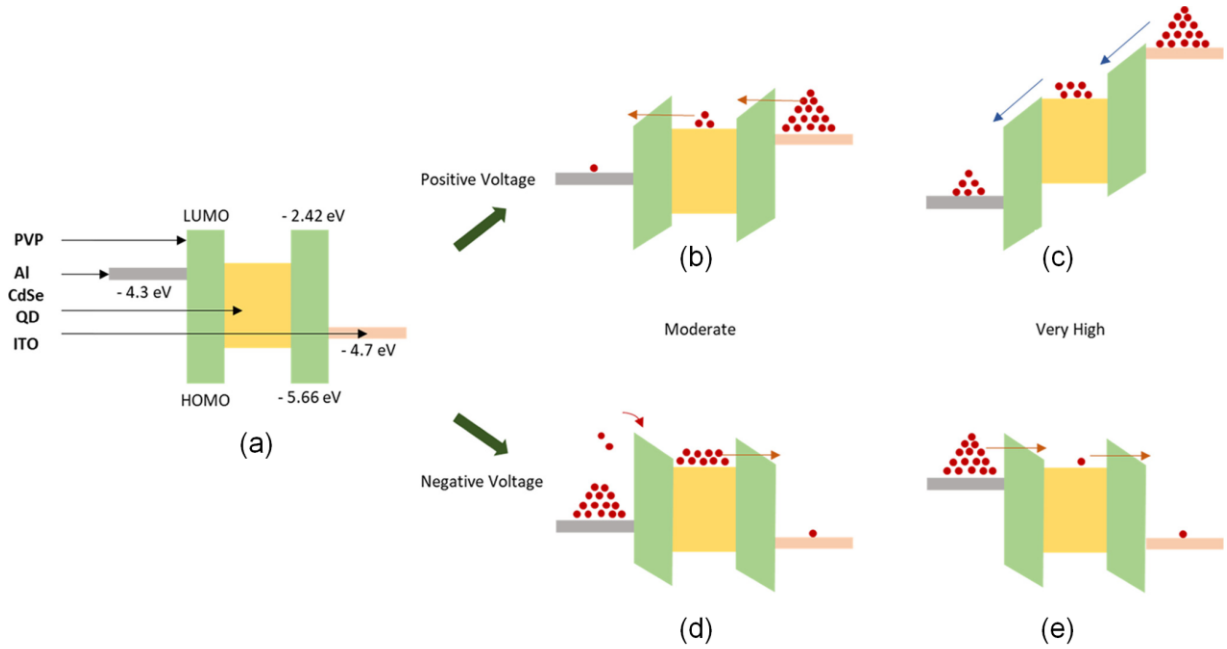

Figure 3.8: (a) Schematic of the distribution of energy levels of PVP and CdSe quantum dots along with the corresponding work functions of the metal contacts. (b) Alignment of energy levels with applied moderate forward bias. (c) Alignment of energy levels with very high positive voltage. (d) Alignment of energy levels with moderate negative voltage. (e) Alignment of energy levels with high negative voltage.

3.4 Conclusions

A sandwiched device structure consisting of a nanocomposite of an insulating polymer and monodispersed CdSe quantum dots as the active layer formed a uniform pinhole-free surface. The CdSe QDs were synthesized using the hot injection method and they were blended with PVP to form the nanocomposite. Several characterization techniques confirmed the successful synthesis of monodispersed CdSe QDs. The electrical behavior of the device with a structure of Al/CdSe QDs-PVP/ITO was studied. The device exhibited excellent RS behavior with a maximum I_{ON}/I_{OFF} of 10^5, endurance cycle over 4000 cycles, fast response time in ns and low power consumption. By observing the I−V characteristics of the device, it was found that the current in the device varies differently with applied voltage. In the low conducting state, it first

varies linearly, then quadratically, and finally exponentially, but in the case of the high conducting state, it varies linearly. The conduction mechanisms in the off state are due to the thermally generated free charge carriers and SCLC conduction, while the conduction mechanism in the on state is due to ohmic conduction owing to the formation of a conductive path across the active layer. We modelled the behavior to understand the whole transport mechanism by considering a nanoscale heterostructure of the insulator and quantum dots. In the forward bias, the conduction follows both thermal and SCLC, whereas, in the reverse bias, the conduction is mainly dominated by space charge limited conduction. Therefore, a high I_{ON}/I_{OFF} in a memory device can be achieved by constructing a nanoscale heterostructure device structure.