

Mitigation of Destabilizing Effects of CPLs in an Islanded DC Microgrid

In the previous chapters, mitigation of CPL induced negative impedance instabilities has been addressed in individual dc/dc converters in the presence of CPL. In a practical dc distribution such as dc microgrid, many power converters are used to interface RESs and storage units, which are interconnected and controlled to work as a single system. Therefore, to address the mitigation of negative impedance instabilities introduced by CPLs and voltage regulation in an integrated system of power converters, this chapter addresses mitigation of the destabilizing effects of CPLs in an islanded dc microgrid using robust sliding mode control.

A dc microgrid usually consists of distributed RESs, Energy Storage Units (ESUs), grid-connecting bidirectional VSC and local dc load. When integrating RESs, ESUs, and dc loads, there is a need for power conversion through power electronic interfaces to achieve different voltage levels. This results in cascaded distributed power architecture of DCMG in which power electronic converters act as interfaces between subsystems with different voltage levels [Kwasinski and Onwuchekwa, 2011; Huddy and Skufca, 2013]. In a cascaded distributed power architecture if control performance and bandwidth of POLCs is sufficiently high, they behave as CPLs and introduce destabilizing effects in the upstream converters or input filters, and in the system as a whole [Magne et al., 2014; Sulligoi et al., 2014]. The destabilizing effects of CPLs result in limit cycles in the switch model dynamics which may cause the dc bus voltage to show severe oscillations or it may lead to voltage collapse. In addition to these effects, inter-converter dynamics and uncertainties associated with RESs further aggravate the stability challenges in DCMGs and may lead to an unstable system, even if individual converters are stable. Therefore, the stability of a DCMG in the presence of CPLs needs adequate attention to ensure basic functioning of DCMG.

Due to uncertainties involved with the RESs, inter-converter dynamics and the presence of CPLs, a dc microgrid becomes a highly nonlinear system. The controllers designed through conventional linear approach are tuned to provide a required performance at the given operating point and their performance may degrade badly if operating point drifts, for which controllers were tuned. It implies, controls designed through linear approach ensure stability in a small-signal sense. Researchers have been able to address the CPL induced instabilities using linear control approaches [Radwan and Mohamed, 2012b; Tabari and Yazdani, 2015; Ahmadi and Ferdowsi, 2014]. However, in a RESs based dc microgrid, the operating point may drift due to the presence of uncertainties and use of droop control. Thus controllers designed using conventional linear approach may not ensure stability and the required performance. Therefore, it becomes necessary that the control be designed using robust nonlinear techniques to ensure stability in the entire possible operating range. Authors in [Tahim et al., 2015], have presented nonlinear stability analysis of a droop controlled dc microgrid using bifurcation and phase-plane analysis. The use of large-signal centralized stabilizing system is presented in [Magne et al., 2012b], to stabilize a dc power system by injecting stabilizing powers to each CPL individually, and to ensure global stability. To reduce the number of sensors required by the central stabilizer, an observer to estimate load input voltages is presented by the authors in [Magne et al., 2013].

There has been some efforts to stabilize individual converters in face of CPL. However, entire microgrid with many converters, storage units, and CPL along with other loads poses entirely different challenges. There are several sources of uncertainty in a dc microgrid, thus the controller must be sufficiently robust to ensure stability and performance in face of uncertainty and CPLs. The work presented in this chapter addresses this particular problem. In the first section of this chapter, an SMC based robust nonlinear control scheme is presented for an islanded solar PV based dc microgrid supplying a composite load. A limit on CPL power has been established to ensure system stability under various operating modes. A realistic mathematical model of solar PV array is used to account for the effects of primary source dynamics on the controller performance. The effectiveness of the proposed control scheme is validated through real-time simulation studies using ORDS, under sufficiently large variations in the input voltage and the load.

Mitigation of the destabilizing effects of CPLs and dc bus regulation using robust SMC approach is addressed in a prototype PV based DCMG, realized in laboratory with two RESs (solar PV) interfaced to dc bus using dc/dc boost converter, lead-acid battery based storage system interfaced through a BDC, and load (resistive load, programmable dc CPL representing a voltage regulator type CPL, and a speed controlled dc/ac inverter drive). Tightly regulated voltage regulator and a speed controlled dc/dc drive, both represent CPLs in the system. The design of controllers for RES interfacing converters and battery energy storage interfacing BDC are proposed and analytical proof of the stability is also provided. To achieve the desired dc bus voltage regulation and proportional power/current sharing between two RESs, voltage droop approach is used. Furthermore, a charging/discharging algorithm for battery bank interfacing bidirectional converter is incorporated which facilitates three mode charging of the battery bank. The effectiveness of the proposed control scheme is validated through simulation studies and experimental results under various operating modes.

5.1 ROBUST CONTROL OF ISLANDED DC MICROGRID WITH COMPOSITE LOAD

In this section, a robust sliding mode control scheme for an islanded solar PV based dc microgrid supplying a composite load to mitigate CPL induced instabilities is proposed. In the following subsection, system modeling, design of SMC, and stability analysis are provided, followed by validation of controller performance through real-time simulation studies.

5.1.1 System Modeling of DCMG with Composite Load

A schematic diagram of a typical solar PV based dc microgrid operating in islanded mode, is shown in Figure 5.1(a) and its corresponding circuit diagram is shown in Figure 5.1(b). It consists of multiple PV RESs in parallel and interfaced through dc/dc boost converters, and an ESU interfaced through BDC. The main objectives of an ESU in a dc microgrid are to support the dc bus voltage regulation, to provide backup power, and to absorb the short-time dc bus transients. The dc bus voltage regulation, equal per unit current sharing between parallel RESs, and the stability of the system, are the main operational requirements of a dc microgrid. In the presented system, RES converters are responsible for dc bus voltage regulation under normal situation (bus voltage is greater than some predefined threshold voltage v_{th}). Under this situation, the ESU operates in charging mode or remains at standby, if fully charged. When dc bus voltage falls below V_{th} due to the reduction in RES power or increase in the load demand, ESU starts supplying power to the dc bus (discharging mode), and maintains dc bus voltage at V_{th} . When, the combined power of RESs and ESU fall below the load demand at any moment, and the dc bus voltage drops below V_{th} , the Energy Management System (EMS) which continuously tracks the dc bus voltage, implements load shedding to restore the power balance. However, in this work dc bus voltage regulation is achieved through mutual coordination of RESs and ESU. In the following section, modeling of different subsystems of the DCMG of Figure 5.1 will be presented.

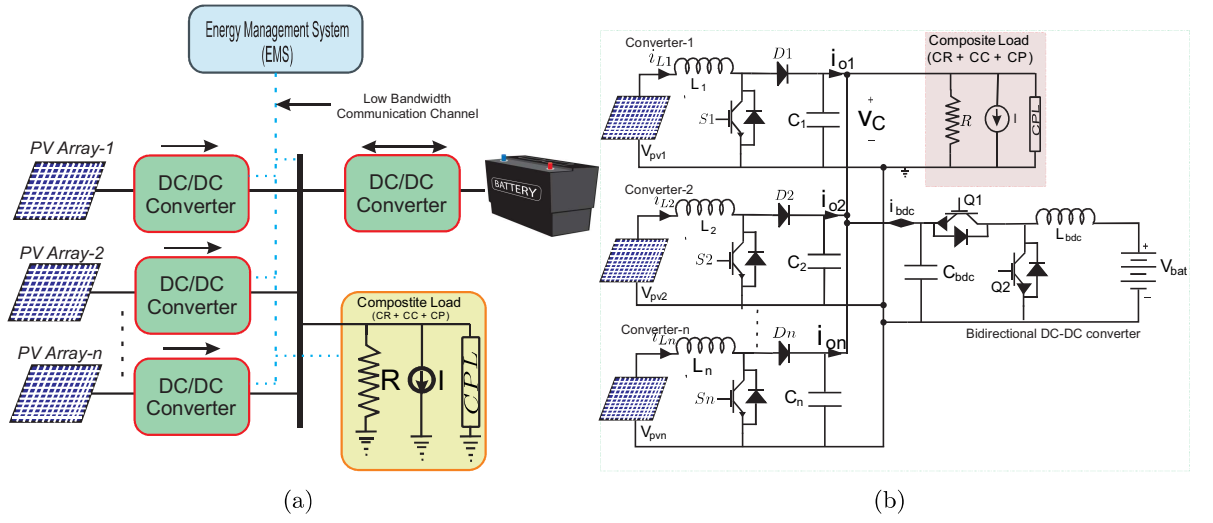


Figure 5.1 : PV based microgrid in island mode: (a) Schematic diagram; (b) Circuit diagram

(a) Model of PV array

The effect of actual PV source dynamics on the performance of the proposed control scheme is taken into account by using the model of the PV array instead of the ideal voltage source. The equivalent circuit of a PV cell is shown in Figure 5.2. The relationship between

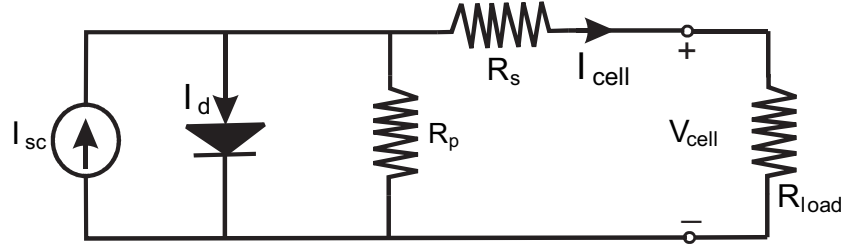


Figure 5.2 : Equivalent circuit of a PV cell

current supplied by the cell I_{cell} and its terminal voltage V_{cell} is given by [Masters, 2004; Gow and Manning, 1999; Moballegh and Jiang, 2014].

$$I_{cell} = I_{sc} - I_d \left[\exp\left(\frac{V_{cell} + I_{cell}R_s}{V_T}\right) - 1 \right] - \frac{V_{cell} + I_{cell}R_s}{R_p} \quad (5.1a)$$

$$V_{cell} = V_d + I_{cell}R_s \quad (5.1b)$$

where I_{sc} is the short-circuit current of the PV cell, I_d is the diode saturation current, V_d is the diode voltage, R_p is the parallel leakage resistance, and R_s is the series resistance that includes contact and wire resistances. V_T is the thermal voltage given by.

$$V_T = \frac{kT}{qQ_d} \quad (5.2)$$

where, k is the Boltzmann's constant, T is the cell temperature (K), q is the electron charge and Q_d is the diode quality factor. Assuming the number of cells connected in series in a PV module are n_{cell} , the voltage of the module is given by $V_{module} = n_{cell}V_{cell}$ and module current remains same as I_{cell} . Similarly, for a PV array containing n_{series} series connected modules per

string and $n_{parallel}$ parallel strings, PV array parameters are given by.

$$I_{PV} = I_{cell}n_{parallel} \quad (5.3a)$$

$$I_{sat,PV} = I_{sat}n_{parallel} \quad (5.3b)$$

$$V_{PV} = V_T n_{series} \quad (5.3c)$$

$$R_{s,PV} = R_s \frac{n_{series}}{n_{parallel}} \quad (5.3d)$$

$$R_{p,PV} = R_p \frac{n_{series}}{n_{parallel}} \quad (5.3e)$$

where I_{pv} , $I_{sat,PV}$, V_{pv} , $R_{s,PV}$ and $R_{p,PV}$ are the current supplied, saturation current, voltage, series resistance and parallel leakage resistance respectively, of the PV array.

(b) Model of interfacing converters and load

The nonlinear state-space averaged model of the dc microgrid circuit diagram shown in Figure 5.1(b) is given in (5.4). The capacitor voltage v_C , inductor currents of RES interfacing converters i_{Lj} , and inductor current of BDC i_{Lbdc} are chosen as state variables. Furthermore, the load is considered to be a composite load and parasitic effects of the components are ignored.

$$\frac{di_{Lj}}{dt} = \frac{V_{pv,j}}{L_j} - \frac{(1-u_j)}{L_j} v_C \quad (5.4a)$$

$$\frac{di_{Lbdc}}{dt} = \frac{V_{bat}}{L_{bdc}} - \frac{u_{Lbdc}}{L_{bdc}} v_C \quad (5.4b)$$

$$\frac{dv_C}{dt} = \frac{1}{C_{eq}} \sum_{j=1}^n (1-u_j) i_{Lj} + \frac{1}{C_{eq}} u_{bdc} i_{Lbdc} - \frac{1}{C_{eq}} \left(\sum_{j=1}^n i_{oj} \pm i_{bdc} \right); \quad j = 1 \dots n \quad (5.4c)$$

where j is the number of RES interfacing converters. $u_j \in \{0,1\}$, $V_{PV,j}$, L_j , C_j and i_{Lj} are the control input, PV array voltage, inductance, capacitance and the inductor current respectively, of j^{th} dc-dc boost converter. $u_{bdc} \in \{0,1\}$, V_{bat} , L_{bdc} , C_{bdc} and i_{Lbdc} are the control input, battery bank voltage, inductance, capacitance and the inductor current respectively, of the BDC. The equivalent capacitance of the system is given by $C_{eq} = C_{bdc} + C_1 + C_2 + \dots + C_n$. Furthermore, $v_{Cbdc} = v_{C1} = v_{C2} = \dots = v_{Cn} = v_C$. The load current i_{load} drawn by the composite (RIP) load is equal to $\sum_{j=1}^n i_{oj} \pm i_{bdc}$, and is given by

$$i_{load} = \frac{v_C}{R_L} + i_{const} + \frac{P}{v_C} \quad (5.5)$$

where, R_L is the resistance of the constant resistance component of the load, i_{const} is the constant current component of load current, and P is the rated power of the CPL component.

The voltage droop control approach is widely used to ensure equal per unit current sharing among parallel operating RESs and desired voltage regulation. The voltage droop controllers rely on local information and are free from any data exchange between the RESs, resulting in an uncoupled system [Chen, 1995]. Therefore, the model of a single converter can be used to design the control.

The conventional droop control has a trade-off between accuracy of current sharing and the voltage regulation [Anand et al., 2013]. Therefore, to avoid the drawback of conventional droop control, here an adaptive nonlinear droop control, proposed in [Khorsandi et al., 2014], is used. In adaptive nonlinear droop, the slope of droop curve increases with the increase in load current from no-load to full load, and it also causes a proportional upward shift in the voltage to compensate for the voltage drop due to droop action. The resulting effect is that the equivalent droop coefficient changes adaptively from no-load to full load, being its minimum value at no-load and maximum value at full-load. The only drawback is poor current sharing performance during light loads. However, during light load condition, current sharing is not

that critical, as RESs supply current which is far below than their rated capacity. The adaptive nonlinear droop equation is given by

$$v_{Cref,j} = v_{dc,ref} - \kappa_j i_{oj}^{\xi_j} \quad (5.6)$$

where $v_{Cref,j}$ is the reference capacitor voltage for j^{th} converter, $v_{dc,ref}$ is the nominal value of the dc bus voltage, i_{oj} is the output current of j^{th} the converter unit. κ and ξ are defined as arc constant and arc coefficient respectively.

$$\kappa_j = \frac{v_{dc,ref} - V_L}{I_{max,j}^{\xi}} \quad (5.7)$$

where $I_{max,j}$ is the maximum allowable output current of the j^{th} converter unit and V_L is the minimum acceptable dc bus voltage. The equivalent droop coefficient R_d as a function of the converter output current, is given by.

$$R_{d,j} = \frac{\partial v_{Cref,j}}{\partial i_{oj}} = \frac{-\xi (v_{dc,ref} - V_L)}{I_{max,j}^{\xi}} i_{oj}^{\xi-1} \quad (5.8)$$

After the selection of maximum value of droop coefficient $R_{d,j}^{max}$, the value of arc constant ζ can be obtained using the following relation.

$$\xi_j = \frac{R_{d,j}^{max} \cdot I_{max,j}}{v_{dc,ref} - V_L} \quad (5.9)$$

5.1.2 Sliding Mode Control Design

To design the sliding mode controllers for various dc/dc converters of the system shown in Figure 5.1(b), the individual state-space averaged model of the converters are used. An extended model of individual converter model is obtained by adding a disturbance term $D(t)$ in the original model. This disturbance term takes into account impact of remaining system and the changes in the load, and also helps to minimize steady-state error in the dc bus voltage [Kondratiev et al., 2006].

(a) Control design for RES interfacing converters

The extended model of j^{th} dc/dc boost converter interfacing RES is given by

$$\frac{di_{Lj}}{dt} = \frac{V_{pv,j}}{L_j} - \frac{\hat{u}_j}{L_j} v_C \quad (5.10a)$$

$$\frac{dv_C}{dt} = \frac{\hat{u}_j}{C_{eq}} i_{Lj} - \frac{i_{oj}}{C_{eq}} + \frac{D_j}{C_{eq}} \quad (5.10b)$$

$$\frac{dD_j}{dt} = \sigma_j (v_C - v_{Cref,j}) \quad (5.10c)$$

where $D_j = \sigma_j \int (v_C - v_{Cref,j}) dt$; $\sigma > 0$, $\hat{u}_j = 1 - u_j$, and i_{oj} is the output current of the j^{th} converter. In general, the load current contribution from j^{th} converter, i_{oj} is given by

$$i_{oj} = b_j i_{load}; \quad \sum_{j=1}^n b_j \pm b_{bdc} = 1 \quad (5.11)$$

where b_j is the fraction of total load current supplied by the j^{th} RES converter, and b_{bdc} is the fraction of total load current supplied or drawn by the BDC.

Switching function: The switching function is chosen such that supply of constant power to the load and zero steady state error in the dc bus voltage is ensured. The switching function for j^{th} RES converter, s_j is defined by

$$s_j := (i_{Lj} - i_{Lref,j}) + \beta_{1j} (v_C - v_{Cref,j}) + \beta_{2j} D_j \quad (5.12)$$

where $i_{Lref,j}$ and $v_{Cref,j}$ are the reference values of the inductor current and capacitor voltage respectively, of j^{th} converter, and β_{1j} , and β_{2j} are positive constants used to tune control the convergence speed. The first term in the switching function expression given in (5.12) requires reference inductor current which depends on the input voltage, output voltage and the load, thus it is a dynamic variable. The high pass filtered inductor current is used to estimate the inductor current error ($i_{Lj} - i_{Lref,j}$) [Santi et al., 2003; Mattavelli et al., 1993].

$$\dot{s}_j = -\lambda_j s_j - Q_j \operatorname{sgn}(s_j) \quad (5.13)$$

where $\lambda > 0$ is the parameter which controls the convergence speed and $Q > 0$, which depends on the magnitude of uncertainty. Substituting (5.10) and (5.12) into (5.13) and solving for $\hat{u}$ gives the following expression of the instantaneous duty cycle for j^{th} RES interfacing converter

$$\hat{u}_j(t) = \frac{\lambda_j s_j + Q_j \text{sgn}(s_j) + \frac{\beta_{1j} D_j}{C_{eq}} + \frac{V_{pv,j}}{L_j} + \beta_{2j} \sigma_j (v_C - v_{Cref,j}) - \frac{\beta_{1j} i_{oj}}{C_{eq}}}{\frac{1}{L_j} v_C - \frac{\beta_{1j}}{C_{eq}} i_{Lj}} \quad (5.14)$$

The control law given in (5.14), is obtained by considering the generalized load profile. The control for a specific load model can be obtained by substituting respective load model in (5.14).

The control law (5.14) forces the system trajectory from an arbitrary point on to the manifold $s = 0$ and maintains it on $s = 0$ then on. The voltage reference $v_{Cref,j}$ to the converter is modified to ensure desired voltage regulation and equal/proportional current sharing according to the adaptive nonlinear droop (5.6). The droop characteristics basically modifies the reference voltage (nominal dc bus voltage) before applying it to a particular RES interfacing converter, based on current supplied by it.

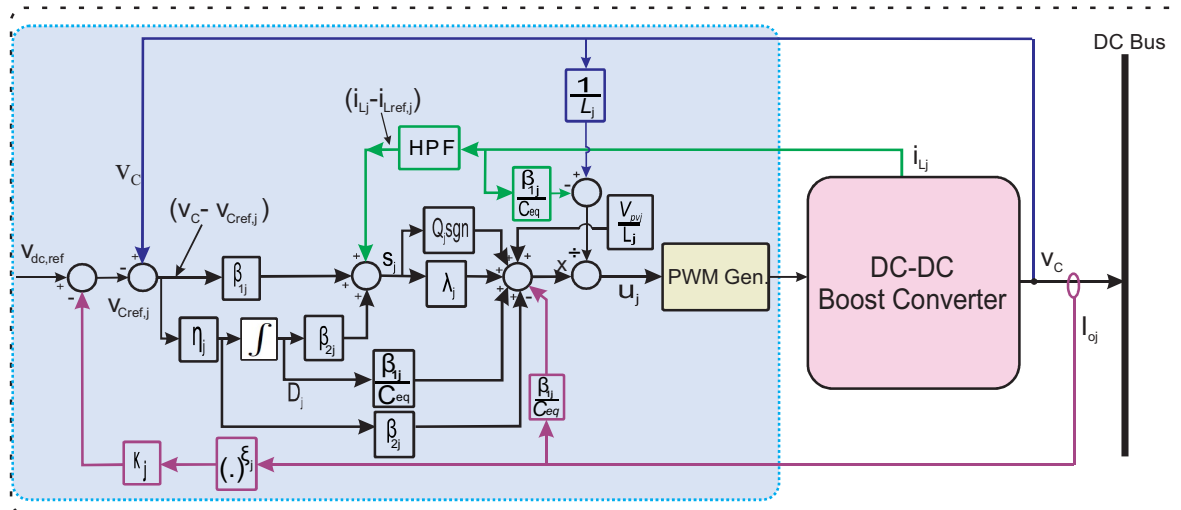


Figure 5.3 : The proposed sliding mode controller for j^{th} RES converter

(b) Control design for BDC

The extended model of BDC interfacing battery bank is given by

$$\frac{di_{Lbdc}}{dt} = \frac{V_{bat}}{L_{bdc}} - \frac{u_{bdc}}{L_{bdc}} v_C \quad (5.15a)$$

$$\frac{dv_C}{dt} = \frac{u_{bdc}}{C_{eq}} i_{Lbdc} - \frac{i_{bdc}}{C_{eq}} + \frac{D_{bdc}}{C_{eq}} \quad (5.15b)$$

$$\frac{dD_{bdc}}{dt} = \sigma_{bdc}(v_C - v_{Cref,bdc}) \quad (5.15c)$$

where, $D_{bdc} = \sigma_{bdc} \int (v_C - v_{Cref,bdc}) dt$; $\sigma_{bdc} > 0$, and i_{bdc} is the current supplied to dc bus (positive in discharging mode and negative in charging mode).

Switching function: The switching function for BDC is defined as follows

$$s_{bdc} := (i_{Lbdc} - i_{Lref,bdc}) + \alpha_1(v_C - V_{Cref,bdc}) + \alpha_2 D_{bdc} \quad (5.16)$$

where $i_{Lref,bdc}$ and $v_{Cref,bdc}$ are the reference values of the inductor current and capacitor voltage respectively of BDC, and α_1 and α_2 are positive constants to control the convergence speed. The sign of the inductor current reference $i_{Lref,bdc}$ depends on the mode of operation of BDC (positive in discharging mode and negative in charging mode) and its magnitude is decided based on the present value of SoC of the battery bank. The inductor current reference in two operating modes is estimated as follows

$$i_{Lref,bdc} = -\frac{100}{SoC} I_{c,min} \quad (\text{charging mode}) \quad (5.17a)$$

$$i_{Lref,bdc} = \frac{SoC}{100} I_{d,max} \quad (\text{discharging mode}) \quad (5.17b)$$

where $I_{c,min}$ and $I_{d,max}$ are the minimum desired charging current and maximum permissible discharging current respectively. The above strategy allows high discharging current when battery bank is fully charged and vice-versa. Similarly, in charging mode the strategy allows fast charging of the fully depleted battery bank and vice-versa.

Control law: Reaching dynamics, as given in (5.13), is used to derive the control law for BDC

$$\dot{s}_{bdc} = -\lambda_{bdc} s_{bdc} - Q_{bdc} \text{sgn}(s_{bdc}) \quad (5.18)$$

where $\lambda_{bdc} > 0$ is the parameter which controls the convergence speed and $Q_{bdc} > 0$, which depends on the magnitude of uncertainty. Substituting (5.15) and (5.16) into (5.18) and solving for u_{bdc} gives the following expression of the instantaneous duty cycle for BDC

$$u_{bdc}(t) = \frac{-\lambda_{bdc} s_{bdc} - Q_{bdc} \text{sgn}(s_{bdc}) - \frac{V_{bat}}{L_{bdc}} - \alpha_2 \sigma_{bdc}(v_C - v_{Cref,bdc}) + \frac{\alpha_1 i_{bdc}}{C_{eq}}}{\frac{\alpha_1}{C_{eq}} i_{Lbdc} - \frac{1}{C_{eq}} v_{Cbdc}} \quad (5.19)$$

5.1.3 Existence of Sliding Mode and Stability of Switching Surface

In this section, the existence of sliding mode and the stability of the switching function are presented. The system trajectory from an arbitrary initial point must reach the switching surface in finite time and constrained to it then on. If after hitting the switching surface, the trajectory converges towards the desired operating point, motion is said to be stable.

(a) Stability of the switching surface

To prove the stability of the motion on the manifold $s = 0$, the generalized system model (5.4) operating under the sliding mode control laws of (5.14) and (5.19) is considered. To ensure the system stability, trajectories after hitting the manifold must converge to the

desired operating point along the manifold $s = 0$. As (5.13) and (5.18) ensure $s = 0$ in finite time, the switching functions of (5.12) and (5.16), now become

$$s_j := (i_{Lj} - i_{Lref,j}) + \beta_{1j}(v_C - v_{Cref,j}) + \beta_{2j}D_j = 0 \quad (5.20)$$

and

$$s_{bdc} := (i_{Lbdc} - i_{Lref,bdc}) + \alpha_1(v_C - v_{Cref,bdc}) + \alpha_2D_{bdc} = 0 \quad (5.21)$$

where D_j and D_{bdc} are disturbances affecting the j^{th} RES converter and BDC respectively. On the manifold, the system order is reduced by $(n+1)$, due to linear dependence of state variables resulting from $s_j = 0$ and $s_{bdc} = 0$. Solving (5.20) and (5.21) for i_{Lj} and i_{Lbdc} , the following reduced order system dynamics is obtained,

$$i_{Lj} = -\beta_{1j}(v_C - v_{Cref,j}) - \beta_{2j}D_j + i_{Lref,j} \quad (5.22a)$$

$$i_{Lbdc} = -\alpha_1(v_C - v_{Cref,bdc}) - \alpha_2D_{bdc} + i_{Lref,bdc} \quad (5.22b)$$

$$\frac{dv_C}{dt} = \frac{1}{C_{eq}} \sum_{j=1}^n (1 - u_j)i_{Lj} + \frac{1}{C_{eq}} u_{bdc}i_{Lbdc} - \frac{i_{load}}{C_{eq}} \quad (5.22c)$$

$$\frac{dD_j}{dt} = \sigma_j(v_C - v_{Cref,j}) \quad (5.22d)$$

$$\frac{dD_{bdc}}{dt} = \sigma_{bdc}(v_C - v_{Cref,bdc}) \quad (5.22e)$$

Eliminating i_{Li} and i_{Lbdc} , and incorporating voltage droop equation (5.6), the reduced order dynamic model becomes

$$\begin{aligned} C_{eq} \frac{dv_C}{dt} + \sum_{j=1}^n \beta_{1j}(1 - u_j)(v_C - v_{dc,ref} + \kappa_j i_{oj}^{\xi_j}) + \sum_{j=1}^n \beta_{2j}(1 - u_j)D_j - \sum_{j=1}^n (1 - u_j)i_{Lref,j} \\ + \alpha_1 u_{bdc}(v_C - v_{Cref,bdc}) + \alpha_2 u_{bdc}D_{bdc} - u_{bdc}i_{Lref,bdc} + i_{load} = 0 \end{aligned} \quad (5.23)$$

Differentiating (5.23) with respect to time.

$$\begin{aligned} C_{eq} \frac{d^2 v_C}{dt^2} + \sum_{j=1}^n \beta_{1j}(1 - u_j) \frac{dv_C}{dt} + \sum_{j=1}^n \beta_{1j}(1 - u_j) \kappa_j \frac{di_{oj}^{\xi_j}}{dt} + \alpha_1 u_{bdc} \frac{dv_C}{dt} + \frac{di_{load}}{dt} \\ + \sum_{j=1}^n \beta_{2j}(1 - u_j) \sigma_j v_C + \alpha_2 u_{bdc} \sigma_{bdc} v_C + \sum_{j=1}^n \beta_{2j}(1 - u_j) \sigma_j \kappa_j i_{oj}^{\xi_j} \\ = \sum_{j=1}^n \beta_{2j}(1 - u_j) v_{dc,ref} + \alpha_2 u_{bdc} v_{Cref,bdc} \end{aligned} \quad (5.24)$$

Substituting output current of the j^{th} converter in terms of the total load current using (5.11).

$$\begin{aligned} C_{eq} \frac{d^2 v_C}{dt^2} + \sum_{j=1}^n \beta_{1j}(1 - u_j) \frac{dv_C}{dt} + \sum_{j=1}^n \beta_{1j}(1 - u_j) \kappa_j b_j^{\xi_j} \frac{di_{load}^{\xi_j}}{dt} + \alpha_1 u_{bdc} \frac{dv_C}{dt} + \frac{di_{load}}{dt} \\ + \sum_{j=1}^n \beta_{2j}(1 - u_j) \sigma_j v_C + \alpha_2 u_{bdc} \sigma_{bdc} v_C + \sum_{j=1}^n \beta_{2j}(1 - u_j) \sigma_j \kappa_j b_j^{\xi_j} i_{load}^{\xi_j} \\ = \sum_{j=1}^n \beta_{2j}(1 - u_j) v_{dc,ref} + \alpha_2 u_{bdc} v_{Cref,bdc} \end{aligned} \quad (5.25)$$

Considering linear approximation of the load current $i_{load}(v_C)$, we can write.

$$\begin{aligned} i_{load} &\approx \frac{\partial i_{load}}{\partial v_C} v_C \\ \frac{di_{load}}{dt} &\approx \frac{\partial i_{load}}{\partial v_C} \frac{dv_C}{dt} \end{aligned} \quad (5.26)$$

Substitution of (5.26) into (5.25), and assuming $\xi = 1$ to simplify (5.25), results in

$$\begin{aligned}
& C_{eq} \frac{d^2 v_C}{dt^2} + \left(\sum_{j=1}^n \beta_{1j}(1-u_j) + \sum_{j=1}^n \beta_{1j}(1-u_j) \kappa_j b_j \frac{\partial i_{load}}{\partial v_C} + \alpha_1 u_{bdc} + \frac{\partial i_{load}}{\partial v_C} \right) \frac{dv_C}{dt} \\
& + \left(\sum_{j=1}^n \beta_{2j}(1-u_j) \sigma_j + \alpha_2 u_{bdc} \sigma_{bdc} + \sum_{j=1}^n \beta_{2j}(1-u_j) \sigma_j \kappa_j b_j \frac{\partial i_{load}}{\partial v_C} \right) v_C \\
& = \sum_{j=1}^n \beta_{2j}(1-u_j) v_{dc,ref} + \alpha_2 u_{bdc} v_{Cref,bdc}
\end{aligned} \tag{5.27}$$

(5.27) can be written as

$$\begin{aligned}
& C_{eq} \frac{d^2 v_C}{dt^2} + F_1 \frac{dv_C}{dt} + F_2 v_C = F_3 \\
& \text{where,} \\
& F_1 = \alpha_1 u_{bdc} + \sum_{j=1}^n \beta_{1j}(1-u_j) + \left(1 + \sum_{j=1}^n \beta_{1j}(1-u_j) \kappa_j b_j \right) \frac{\partial i_{load}}{\partial v_C} \\
& F_2 = \alpha_2 u_{bdc} \sigma_{bdc} + \sum_{j=1}^n \beta_{2j}(1-u_j) \sigma_j + \sum_{j=1}^n \beta_{2j}(1-u_j) \sigma_j \kappa_j b_j \frac{\partial i_{load}}{\partial v_C} \\
& F_3 = \sum_{j=1}^n \beta_{2j}(1-u_j) v_{dc,ref} + \alpha_2 u_{bdc} v_{Cref,bdc}
\end{aligned} \tag{5.28}$$

For the stability of the system on the manifold $s = 0$, the following conditions must be satisfied

$$F_1 > 0 \tag{5.29a}$$

$$F_2 > 0 \tag{5.29b}$$

Equation (5.29) gives stability conditions for the islanded dc microgrid of Figure 5.1 with a generalized load profile. Next, the stability of the system supplying a composite load will be established.

Stability conditions for composite (RIP) load profile: Considering equal current sharing between parallel connected RES interfacing converters, it follows that

$$\begin{aligned}
& \beta_{1j} = \beta_1; \beta_{2j} = \beta_2; \beta_{3j} = \beta_3; \sigma_j = \sigma \\
& \kappa_j = \kappa; \xi_j = \xi; b_j = b = \frac{1}{n}; \text{ for } j = 1, 2, 3, \dots, n
\end{aligned} \tag{5.30}$$

it implies

$$\begin{aligned}
& F_1 = \alpha_1 u_{bdc} + \beta_1 \sum_{j=1}^n (1-u_j) + \left(1 + \beta_1 \kappa b \sum_{j=1}^n (1-u_j) \right) \frac{\partial i_{load}}{\partial v_C} \\
& F_2 = \alpha_2 u_{bdc} \sigma_{bdc} + \beta_2 \sigma \sum_{j=1}^n (1-u_j) + \beta_2 \sigma \kappa b \sum_{j=1}^n (1-u_j) \frac{\partial i_{load}}{\partial v_C}
\end{aligned} \tag{5.31}$$

Considering the composite load profile of (5.5)

$$\frac{\partial i_{load}}{\partial v_C} = \frac{1}{R_L} - \frac{P}{v_{dc,ref}^2} \tag{5.32}$$

It implies that for the stability of the system the following conditions must be satisfied

$$\alpha_1 u_{bdc} + \beta_1 \sum_{j=1}^n (1-u_j) + \left(1 + \beta_1 \kappa b \sum_{j=1}^n (1-u_j) \right) \left(\frac{1}{R_L} - \frac{P}{v_{dc,ref}^2} \right) > 0 \tag{5.33a}$$

$$\alpha_2 u_{bdc} \sigma_{bdc} + \beta_2 \sigma \sum_{j=1}^n (1-u_j) + \beta_2 \sigma \kappa b \sum_{j=1}^n (1-u_j) \left(\frac{1}{R_L} - \frac{P}{v_{dc,ref}^2} \right) > 0 \tag{5.33b}$$

Let

$$K_1 := \frac{\alpha_1 u_{bdc} + \beta_1 \sum_{j=1}^n (1 - u_j)}{1 + \beta_1 \kappa b \sum_{j=1}^n (1 - u_j)} \quad (5.34a)$$

$$K_2 := \frac{\alpha_2 u_{bdc} \sigma_{bdc} + \beta_2 \sigma \sum_{j=1}^n (1 - u_j)}{\beta_2 \sigma \kappa b \sum_{j=1}^n (1 - u_j)} \quad (5.34b)$$

Simplifying (5.33) using (5.34), we get

$$\frac{P}{v_{dc,ref}^2} - \frac{1}{R_L} < K_1 \quad (5.35a)$$

$$\frac{P}{v_{dc,ref}^2} - \frac{1}{R_L} < K_2 \quad (5.35b)$$

Therefore, in order to ensure stability, the following condition must be satisfied.

$$\frac{P}{v_{dc,ref}^2} - \frac{1}{R_L} < K; \text{ where } K = \text{Min}\{K_1, K_2\} \quad (5.36)$$

It implies

$$P < v_{dc,ref}^2 \left(\frac{1}{R_L} + K \right); \text{ or } P - P_{R_L} < v_{dc,ref}^2 K \quad (5.37)$$

where P_{R_L} is the power consumed by the resistive component of the load. It can be seen from (5.37) that, the limit on CPL component of the load depends on power consumed by the resistive component, nominal dc bus voltage, and K . In the worst case, when the minimum value of K is zero (with $u_{bdc} = 0$ and $u_j = 1$), to ensure the stability of the system CPL power P must be less than power consumed by the resistive component of the load ($\frac{v_{dc,ref}^2}{R_L}$).

Remark 5.1. Thus, the worst case limit on CPL power obtained from (5.37) is in congruence with the established condition to ensure the small-signal stability of a system in presence of CPLs ($P_{CPL} < P_{CVL}$). In all other cases, this limit on CPL power would always be higher than the worst case limit.

(b) Existence of sliding mode

The chosen reaching dynamics ensures the existence of the sliding mode $s = 0$. It is straightforward to prove the existence condition $s^T \dot{s} < -\eta |s|$ for $\eta > 0$ for the reaching dynamics (5.13) (see Chapter 2, Section 2.1.3).

5.1.4 Real-time Simulation Studies

The performance of the proposed control scheme has been validated using PV based dc micro-grid shown in Figure 5.1 with $n = 3$. The input supply to each converter is coming from the modeled PV array. The system is modeled in *MATLAB/SIMULINKTM* and simulated in real-time using ORDS, under the following operating conditions.

- 1 $R_L = 300 \, \Omega$, $i_{const} = 1 \, A$ and abruptly increased to $2.5 \, A$ at $t = 0.3 \, s$, $P = 400 \, W$ and abruptly increased to $1000 \, W$ at $t = 0.5 \, sec$. (Figure 5.6)
- 2 $L_1 = 1 \, mH$, $L_2 = 1.1L_1$, $L_3 = 0.9L_1$ with loading profile as in 1.(Figure 5.7)
- 3 RES boost converter-2 goes offline when the system is supplying load with $R_L = 300 \, \Omega$, $i_{const} = 1 \, A$, $P = 400 \, W$. (Figure 5.8)
- 4 $R_L = 300 \, \Omega$, $i_{const} = 1 \, A$ and abruptly increased to $5 \, A$ at $t = 0.3 \, s$, $P = 400 \, W$ and abruptly increased to $2000 \, W$ at $t = 0.5 \, s$. (Figure 5.9).

The dc microgrid system specifications and the controller parameters used in the real-time simulation studies are provided in Table 5.1. Each PV array consists of two parallel strings of five series modules/string, BP Solar SX3190 module specifications are considered in this study. The I-V and P-V characteristics of a BP Solar SX3190 module are given in Figure 5.4.

Table 5.1 : Islanded dc microgrid with composite load: System specifications and controller parameters

Parameter	Value	Parameter	Value
System rating	8 kW	DC bus voltage $V_{dc,ref}$	300 V
V_{th}	295 V	C_{bus}	2000 μF
PV arrays:			
$P_{max1}, P_{max2}, P_{max3}$	1900 W	$I_{sc1}, I_{sc2}, I_{sc3}$	17.2 A
$V_{oc1}, V_{oc2}, V_{oc3}$	183.6 V		
Converters:			
P_1, P_2, P_3	2 kW	L_1, L_2, L_3	1 mH
r_{L1}, r_{L2}, r_{L3}	0.005 Ω	C_1, C_2, C_3	47 μF
P_{bdc}	2 kW	$L_{bdc}, r_{Lbdc}, C_{bdc}$	2.2 mH, 5 m Ω , 47 μF
Nominal Load			
R_L	300 Ω	P	400 W
I_{const}	1 A		
Controllers			
$\beta_{11}, \beta_{12}, \beta_{13}$	30	$\beta_{21}, \beta_{22}, \beta_{23}$	2
$\kappa_1, \kappa_2, \kappa_3$	0.7	ξ_1, ξ_2, ξ_3	1.33
$\lambda_1, \lambda_2, \lambda_3$	40	Q_1, Q_2, Q_3	10000
α_1	0.005	α_2	2
λ_{bdc}	10000	Q_{bdc}	10000
$\sigma_1, \sigma_2, \sigma_3$	1800	σ_{bdc}	1800

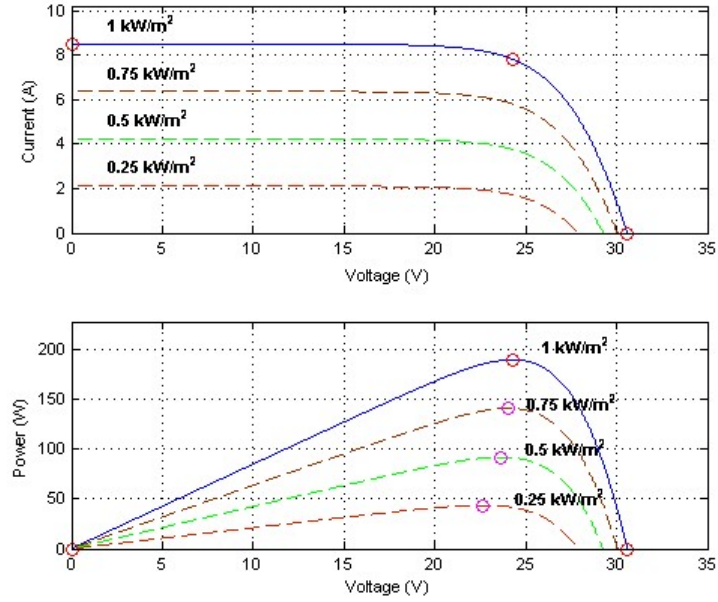


Figure 5.4 : I-V and P-V plots of BP Solar SX3190 PV modules used in the study

In order to include the influence of the changing solar irradiance from morning to evening, or due to partial/full shading of the PV arrays, its variable value is used in the

simulation studies. The solar irradiance pattern used in the simulation studies of three PV arrays is shown in Figure 5.5. The parameters of the adaptive nonlinear droop controller κ

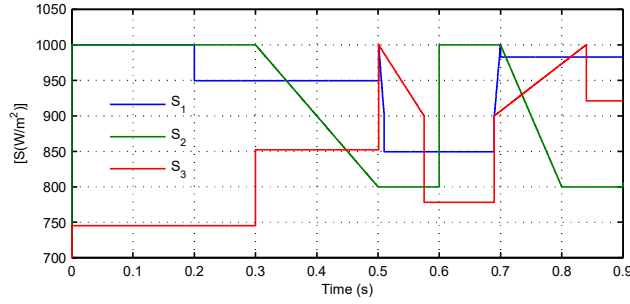


Figure 5.5 : Solar irradiance (S) patterns for three PV arrays used in the study

and ξ are calculated considering the maximum value of droop coefficient $R_{d,max}$, maximum allowable converter output current I_{max} , and voltage regulation of 2, 10, and 5% respectively.

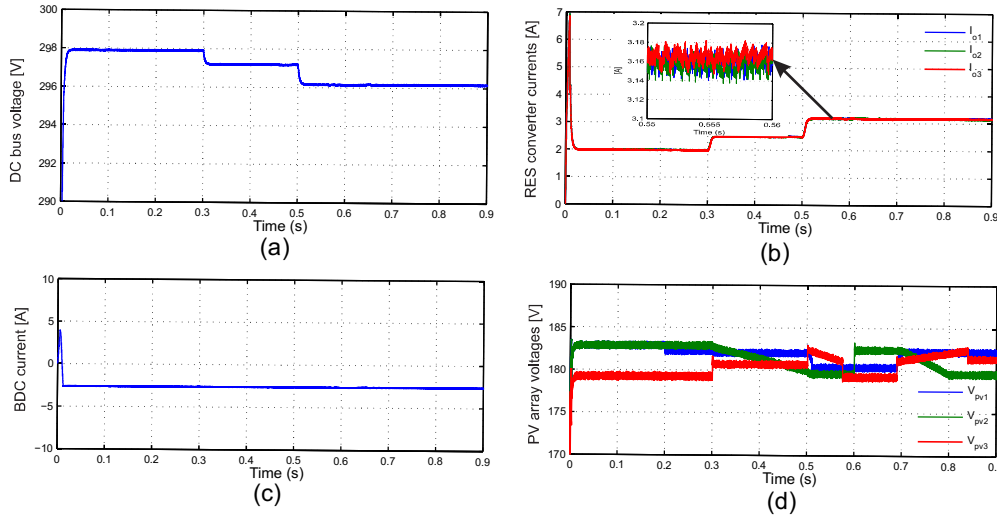


Figure 5.6 : Real-time simulation results under Operating Condition-1: (a) dc bus voltage; (b) Output currents of RES interfacing converters; (c) BDC current; and (d) Voltages of the PV arrays

Real-time simulation results under Operating Condition-1 are shown in Figure 5.6. The dc bus voltage is 298 V (Figure 5.6(a)) with base load which drops to 297.2 V when a step increase of 250% is applied in constant current component of the load at $t = 0.3$ s, and further decreases to 296.2 V when a step change of same magnitude is applied in the CPL power at $t = 0.5$ s. Figure 5.6(b) shows the currents shared by three RES converters. It can be seen that the currents are shared equally, and increased load current due to increase in the load at $t = 0.3$ s and $t = 0.5$ s, is also shared equally. As shown in Figure 5.6(c), the BDC start in discharging mode and switches to charging mode, and draws a charging current of 2.6 A. Even after load increase at $t = 0.3$ s and $t = 0.5$ s, BDC continues to operate in charging mode as dc bus voltage is > 295 V. The influence of the variations in the solar irradiance of the PV arrays can be seen on the voltage of PV arrays (Figure 5.6(d)). DC bus voltage regulation, current sharing accuracy, and system stability under variable solar irradiance demonstrates the effectiveness of the proposed control scheme to handle input side disturbances.

To validate the robustness of the proposed control to system parameter variations, the system was simulated with the same load profile as in Operating Condition-1, but with different values of inductances of the RES interfacing converters. It can be seen from Figure 5.7 that, this variation in the inductances does not have any significant impact on the dc bus voltage, current sharing accuracy between RESs, and the system stability. Figure 5.8, shows the effect of complete shading of a particular PV array or failure of a particular RES converter. It can be seen that when RES converter-2 goes offline at $t = 0.3$ s, the dc bus voltage drops to 296.4 V from its previous value of 298 V (Figure 5.8(a)). Furthermore, converters-1 and 3 equally share the current supplied by converter-2 (Figure 5.8(b)). The BDC is still operating in charging mode drawing a current of 2.6 A, as dc bus voltage is (> 295 V) (Figure 5.8(c)). The effect of converter fault is also visible in the second PV array voltage shown in Figure 5.8(d).

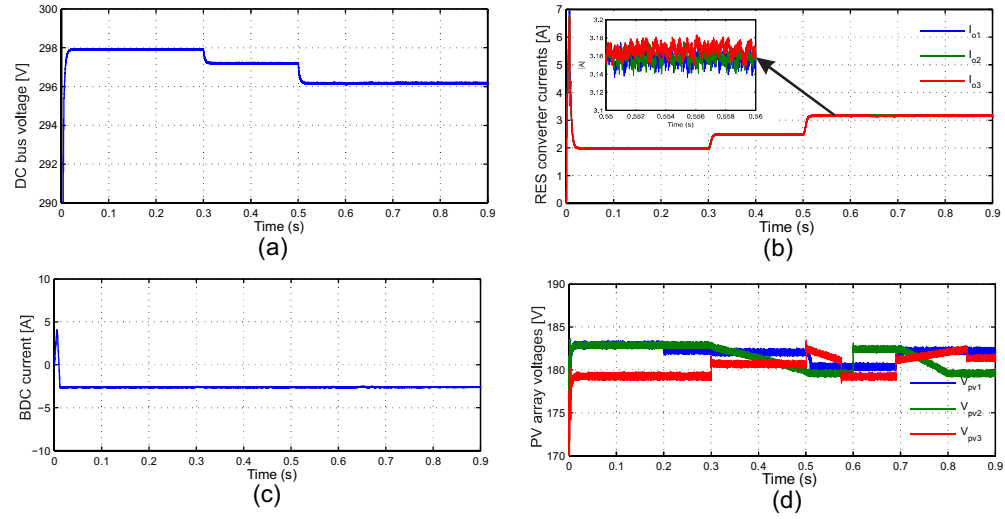


Figure 5.7 : Real-time simulation results under Operating Condition-2: (a) dc bus voltage; (b) Output currents of RES interfacing converters; (c) BDC current; and (d) Voltages of the PV arrays

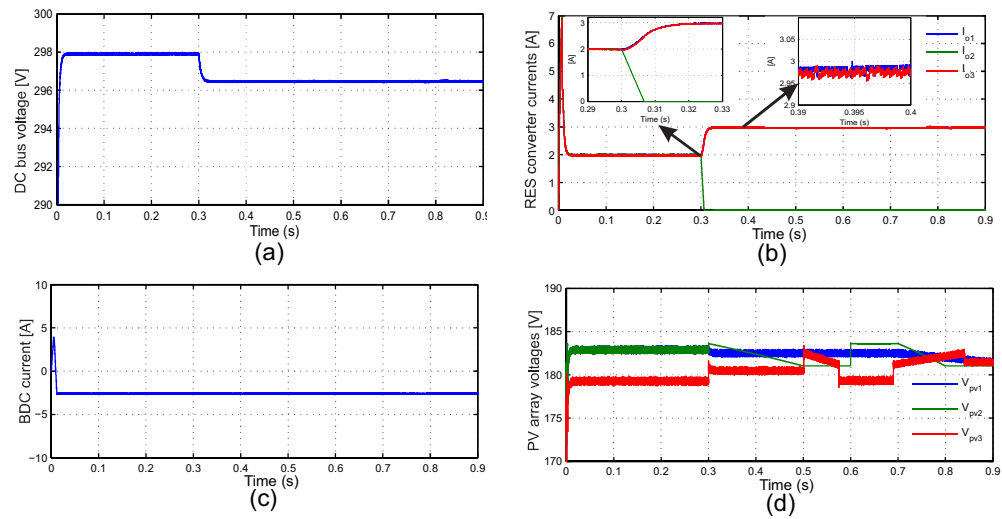


Figure 5.8 : Real-time simulation results under Operating Condition-3: (a) dc bus voltage; (b) Output currents of RES interfacing converters; (c) BDC current; and (d) Voltages of the PV arrays

Figure 5.9 shows simulation results under the Operating Condition-4, when a huge step change of 500% is applied in the constant current and constant power components of the load at $t = 0.3$ s and $t = 0.5$ s respectively. In response to the first step change, the dc bus voltage drops to 296 V (Figure 5.9(a)). The second step change in CPL power at $t = 0.5$ s is sufficient to decrease the dc voltage below 295 V. However, as soon as the dc bus voltage drops below 295 V, the BDC previously operating in charging mode (Figure 5.9(c)), switches to discharging mode and regulates bus voltage at 295 V. The current sharing accuracy is maintained under this operating condition as well (Figure 5.9(b)). As in previous cases, the operating voltages of the PV arrays vary corresponding to the changes in the solar irradiance (Figure 5.9(d)).

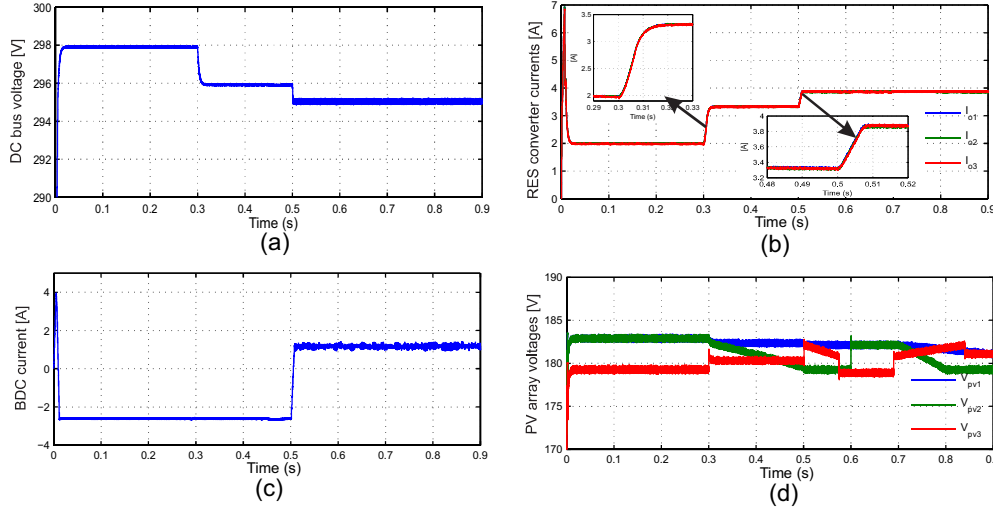


Figure 5.9 : Real-time simulation results under Operating Condition-4: (a) dc bus voltage; (b) Output currents of RES interfacing converters; (c) BDC current; and (d) Voltages of the PV arrays

Above real-time simulation studies validate the effectiveness of the proposed sliding mode control scheme with adaptive droop controls under various operating conditions. The controller demonstrates robustness to the supply and load side disturbances, and variations in the system parameters. The stability of the system is maintained even when the system is supplying a total load of approximately 3.8 kW, and dc bus voltage regulation of 1.66% is ensured.

5.2 ROBUST CONTROL OF PROTOTYPE PV BASED DC MICROGRID

In this section, nonlinear control of an islanded PV based DCMG feeding a CPL dominated load is presented. The control is designed through SMC approach. The test system consists of two solar PV arrays interfaced through dc/dc boost converters, ESU with three mode charging, and load (comprising of resistive load and two types of CPLs namely, voltage regulator and dc/ac inverter drive with tight speed regulation). The effectiveness of the control scheme is validated through real-time simulation studies and experimental results.

5.2.1 Test System and its Operating Modes

The schematic diagram of test system under consideration is shown in Figure 5.10(a) and its corresponding circuit diagram is shown in Figure 5.10(b). The system consists of two solar PV RESs, interfaced through dc/dc boost converters to a 380 V dc bus. To ensure equal current sharing between the RESs and desired voltage regulation, voltage droop control approach is used. A battery bank, interfaced through a BDC, is used to provide backup power

and to regulate dc bus voltage, when power produced from the PV arrays is not sufficient to meet the load demand. To represent a practical system, the load is considered to have both, conventional resistive load and CPL. Furthermore, two types of CPLs namely, tightly controlled voltage regulator (represented by a programmable dc CPL) and a dc/ac inverter drive, which are largely present in a practical system, are considered in the presented work. The charging algorithm of BDC facilitates three mode charging of battery bank namely, Constant Current Charging (CC), Constant Voltage Charging (CV), and Float Charging (FC) to enhance the battery life. The BDC switches its mode of operation depending on the dc bus voltage and SoC of batteries. The implemented charging and discharging algorithm for BDC will be described in detail in the following subsection.

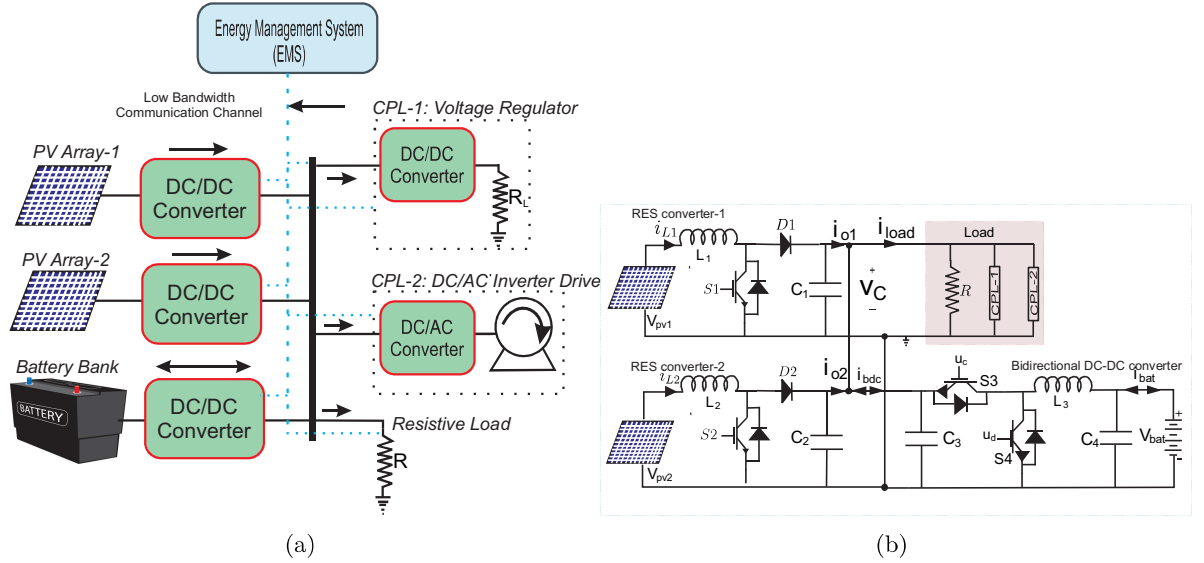


Figure 5.10 : Laboratory prototype of PV based dc microgrid: (a) Schematic diagram; (b) Circuit diagram

(a) Charging/discharging algorithm

The controller of BDC selects an appropriate mode of operation for BDC based on the dc bus voltage and the SoC of battery bank. If the dc bus voltage decreases by more than 5% of its nominal value of (380 V) due to a reduction in the RES power or increased load, and the battery bank SoC is $\geq 50\%$, then BDC switches to discharging mode (voltage control mode). Otherwise it operates in the charging mode. Under discharging mode, if the SoC of the battery bank falls below 50% or Depth of Discharge (DoD) is reached, the BDC goes into standby mode, and waits until the dc bus voltage recovers. Once, the dc bus voltage recovers to normal operating range, BDC starts the next charging cycle.

While in charging mode, depending on the measured dc bus voltage and the SoC of battery bank, the controller of BDC selects corresponding charging mode out of the three charging modes. A battery with low SoC draws a huge current compared to that with high SoC, so regulated constant current charging is required during low charge regime. For $50\% \leq \text{SoC} < 80\%$, battery starts charging in CC mode. Once SoC reaches 80%, the current drawn by battery becomes relatively small and the controller switches to CV charging mode until SoC equals to 95%. Beyond this SoC battery bank remains in float charging mode, and draws only a small amount of current, sufficient to compensate the battery internal losses. In the FC mode, the battery voltage remains constant equal to its float voltage V_{float} . The different modes of BDC operation are summarized in Table 5.2 and flowchart of the scheme is shown in Figure 5.11.

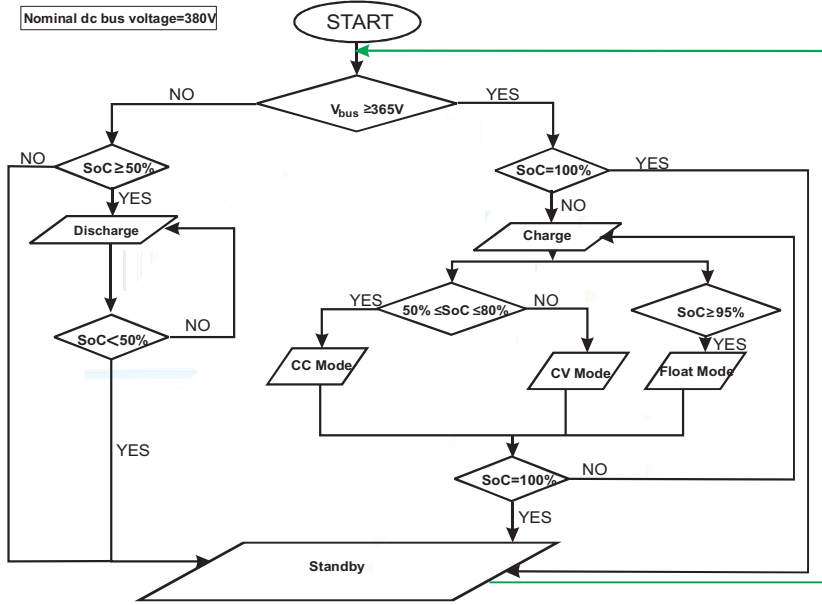


Figure 5.11 : Flow-chart of charging/discharging algorithm for bidirectional dc/dc converter

Table 5.2 : Different modes of operation of bidirectional dc/dc converter

Mode	V_{bus}	%SoC
Case:I (charging mode)	$\geq 365V$	≥ 50
(a) CC	$\geq 365V$	$50 \leq SoC < 80$
(b) CV	$\geq 365V$	$80 \leq SoC < 95$
(c) FC	$\geq 365V$	≥ 95
Case:II (discharging mode)	$< 365V$	≥ 50
Case:III (standby)	$< 365V$	< 50

(b) System operating modes

Depending on the power produced by the RESs, loading condition in the system, and the SoC of the battery bank, the system can operate in one of the following two operating modes.

Mode I: Normal operating mode

In this mode, the power produced by the RESs is greater than the load demand, therefore additional power is used to charge the ESU. The RES interfacing converters operating under voltage droop control are responsible for dc bus voltage regulation and BDC operates in one of the charging modes depending on the SoC of the battery bank. The dc microgrid continues to operate in this mode until the dc bus voltage drop below a threshold voltage ($V_{th} = 0.96v_{dc,ref}$). The dc bus voltage can drop below V_{th} due to the reduction in RES power or increased load demand. Once, dc bus voltage drops below V_{th} , the dc microgrid switches to mode II.

Mode II: Voltage regulation mode

In this operating mode, due to deficit of the power, the RES interfacing converters are unable to maintain the dc bus voltage. At this point, BDC switches to discharging mode and supports dc bus voltage regulation. The microgrid continues to operate in this mode until RES produce sufficient power to meet the load demand or battery bank hits the set threshold of DoD i.e. ($SoC < 50\%$).

5.2.2 Mathematical Modeling of Island DC Microgrid

In this section modeling of different components of the dc microgrid with reference to circuit diagram shown in Figure 5.10 is presented. The mathematical modeling of the load, RES interfacing converters, and BDC, presented in the following subsections will be used to design the sliding mode controllers in the next section.

(a) Load modeling

The total instantaneous current drawn by a mixed load from the dc bus is given by

$$i_{Load}(t) = \frac{v_{bus}(t)}{R_L} + \frac{P}{v_{bus}(t)}; \quad \forall \quad v_{bus}(t) > \varepsilon \quad (5.38)$$

where P is the combined rated power of two CPLs (CPL-1 and CPL-2), R_L is the resistance of the constant voltage load, and ε , is a small positive number.

(b) Modeling of RES interfacing converters

The nonlinear state-space averaged model of the RES interfacing converters is given in (5.39). The moving averages of capacitor voltage v_C , and inductor current i_{Lj} are chosen as state variables. Furthermore, the parasitic effects of the components are ignored.

$$\frac{di_{Lj}}{dt} = \frac{V_{pv,j}}{L_j} - \frac{(1-u_j)}{L_j} v_C; \quad j = 1, 2 \quad (5.39a)$$

$$\frac{dv_C}{dt} = \frac{1}{C_{eq}} \sum_{j=1}^2 (1-u_j) i_{Lj} - \frac{i_{oj}}{C_{eq}} \quad (5.39b)$$

where $u_j \in \{0, 1\}$, $V_{PV,j}$, L_j and i_{Lj} are the control input, input voltage (PV array voltage), inductance and the inductor current of j^{th} RES converter. v_C is the capacitor voltage which is equal to dc bus voltage $v_{bus} = v_{C1} = v_{C2} = v_{C3}$. The equivalent capacitance of the system is given by $C_{eq} = C_1 + C_2 + C_3 + C_{bus}$ (*additional bus capacitance, if any*).

As discussed in Section 5.1.1, the adaptive nonlinear voltage droop [Khorsandi et al., 2014] approach is used to ensure equal/proportional current sharing among RESs operating in parallel and the desired voltage regulation. Since the droop control results in an uncoupled system, the model of an individual RES converter is used to design the SMCs. The extended model of j^{th} RES converter after including the disturbance term $D(t)$, accounting for the impact of rest of the system together with load change, is given by

$$\frac{di_{Lj}}{dt} = \frac{V_{pvj}}{L_j} - \frac{\hat{u}_j}{L_j} v_C \quad (5.40a)$$

$$\frac{dv_C}{dt} = \frac{i_{Lj}}{C_{eq}} \hat{u}_j - \frac{i_{oj}}{C_{eq}} + \frac{D_j}{C_{eq}} \quad (5.40b)$$

$$\frac{dD_j}{dt} = \sigma_j (v_C - v_{Cref,j}) \quad (5.40c)$$

where $D_j = \sigma_j \int (v_C - v_{Cref,j}) dt$; $\sigma > 0$, $\hat{u}_j = 1 - u_j$, and i_{oj} are the disturbance effecting j^{th} RES converter, control input and output current of the j^{th} RES converter.

$$i_{oj} = b_j i_{load}; \text{ such that } \sum_{j=1}^2 b_j \pm b_{bdc} = 1 \quad (5.41)$$

where b_j is the fraction of total load current supplied by the j^{th} RES converter, and b_{bdc} is the fraction of the total load current supplied or drawn by the BDC.

(c) Modeling of bidirectional converter

In this section, modeling of BDC in different mode of operations is presented.

Charging Mode: During the charging mode, the BDC operates as a buck converter and power

flows from the dc bus to the battery bank. The state-space averaged model of the BDC in charging mode is given by

$$\frac{di_{L3}}{dt} = \frac{V_{bus}}{L_3} u_c - \frac{v_{C4}}{L_3} \quad (5.42a)$$

$$\frac{dv_{C4}}{dt} = \frac{i_{L3}}{C_4} - \frac{i_{bat}}{C_4} \quad (5.42b)$$

where i_{L3} is the inductor current of BDC, v_{C4} is the battery side capacitor (C_4) voltage, V_{bus} is the dc bus voltage, and i_{bat} is the charging current supplied to the battery bank.

Discharging mode: During discharging mode, BDC operates as a boost converter and power flows from the battery bank to the dc bus. The state-space averaged model of the BDC in discharging mode is given by

$$\frac{di_{L3}}{dt} = \frac{V_{bat}}{L_3} - (1 - u_d) \frac{v_C}{L_3} \quad (5.43a)$$

$$\frac{dv_C}{dt} = \frac{i_{L3}}{C_3} (1 - u_d) - \frac{i_{bdc}}{C_3} \quad (5.43b)$$

where v_C is the dc bus side capacitor (C_3) voltage, V_{bat} is the battery bank voltage, and i_{bdc} is the current supplied by BDC to dc bus. L_3 , C_3 , and C_4 are BDC's inductance, dc bus side and battery side capacitances respectively. u_c and $u_d \in \{0, 1\}$, are the control input in charging and discharging mode respectively. Furthermore, $i_{L3}, v_C, v_{C4} \in \Omega$, where set Ω is a subset of $\mathbb{R}^3$ i.e. $i_{L3}, v_C, v_{C4} \in \Omega \subseteq \mathbb{R}^3 \setminus \{0\}$

5.2.3 Sliding Mode Control Design

The control for RES interfacing converters and BDC are designed through SMC approach. To ensure constant frequency switching PWM based sliding mode controllers are proposed. In the following subsections, robust sliding mode controllers are proposed for RES converters and the BDC, interfacing battery bank.

(a) Control resign for RES interfacing converters

To derive the SMC for RES converters, an extended model of individual RES converters is used.

Switching function: The switching function is chosen such that supply of constant power to the load and zero steady state error in the dc bus voltage is ensured. The switching function s_j for j^{th} RES interfacing converter is given by

$$s_j := \beta_{1j}(v_C - v_{Cref,j}) + \beta_{2j}(i_{Lj} - i_{Lref,j}) + \beta_{3j}D_j \quad (5.44)$$

where $i_{Lref,j}$ is the reference value of the inductor current of j^{th} converter, and β_{1j} , β_{2j} , and β_{3j} are the positive constants. The second term in the switching function expression given in (5.44), requires reference inductor current which depends on input voltage, output voltage and the load, thus it is dynamic variable. The high pass filtered inductor current is used to estimate the inductor current error ($i_{Lj} - i_{Lref,j}$) [Santi et al., 2003; Mattavelli et al., 1993].

Control law: The reaching dynamics defining the evolution of the switching function s must ensure the motion of the system trajectory from an arbitrary point on to the switching surface $s = 0$ in finite time. The chosen reaching dynamics defining the evolution of the switching function is given by,

$$\dot{s}_j = -\lambda_j s_j - Q_j \text{sgn}(s_j) \quad (5.45)$$

where $\lambda_j > 0$ is the parameter which controls the convergence speed and $Q_j > 0$, which depends on the magnitude of uncertainty. It is straightforward to prove the reachability condition $s^T \dot{s} < -\eta |s|$; $\eta > 0$ for reaching dynamics of (5.45). Substituting (5.40) and (5.44) into (5.45)

and solving for $u(\hat{t})$ results the following instantaneous duty cycle expression

$$\hat{u}_j(t) = \frac{\lambda_j s_j + Q_j \text{sgn}(s_j) + \frac{\beta_{1j} D_j}{C_{eq}} + \frac{\beta_{2j} V_{pv,j}}{L_j}}{\frac{\beta_{2j}}{L_j} v_C - \frac{\beta_{1j}}{C_{eq}} i_{Lj}} + \frac{\beta_{3j} \sigma_j (v_C - v_{Cref,j}) - \frac{\beta_{1j} i_{oj}}{C_{eq}}}{\frac{\beta_{2j}}{L_j} v_C - \frac{\beta_{1j}}{C_{eq}} i_{Lj}} \quad (5.46)$$

The control law given in (5.46), is obtained by considering the generalized load profile. The control for a specific load model can be obtained by substituting respective load model in (5.46).

The control law (5.46) forces the system trajectory from an arbitrary point on to the switching surface $s = 0$ and maintains the system trajectory on $s = 0$ then on. The voltage reference $v_{Cref,j}$ to each converter is modified to ensure desired voltage regulation and equal/proportional current sharing according to the adaptive nonlinear droop characteristics (5.6). Droop characteristics of (5.6) is to be substituted into (5.46) to get the final expression of the control law. Furthermore, the values of the droop coefficient of the two converters should be same to ensure equal current sharing.

(b) Control design for BDC

The sliding mode controllers for different mode of operations of BDC are proposed in the following subsection.

Switching function: To implement the charging and discharging algorithm presented in the Section 5.2.1, the sliding mode controller of BDC uses three switching functions and facilitates desired mode transitions. The following three switching functions are defined

- (1) Switching function for constant current and float charging modes is given by

$$s_{c,ccf} = \alpha_{c,ccf}(i_{L3} - i_{Lref,3}) + D_c \quad (5.47)$$

- (2) Switching function for constant voltage mode is given by

$$s_{c,cv} = i_{L3} v_{C4} - i_{Lref,3} v_{Cref,4} + \alpha_{c,cv}(v_{C4} - v_{Cref,4}) + D_c \quad (5.48)$$

- (3) Switching function for discharging mode is given by

$$s_d = i_{L3} v_C - i_{Lref,3} v_{Cref} + \alpha_d(v_C - v_{Cref}) + D_d \quad (5.49)$$

where $D_c = \sigma_c \int (v_{C4} - v_{Cref,4}) dt$; $\sigma_c > 0$ and $D_d = \sigma_d \int (v_C - v_{Cref}) dt$; $\sigma_d > 0$ are the disturbances which account for the influence of rest of the system and changes in load, in charging and discharging mode respectively. $i_{Lref,3}$ is the reference value of inductor current for inner loop current control and, $v_{Cref,4}$ and $v_{Cref,3}$ are the reference values of battery side capacitor voltage and dc bus side capacitor voltage respectively for outer loop voltage control. $\alpha_{c,ccf}$, $\alpha_{c,cv}$ and α_d are the switching function parameters.

Control law: In this section, control laws using switching functions defined in the previous subsection are derived. The control laws force the system trajectory from an arbitrary initial point, on to the switching surface ($s = 0$) and constrains it to the switching surface then on. The PWM based sliding mode controllers for BDC are designed through reaching dynamics approach. The chosen reaching dynamics is given by

$$\dot{s}_3 = -\lambda_3 s_3 - Q_3 \text{sgn}(s_3) \quad (5.50)$$

where λ_3 , $Q_3 > 0$ and s_3 ($s_{c,ccf}$, $s_{c,cv}$ and s_d) are the parameters of reaching dynamics and switching function corresponding to the BDC. It is straightforward to prove the reachability condition $s^T \dot{s} < -\eta |s|$; $\eta > 0$ using reaching dynamics of (5.50).

To derive the control laws for different modes of the BDC, extended model corresponding to the respective mode, similar to extended model of RES converter of (5.40), is obtained

separately for charging and discharging mode using disturbances D_c and D_d respectively. The instantaneous duty $u_{c,ccf}$ for constant current and float mode charging using (5.42), (5.47) and (5.50) is given by

$$u_{c,ccf} = \frac{v_{C4}}{V_{bus}} + \frac{-L_3(\lambda_3 s_{c,ccf} + Q_3 \text{sgn}(s_{c,ccf}) + \sigma_c(v_{C4} - v_{Cref,4}))}{\alpha_{c,ccf} V_{bus}} \quad (5.51)$$

The same constant current charging controller can be used for float charging. The controller automatically changes its charging current reference (constant current to float charge current reference) using the proposed charging algorithm. The instantaneous duty $u_{c,cv}$ for constant voltage mode charging using (5.42), (5.48) and (5.50) is given by,

$$\begin{aligned} u_{c,cv} &= \frac{v_{C4}}{V_{bus}} - \frac{L_3(i_{L3} + \alpha_{c,cv})(i_{L3} - i_{bat} + D_c)}{C_3 v_{C4} V_{bus}} \dots \\ &\dots + \frac{-L_3(\lambda_3 s_{c,cv} + Q_3 \text{sgn}(s_{c,cv})) + \sigma_c(v_{C4} - v_{Cref,4})}{v_{C4} V_{bus}} \end{aligned} \quad (5.52)$$

Similarly, using (5.43), (5.49) and (5.50), the instantaneous duty cycle u_d for discharging mode is given by

$$\begin{aligned} u_d &= \frac{C_3(v_C^2 - v_C V_{bat}) - L_3(i_{L3} + \alpha_d)(i_{L3} - i_{bdc} + D_d)}{C_3 v_C^2 - L_3 i_{L3}(i_{L3} + \alpha_d)} \dots \\ &\dots + \frac{-C_3 L_3^2(\lambda_3 s_d + Q_3 \text{sgn}(s_d)) + \sigma_d(v_C - v_{Cref,3})}{C_3 v_C^2 - L_3 i_{L3}(i_{L3} + \alpha_d)} \end{aligned} \quad (5.53)$$

The instantaneous duty cycles represented by the equations (5.46), (5.51), (5.52), and (5.53) are then compared with repetitive triangular signal of desired switching frequency to generate fixed frequency PWM pulses for the BDC.

5.2.4 Stability on Switching Surface

In this section, stability of the converter's dynamics during sliding mode $s = 0$ will be established. Stability of the RES converters and the BDC will be discussed separately, considering the influence of the disturbance of the rest of the system, on the respective converter.

(a) Stability of RES Interfacing Converters on Switching Surface

The reduced order dynamics of the first RES converter during sliding mode $s_1 = 0$ is given by

$$i_{L1} = -\frac{\beta_{11}}{\beta_{21}}(v_C - v_{Cref,1}) - \frac{\beta_{31}}{\beta_{21}}D_1 + i_{Lref,1} \quad (5.54a)$$

$$\frac{dv_C}{dt} = \frac{\hat{u}_1}{C_{eq}} i_{L1} - \frac{i_{o1}}{C_{eq}} \quad (5.54b)$$

$$\frac{dD_1}{dt} = \sigma_1(v_C - v_{Cref,1}) \quad (5.54c)$$

Eliminating i_{L1} and incorporating voltage droop equation (5.6), the reduced order dynamic model becomes

$$\begin{aligned} C_{eq} \frac{dv_C}{dt} + \frac{\beta_{11}}{\beta_{21}} \hat{u}_1 (v_C - v_{dc,ref} + \kappa_1 i_{o1}^{\xi_1}) + \frac{\beta_{31}}{\beta_{21}} \hat{u}_1 \sigma_1 \int (v_C - v_{dc,ref} + \kappa_1 i_{o1}^{\xi_1}) dt \dots \\ \dots - i_{Lref,1} + i_{o1} = 0 \end{aligned} \quad (5.55)$$

substituting i_{o1} in terms of total load current from (5.41) and differentiating (5.55) with respect to time, (5.55) becomes.

$$\begin{aligned} C_{eq} \frac{d^2 v_C}{dt^2} + \frac{\beta_{11}}{\beta_{21}} \hat{u}_1 \frac{dv_C}{dt} + \frac{\beta_{11}}{\beta_{21}} \hat{u}_1 \kappa_1 b_1^{\xi_1} \frac{di_{load}^{\xi_1}}{dt} + \frac{\beta_{31}}{\beta_{21}} \hat{u}_1 \sigma_1 v_C - \dots \\ \dots \frac{\beta_{31}}{\beta_{21}} \hat{u}_1 \sigma_1 v_{dc,ref} + \frac{\beta_{31}}{\beta_{21}} \hat{u}_1 \sigma_1 \kappa_1 b_1^{\xi_1} i_{load}^{\xi_1} + b_1 \frac{di_{load}}{dt} = 0 \end{aligned} \quad (5.56)$$

Considering linear approximation of the load current $i_{load}(v_C)$, we can write.

$$\begin{aligned} i_{load} &\approx \frac{\partial i_{load}}{\partial v_C} v_C \\ \frac{di_{load}}{dt} &\approx \frac{\partial i_{load}}{\partial v_C} \frac{dv_C}{dt} \end{aligned} \quad (5.57)$$

Substitution of (5.57) into (5.56), and assuming $\xi = 1$ to simplify (5.56), results in

$$\begin{aligned} C_{eq} \frac{d^2 v_C}{dt^2} + \left(\frac{\beta_{11}}{\beta_{21}} \hat{u}_1 + \frac{\beta_{11}}{\beta_{21}} \hat{u}_1 \kappa_1 b_1 \frac{\partial i_{load}}{\partial v_C} + b_1 \frac{\partial i_{load}}{\partial v_C} \right) \frac{dv_C}{dt} \dots \\ \dots + \left(\frac{\beta_{31}}{\beta_{21}} \hat{u}_1 \sigma_1 + \frac{\beta_{31}}{\beta_{21}} \hat{u}_1 \sigma_1 \kappa_1 b_1 \frac{\partial i_{load}}{\partial v_C} \right) v_C = \frac{\beta_{31}}{\beta_{21}} \hat{u}_1 \sigma_1 v_{dc,ref} \end{aligned} \quad (5.58)$$

For the stability of the system on the switching surface $s = 0$, following conditions must be satisfied.

$$\frac{\beta_{11}}{\beta_{21}} \hat{u}_1 + \left(b_1 + \frac{\beta_{11}}{\beta_{21}} \hat{u}_1 \kappa_1 b_1 \right) \frac{\partial i_{load}}{\partial v_C} > 0 \quad (5.59a)$$

$$\frac{\beta_{31}}{\beta_{21}} \hat{u}_1 \sigma_1 + \frac{\beta_{31}}{\beta_{21}} \hat{u}_1 \sigma_1 \kappa_1 b_1 \frac{\partial i_{load}}{\partial v_C} > 0 \quad (5.59b)$$

Considering the load profile of (5.38)

$$\frac{\partial i_{load}}{\partial v_C} = \frac{1}{R_L} - \frac{P}{v_{dc,ref}^2} \quad (5.60)$$

where $v_{dc,ref}$ is nominal value of the dc bus voltage. Substituting (5.60) into (5.59) implies

$$\frac{\beta_{11}}{\beta_{21}} \hat{u}_1 + \left(b_1 + \frac{\beta_{11}}{\beta_{21}} \hat{u}_1 \kappa_1 b_1 \right) \left(\frac{1}{R_L} - \frac{P}{v_{dc,ref}^2} \right) > 0 \quad (5.61a)$$

$$\frac{\beta_{31}}{\beta_{21}} \hat{u}_1 \sigma_1 + \frac{\beta_{31}}{\beta_{21}} \hat{u}_1 \sigma_1 \kappa_1 b_1 \left(\frac{1}{R_L} - \frac{P}{v_{dc,ref}^2} \right) > 0 \quad (5.61b)$$

Let

$$K_1 := \frac{\beta_{11} \hat{u}_1}{\beta_{21} b_1 + \beta_{11} \hat{u}_1 \kappa_1 b_1}; \text{ and } K_2 := \frac{1}{\kappa_1 b_1} \quad (5.62)$$

Simplifying (5.61) using (5.62), we get

$$\frac{P}{v_{dc,ref}^2} - \frac{1}{R_L} < K_1; \text{ and } \frac{P}{v_{dc,ref}^2} - \frac{1}{R_L} < K_2 \quad (5.63)$$

Therefore, in order to ensure stability, the following condition must satisfy.

$$\frac{P}{v_{dc,ref}^2} - \frac{1}{R_L} < K; \text{ where } K = \text{Min}\{K_1, K_2\} \quad (5.64)$$

It implies

$$P < v_{dc,ref}^2 \left(\frac{1}{R_L} + K \right) \quad (5.65)$$

It can be seen from (5.65) that, the limit on CPL component of the load depends on power consumed by the resistive component, nominal dc bus voltage, and K . In the worst case, when the minimum value of K is zero (with $\hat{u}_1 = 0$ i.e. $u_1 = 1$), to ensure the stability of the system CPL power must be less than the power consumed by the resistive component of the load. All other cases will result in higher limits on CPL power. Same method can be applied to prove the stability of second RES converter.

(b) Stability of BDC on Switching Surface

The reduced order dynamics of the BDC during sliding mode and CC charging mode with $s_{c,ccf} = 0$ is given by

$$i_{L3} = -\frac{1}{\alpha_{c,ccf}} D_c + i_{Lref,1} \quad (5.66a)$$

$$\frac{dv_{C4}}{dt} = \frac{1}{C_4} i_{L3} - \frac{i_{bdc}}{C_4} \quad (5.66b)$$

$$\frac{dD_c}{dt} = \sigma_c (v_{C4} - v_{Cref,4}) \quad (5.66c)$$

while obtaining (5.66) using (5.42) i_{bat} is replaced with i_{bdc} , as during charging (buck) mode, the magnitude of i_{bat} and i_{bdc} is same. Following the procedure of the previous subsection, the reduced order dynamics of BDC in CC charging mode is given by

$$C_{eq} \frac{d^2 v_{C4}}{dt^2} + b_{bdc} \frac{\partial i_{load}}{\partial v_C} + \frac{\sigma_c}{\alpha_{c,ccf}} v_{C4} = \frac{\sigma_c}{\alpha_{c,ccf}} v_{Cref,4} \quad (5.67)$$

For the stability of the system on the switching surface $s = 0$, following conditions must be satisfied.

$$b_{bdc} \frac{\partial i_{load}}{\partial v_C} > 0 \quad (5.68a)$$

$$\frac{\sigma_c}{\alpha_{c,ccf}} > 0 \quad (5.68b)$$

In CC charging mode the battery bank behaves as a constant current load, it implies

$$\frac{\partial i_{load}}{\partial v_C} = 0 \quad (5.69)$$

Therefore, in order to ensure stability, the following condition must be satisfied.

$$\frac{\sigma_c}{\alpha_{c,ccf}} > 0 \quad (5.70)$$

It implies that BDC in CC mode is stable, as by definition σ_c and $\alpha_{c,ccf}$ are positive.

For CV charging and discharging operating of the BDC a nonlinear switching functions have been used. Similar switching function has been used for designing a sliding mode controller for buck converter feeding resistive and CPL (Chapter 3) and boost converter feeding a pure a CPL (Chapter 2). The BDC in charging and discharging mode operates as buck and boost converter respectively. Therefore, for stability proof in CV mode and discharging mode Section 3.2.1 and Section 2.2.1 of Chapter 3 and Chapter 2 respectively, can be referred.

5.2.5 Simulation Studies and Experimental Results

The validation of the proposed nonlinear control scheme using SMC to mitigate the destabilizing effects of CPLs and to control the dc bus voltage in an islanded DCMG, is presented in this section using simulation studies and experimental results.

(a) Simulation studies

The specifications of the test dc microgrid and controller parameters are provided in Table 5.3. In simulation studies, loads CPL-1 and CPL-2 have been modeled as an ideal CPL. The solar PV arrays have been modeled with matching parameters that of actual rooftop PV modules (Moser Baer's Power Series FS Bin 380), used in the experimental setup. A constant solar irradiance of 800 W/m^2 is considered for both PV arrays.

Table 5.3 : Specifications and controller parameters of realized dc microgrid

Parameter(s)	Value(s)
PV Array 1,2	$V_{oc} = 187.8 \text{ V}$, $I_{sc} = 6.54 \text{ A}$, $P_{max} = 760 \text{ W}$
C_1 , C_2 , C_3 , and C_4	Each of $47 \text{ } \mu\text{F}$
L_1 , L_2 , and L_3	Each of 2.2 mH
Battery bank	10 batteries of 12 V , 26 Ah (in series)
R , $CPL-1$, and $CPL-2$	$512 \text{ } \Omega$, 300 W , and 585 W
Nominal dc bus voltage, $V_{dc,ref}$	380 V
β_1 , β_2 , and β_3	100, 400, and 10
λ_1 and Q_1	2000 and 0.2
$\kappa_1 = \kappa_2$ and $\xi_1 = \xi_2$	0.7 and 1.33
$\alpha_{c,ccf}$, $\alpha_{c,cv}$, and α_d	1290, 1000, and 27×10^4
η , η_c , and η_d	3000, 2000, and 2000
λ_2 and Q_2	2500 and 3×10^5
C_{bus}	$2000 \text{ } \mu\text{F}$
Switching frequency, f_s	25 kHz

To validate the steady-state and dynamic performance of the system with the proposed control, it is considered that initially system is feeding a mixed load ($R_L = 512 \text{ } \Omega$ and $CPL-2=585 \text{ W}$) and then $CPL-1$ of 300 W is switched on at $t = 0.25 \text{ s}$. Simulation results corresponding to the above operating condition are shown in Figure 5.12. Figure 5.12(a) shows that the steady-state value of dc bus voltage is 363 V , which reduces to 362.4 V (voltage regulation=4.6 %) when $CPL-1$ is switched on at $t = 0.25 \text{ s}$. The voltages of both PV arrays (V_{pv1} , V_{pv2}) and battery bank (V_{bat}) are 152.75 V and 130.5 V respectively, and reduce slightly in response to load change at $t = 0.25 \text{ s}$. Figure 5.12(b) shows contributions of RES converters and BDC (working in discharging mode) in the load current, and current supplied by the battery bank. In response to load change at $t = 0.25 \text{ s}$, the RES interfacing converters and BDC accordingly increase their output currents. Furthermore, it can be seen that the RES converters supply equal currents. Figure 5.12(c) shows corresponding inductor currents of the RES converters and BDC. Figure 5.12(d) shows individual currents drawn by the three load components. It can be observed that in response to reduction in the dc bus voltage due to load change at $t = 0.25 \text{ s}$, the current drawn by resistive load reduces and that of $CPL-2$ increases.

In the next subsection, experimental results are presented to validate the performance of the proposed control scheme. In addition to the above operating condition, various other operating conditions were considered while obtaining the experimental results.

(b) Experimental validation

An experimental setup of the dc microgrid as shown in Figure 5.13 was developed and tested in the laboratory. Two PV arrays, each of 760 W maximum power were interfaced to dc bus through dc/dc boost converters. A BDC was used to interface battery bank of 120 V , 26 Ah to the dc bus, to facilitate bidirectional power exchange between dc bus and the battery bank. The load in the system consists of a resistive load (programmable dc load in *Constant Resistance* mode), $CPL-1$ (programmable dc load working in *constant power load* mode), and $CPL-2$ is a speed controlled dc/ac inverter drive. An image of the experimental setup is shown in Figure 5.13.

The proposed controllers have been realized through ORDS. The ORDS system, is a high end real-time computation system with large number of analog and digital I/Os to

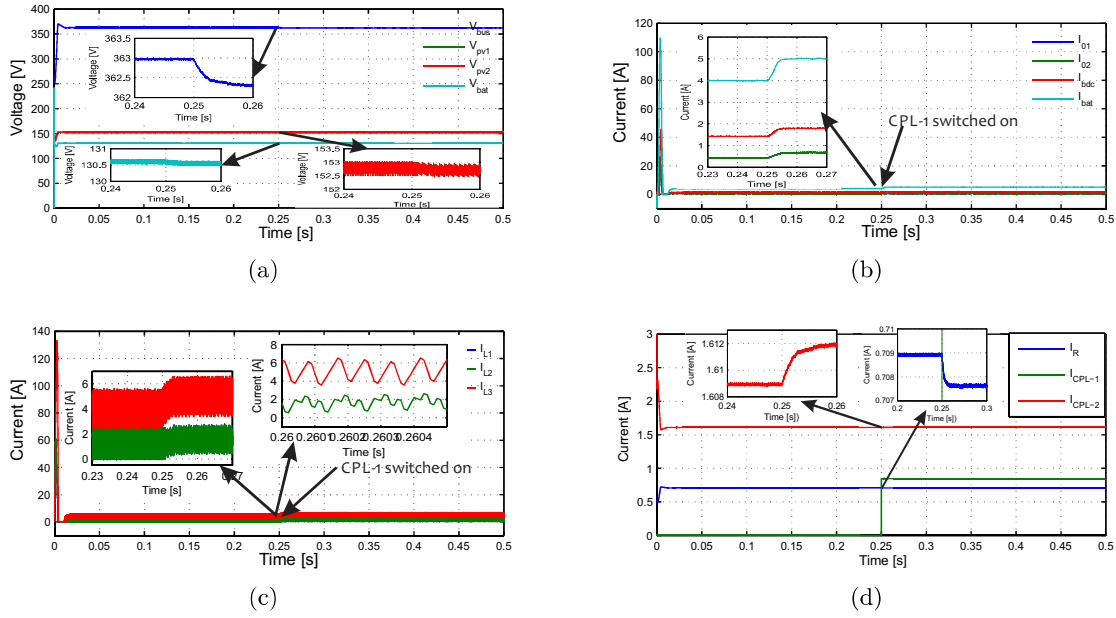


Figure 5.12 : Simulation results with the proposed SMC: System feeding a mixed load (resistive + CPL-2) with BDC in discharging mode, and CPL-1 is switched on at $t = 0.25$ s; (a) V_{bus} , V_{pv1} , V_{pv2} , and V_{bat} ; (b) I_{01} , I_{02} , I_{dc} , and I_{bat} ; (c) I_{L1} , I_{L2} , and I_{L3} ; (d) I_R , I_{CPL-1} and I_{CPL-2}

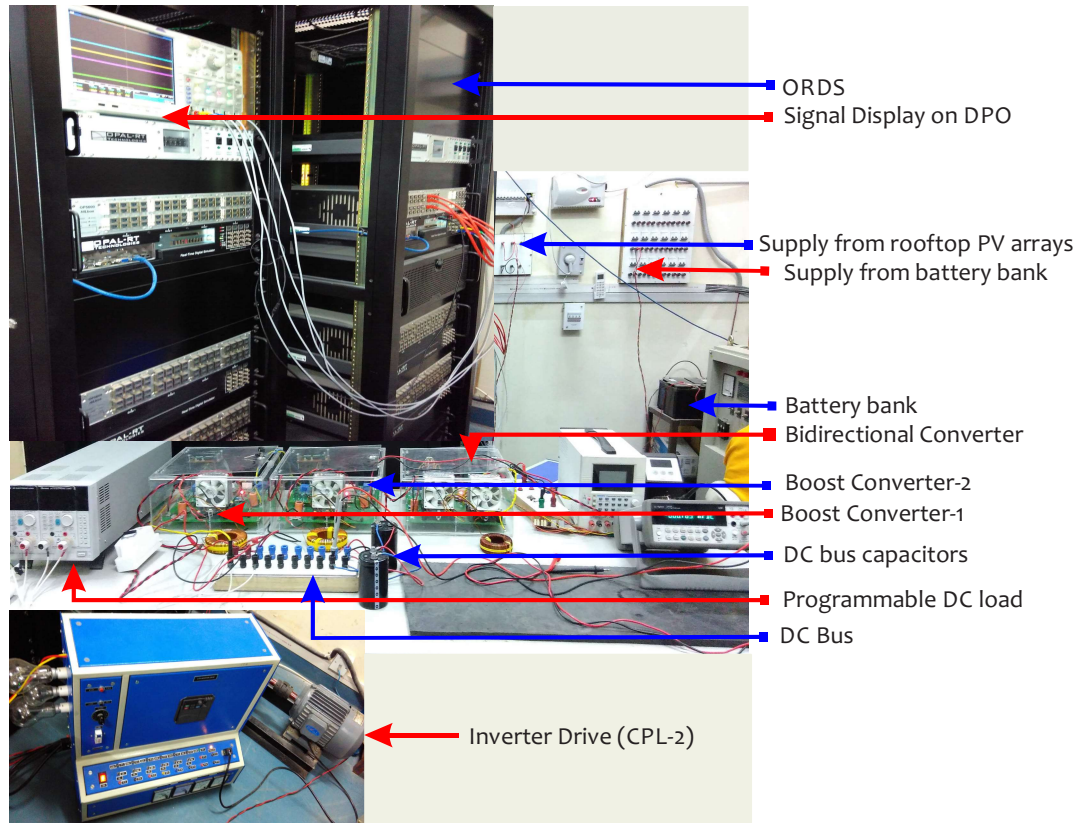


Figure 5.13 : An image of the experimental setup of islanded dc microgrid

interface real hardware or to conduct real-time simulation studies. The acceptable signal range of I/Os is ± 16 V. The desired model intended to run on ORDS is to be modeled in *MATLAB/SIMULINKTM* environment and loaded to the simulator using RT-Lab software. The proposed sliding mode control scheme was modeled in *MATLAB/SIMULINKTM*. The required state variables were sensed and interfaced to the controller through analog inputs and computed control inputs for the system are made available at digital output ports. The values of the controller parameters and references are supplied by the user.

A fixed step size of $10 \mu s$ is used to compute the proposed controllers. The monitored system variables for display and analysis purpose are obtained from analog outputs of ORDS. The values of some of the monitored variables were scaled down to comply I/O ports specifications. Therefore, displayed variables have to be multiplied by their respective scaling factors provided in Table 5.4, to get their actual values.

Table 5.4 : Scaling factors to determine actual values of the variables

Variables	Scaling factor
V_{bus} , V_{pv1} , V_{pv2} , and V_{bat}	40, 20, 20, and 15
All currents	1

To validate the steady state and dynamic performance of the proposed robust SMC scheme, the experimental results were obtained under the following operating conditions

1. System is feeding a resistive load ($R_L = 508 \Omega$), with BDC in CV charging mode.
2. System is feeding a resistive load ($R_L = 508 \Omega$) and CPL-1 (300 W), with BDC in CV charging mode.
3. System is feeding a resistive load ($R_L = 508 \Omega$) and CPL-1 (300 W), with BDC in CC charging mode.
4. System is feeding a resistive load ($R_L = 508 \Omega$) and CPL-1 (200 W), with BDC in float mode.
5. System is feeding a mixed load ($R_L = 508 \Omega$ and inveter drive drawing 1.6A) and then CPL-1 of 300 W switched on, with BDC in discharging mode.

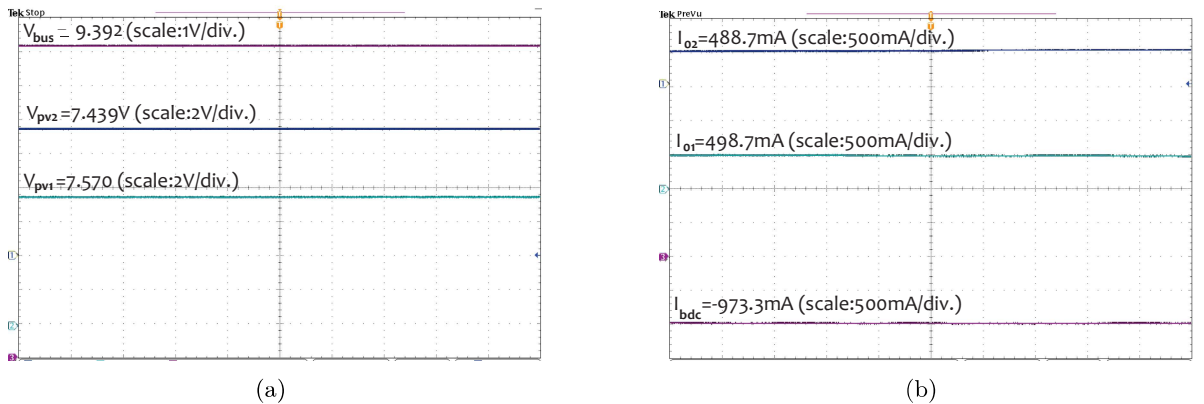


Figure 5.14 : Experimental results with the proposed SMC corresponding to the Operating Condition 1: (a) V_{bus} , V_{pv1} , and V_{pv2} ; (b) I_{o1} , I_{o2} , and I_{bdc}

Figure 5.14 shows plots corresponding to the Operating Condition: 1. It can be observed from Figure 5.14(a) that value of dc bus voltage is 375.68 V (*voltage regulation* = 1.14 %)

and PV array voltages are 155 V and 148.78 V respectively. Figure 5.14(b) shows output current of the two RES converters and a current of (973.3 mA) drawn by BDC from dc bus. It can be seen that the difference in the currents supplied by two RES converters is very small 10 mA. Results corresponding to the Operating Condition: 2 are shown in Figure 5.15. The value of dc bus voltage is 369.64 V (*voltage regulation* = 2.73 %) and PV array voltages are 141 V and 145.34 V respectively (Figure 5.15(a)). Figure 5.15(b) shows output current of the two RES converters and a current of (561.5 mA) drawn by the BDC from dc bus. It can be seen that the difference in the currents supplied by two RES converters is negligible 3.5 mA.

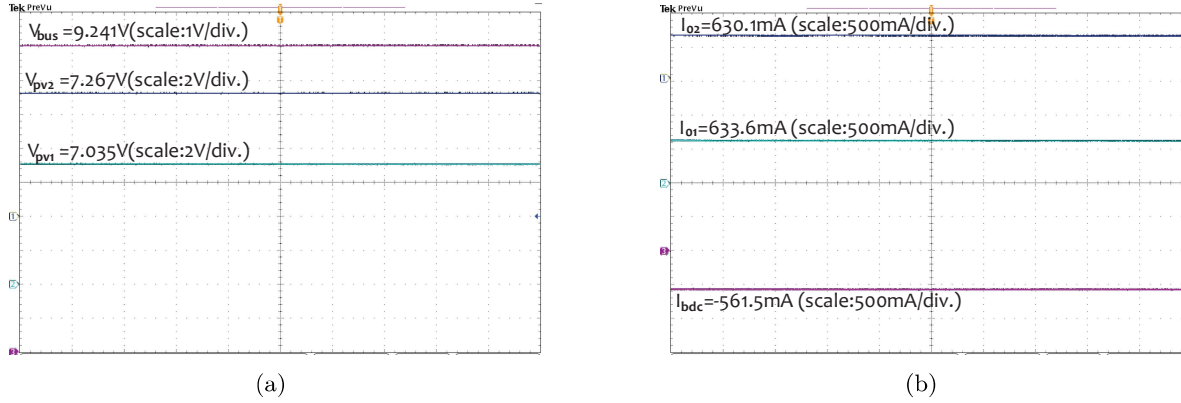
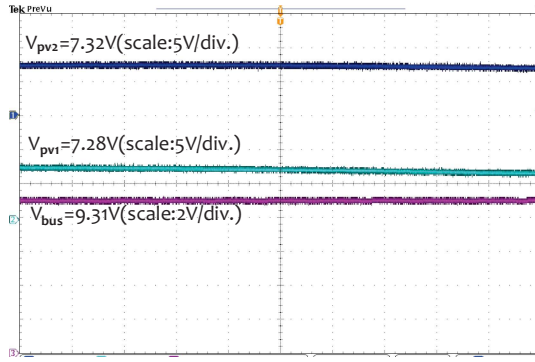


Figure 5.15 : Experimental results with the proposed SMC corresponding to the Operating Condition 2: (a) V_{bus} , V_{pv1} , and V_{pv2} ; (b) I_{o1} , I_{o2} , and I_{bdc}

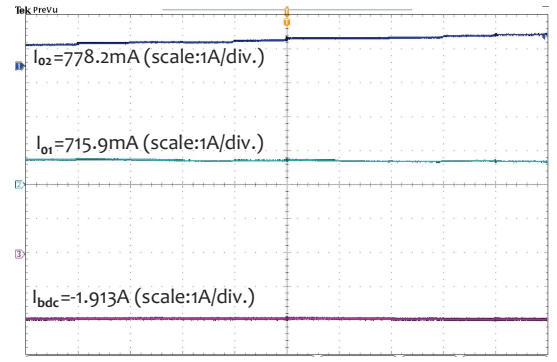
Responses of different voltages and currents for the Operating Condition: 3 are shown in Figure 5.16. Figure 5.16(a) shows dc bus voltage of 372.4 (*voltage regulation* = 2 %), and PV array voltages of 145.6 V and 146.4 V respectively. RES converter's output currents (715.9 mA, 778.2 mA) and the current drawn by the BDC (1.913 A) are shown in Figure 5.16(b). Figure 5.16(c) shows inductor currents of RES interfacing converters, and Figure 5.16(d) shows battery bank voltage (116.85V) and its charging current.

The system response corresponding to the Operating Condition: 4 is shown in Figure 5.17. The value of the dc bus voltage in this case is 366 V (*voltage regulation* = 3.6 %). It can be observed that BDC draws small amount of current (21.49mA) as it is working in float charging mode. The output currents of RES interfacing converters, PV array voltages and battery voltages are also shown in Figure 5.17. To validate the dynamic response of the system to the changes in load, experimental results were obtained under the Operating Condition: 5 as shown in Figure 5.18. The dc bus voltage is 364.8 V (*voltage regulation* = 4%) and it reduces slightly when CPL-1 is switched on. The output currents of both RES interfacing converters (I_{o1} , I_{o2}) and BDC (I_{bdc}), increase in response to the increased load current. It can be seen that in this case BDC is operating in discharging mode.

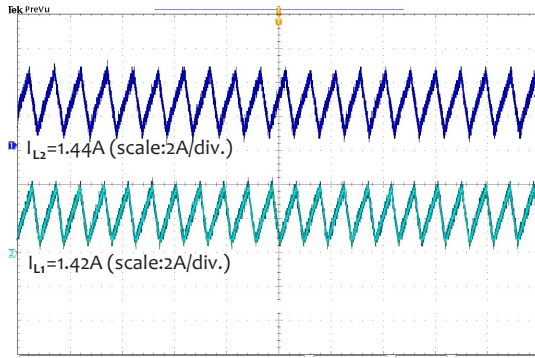
The above simulation studies and experimental results validate the effectiveness of the proposed robust sliding mode control scheme to control an isolated dc microgrid during different operating modes. The proposed control ensures desired voltage regulation (< 5 %) and stability of the system under various operating conditions, in the presence of constant power loads.



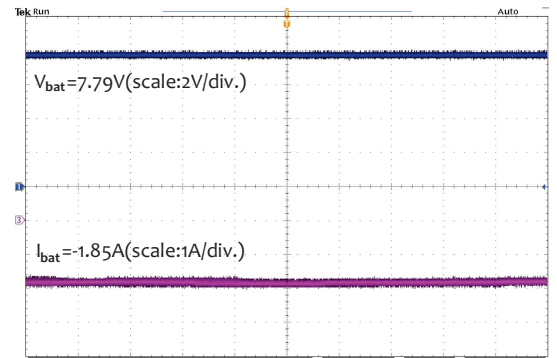
(a)



(b)

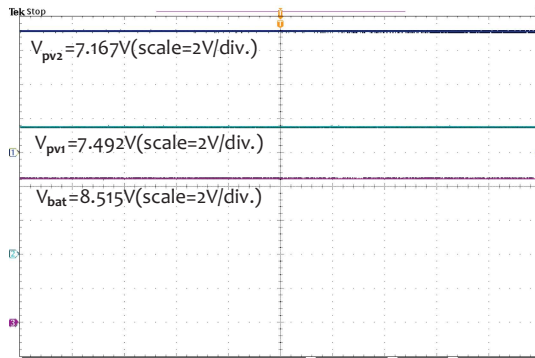


(c)

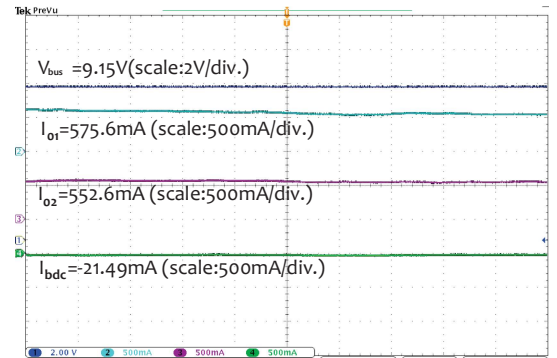


(d)

Figure 5.16 : Experimental results with the proposed SMC corresponding to the Operating Condition 3: (a) V_{pv1} , V_{pv2} , and V_{bat} ; (b) V_{bus} , I_{01} , I_{02} , and I_{dc} ; (c) I_{L1} and I_{L2} ; (d) V_{bat} and I_{dc}



(a)



(b)

Figure 5.17 : Experimental results with the proposed SMC corresponding to the Operating Condition 4: (a) V_{pv1} , V_{pv2} , and V_{bat} ; (b) V_{bus} , I_{01} , I_{02} , and I_{dc}

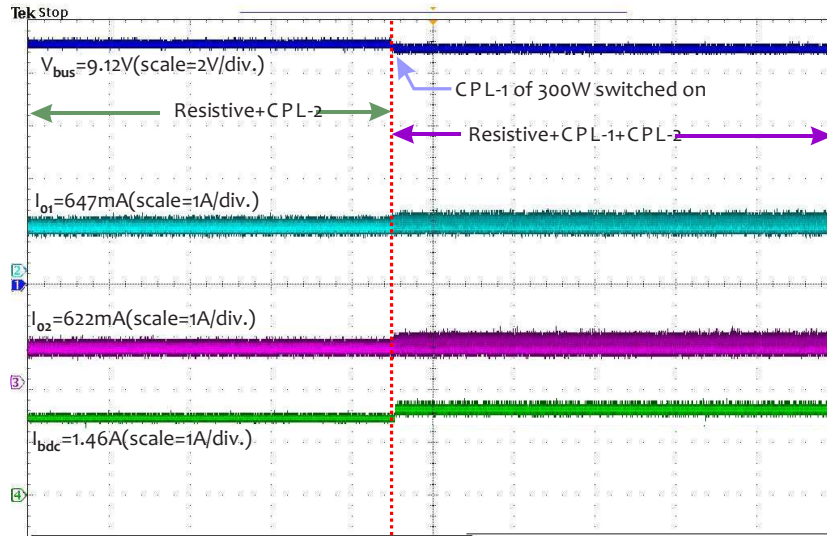


Figure 5.18 : Experimental results with the proposed SMC corresponding to the Operating Condition 5: Dynamic response of (V_{bus} , I_{o1} , I_{o2} , and I_{bdc})

5.3 SUMMARY

In this chapter robust sliding mode control scheme for an islanded dc microgrid feeding a composite load has been proposed. The composite load profile takes into account a typical load profile supplied by a practical dc microgrid. A limit on the CPL power to ensure stable operation has also been established. The effects of the primary source dynamics on the controller performance have been taken into account by using the realistic PV array model. The presented control scheme has been validated through real-time simulation studies using OPAL-RT Digital Simulator under a wide range of operating conditions. The proposed control scheme has been found to be robust with respect to variations in the input voltage, system parameter, and the load. The controller also ensures tight regulation of the dc bus voltage and stability under various operating modes.

Furthermore, in the second section of the chapter, a nonlinear control scheme using robust sliding mode control approach has been presented to mitigate the destabilizing effect of CPLs in an actual islanded dc microgrid. Stability of the system has been established analytically and validated through simulation studies and experimental results. The effectiveness of the proposed control has been validated through simulation studies and experimental results. It has been shown through simulation studies and experimental results that the proposed control scheme ensure stabilized dc bus voltage, i.e. it does not show any destabilizing effect of CPLs, under different operating conditions. It has been found that the proposed control ensures voltage regulation of less than 5% and is robust to changes in the load. To demonstrate the performance of the implemented charging/discharging algorithm for bidirectional dc/dc converter, experimental results have been obtained showing its operation in different operating modes. In the next chapter, contributions of the work presented in this Thesis will be concluded.

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