# 2
# AlGaN/GaN HEMT devices

HEMTs are well known devices used in applications that require high speed operation. Besides AlGaN/GaN system, AlGaAs/GaAs system is also well known in HEMTs. Enhancement of carrier mobility in HEMTs relies on reduction in carrier scattering caused by dopant ions. In order to achieve this objective, modulation doping is commonly employed, e.g., doping of AlGaAs barrier layer close to the AlGaAs/GaAs hetero-interface. This modulation doping in turn induces carriers in the un-doped GaAs channel region. For n-type doping in barrier, barrier region close to the interface is depleted and the corresponding electrons accumulate in a triangular shaped potential well in the GaAs layer close to the interface. Accumulation of electrons in triangular shaped potential well in the GaAs layer results in a two-dimensional electron gas (2-DEG) with electrons having an increased mobility in comparison to electrons in the bulk of the active layer. This increased mobility results from the carriers being spatially separated from dopants in the barrier layer. A similar HEMT structure can be realized using AlGaN/GaN hetero-structure. Compared to GaAs, bulk mobility in GaN is much lower due to an approximately three times higher effective electron mass in GaN as compared to GaAs. However, GaN has a larger peak electron velocity, larger saturation velocity, higher thermal stability, and a larger band gap making it suitable for use as a channel material in microwave power devices [Ambacher *et al.* 1999a]. In addition to this, AlGaN/GaN HEMTs are known to achieve 2-DEG with sheet carrier concentrations of ~$10^{13}$ $cm^{-2}$ or higher close to the interface without any intentional doping resulting in channel electron mobility in range of 1500-2000 $cm^2/V.s$ [Shen *et al.* 2001a]. Further, this sheet carrier concentration is well in excess of those achievable with other III-V material systems [Ambacher *et al.* 1999a]. In this chapter, several physical aspects of the working of AlGaN/GaN HEMT device are discussed along with a discussion on several other design parameters. A brief account on reliability of these devices is presented while highlighting the role of TCAD analysis to address the reliability concerns.

## 2.1 SOURCE OF 2-DEG IN ALGAN/GAN HEMT SYSTEM

Unique properties of AlGaN/GaN system allow designing devices with high sheet carrier density even without any need for doping of AlGaN barrier. This presence of sheet charge density is attributed to presence of polarization field in these group III-Nitride compounds and also shows dependence on surface properties, explained as follows:

### 2.1.1 Polarization in group III-Nitride compounds

Absence of inversion symmetry in GaN results in polarization field in these devices. In the absence of external electric fields, the total macroscopic polarization P of a GaN or AlGaN layer is the sum of spontaneous polarization ($P_{SP}$) in the equilibrium lattice, and the strain induced or piezoelectric polarization ($P_{PE}$). The spontaneous and piezoelectric polarization in wurtzite GaN and AlN is about 10 times larger than in conventional III-V and II-VI semiconductor compounds [Ambacher *et al.* 1999a]. The spontaneous polarization can cause electric fields of up to 3 MV/cm in group III-Nitride crystals, and strain in the pseudo morphically grown AlGaN/GaN or InGaN/GaN heterostructures can cause an additional piezoelectric field of about 2 MV/cm [Ambacher *et al.* 1999a]. These very high polarizations and resulting high electric field are considered to be responsible for high interface charge densities at group III-Nitride interfaces.

However, the type of charge at the interfaces depends on the direction of polarization which in turn is a function of crystallographic orientation. For GaN heterostructures with Ga-face, the spontaneous polarization is directed towards the substrate whereas it is directed towards the surface for N-faced GaN. With the help of polarization induced charges, Ambacher et al. were able to explain the channel formation in AlGaN/GaN HEMT devices along with an explanation for the type of carriers in the channel and a difference in the channel formation for Ga-face and N-face GaN crystals [Ambacher *et al.* 1999a]. According to Ambacher et al., for different AlGaN/GaN layer conditions with Ga-face and N-face growth directions, the polarization vectors are aligned as shown in Fig. 2.1.

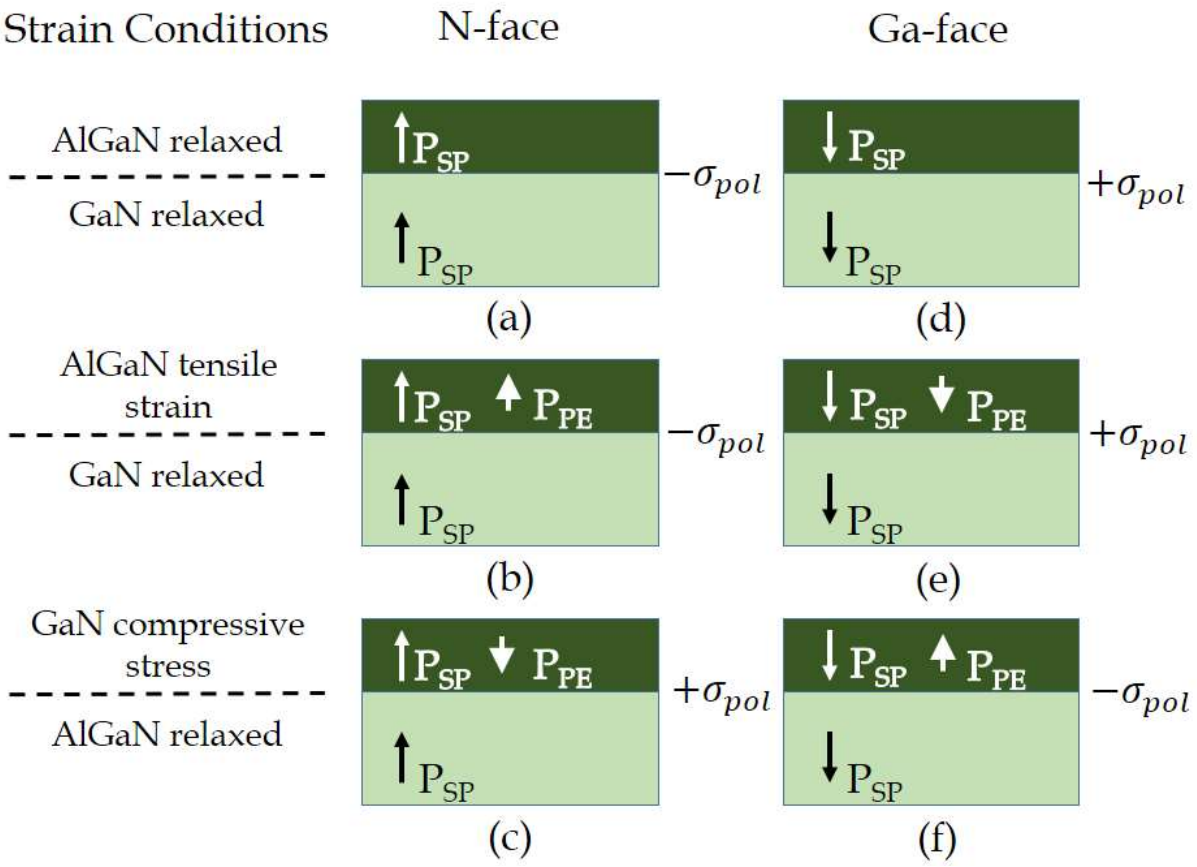



**Figure 2.1:** Orientation of polarization field within the AlGaN and GaN layers grown with N-face and Ga-face under different stress conditions. $P_{SP}$ here denotes the spontaneous polarization in the crystal, while $P_{PE}$ denotes the strain induced piezoelectric polarization field. The polarization induced charges at the interface are also shown as $\sigma_{pol}$ with the associated polarity [Ambacher *et al.* 1999a].

For the case where both AlGaN and GaN layers are relaxed, the $P_{PE}$ component of polarization vector is zero, resulting in only spontaneous polarization. $P_{SP}$ is directed towards substrate for Ga-face devices whereas it is directed towards surface for N-face devices. With a relaxed GaN layer and having AlGaN layer subjected to tensile strain, $P_{SP}$ and $P_{PE}$ are directed in the same direction and add to the total polarization charge. This results in accumulation of $+\sigma_{Pol}$ polarization charge at AlGaN/GaN interface for Ga-face devices and $-\sigma_{Pol}$ charge for N-face devices. On the other hand, for a relaxed AlGaN layer with GaN layer being subjected to compressive stress, the $P_{PE}$ component of polarization is directed in a direction opposite to that of $P_{SP}$. The resulting polarization vector results in a $-\sigma_{Pol}$ polarization charge at AlGaN/GaN interface for Ga-face devices and $+\sigma_{Pol}$ charge for N-face devices.

In order to compensate for the $+\sigma_{Pol}$ charge, an electron channel is formed in the GaN buffer with an assumption that the AlGaN/GaN band offset is high enough and the interface roughness is low. Similarly, $-\sigma_{Pol}$ charge will result in a hole channel formation. Thus, for a Ga-faced AlGaN/GaN structure an electron channel is formed, whereas for a N-faced AlGaN/GaN structure hole channel is formed. Since electron mobility is higher than the hole mobility in GaN, Ga-faced AlGaN/GaN structure is used. Channel carrier density is proportional the difference in polarization vector in the AlGaN and GaN layers. Thus, even in absence of strain in the AlGaN or GaN layer, channel formation will take place on account of spontaneous polarization. On the other hand, strain in the AlGaN layer will improve channel carrier density. The polarization field and associated charges are thus the primary source of electrons in the channel of AlGaN/GaN HEMT devices resulting in carrier density of ~$10^{13}$ $cm^{-2}$.

### 2.1.2 Surface states:

While the above discussion establishes polarization in AlGaN/GaN HEMTs to be the primary source of charge carriers in GaN channel, Ibbetson et al. in [Ibbetson *et al.* 2000] have highlighted the importance of surface states in determining the 2-DEG channel charge. According to this theory, the AlGaN/GaN system can be considered to be composed of following charge components:

- Negative charge arising due to $n_S$ electrons in the 2-DEG.
- Polarization induced charges at the AlGaN/GaN interface and AlGaN surface, denoted by $+\sigma_{Pol}$ and $-\sigma_{Pol}$, respectively.
- Charges carried by ionized donors in AlGaN barrier, $+\sigma_{AlGaN}$.
- Charges due to ionized surface states $+\sigma_{Surface}$
- Combined charges present in the GaN buffer, $\sigma_{Buffer}$.

Neglecting the Fermi level pinning at the device surface, and considering the charge neutrality condition, we get the following expression:

$$-qn_S + \sigma_{Pol} - \sigma_{Pol} + \sigma_{AlGaN} + \sigma_{Buffer} + \sigma_{Surfa} = 0$$

For a well-designed HEMT buffer charge should be as small as possible, i.e. $\sigma_{Buffer} \approx 0$. The above equation thus reduces to [Ibbetson *et al.* 2000] :

$$-qn_S + \sigma_{AlGaN} + \sigma_{Surface} = 0$$

From above equation it can be concluded that the channel charge is due to the sum of any ionized donors present in the AlGaN barrier and ionized surface donors. With un-doped barrier layer, the channel charge thus comes completely from the ionized surface traps. In order for an electron gas to exist, surface traps have to be donor in nature [Ibbetson *et al.* 2000]. If the donor traps are considered to be at an energy level of $E_D$, then they can ionize by donating electrons if their energy lies above the Fermi level ($E_D - E_F > 0$), as depicted in Fig. 2.2(a). This also explains the channel depletion observed for thin barrier layers [Saito *et al.* 2006]. For barrier thickness below critical value, Fermi level at the surface is above the donor energy level. This restricts donor traps from donating their electrons and hence $n_S \approx 0$, leading to a depleted channel. This is a commonly employed technique to achieve normally OFF operation in AlGaN/GaN HEMTs, where the AlGaN layer is recessed under the gate region to deplete the channel [Saito *et al.* 2006] [Kanamura *et al.* 2010]. However, as the barrier layer thickness is increased beyond a critical value, such that the donor trap energy level lies above the Fermi energy at surface, these donor traps now ionize to donate their electron to the 2-DEG channel, as depicted in Fig. 2.2(a)-(c). With the help of this hypothesis, Ibbetson et al. derived an expression for the critical AlGaN barrier thickness required to induce a 2-DEG channel [Ibbetson *et al.* 2000]:

$$t_{CR} = (E_D - \Delta E_C)\epsilon / q\sigma_{Pol}$$

Where $E_D$ is the donor trap energy level, $\Delta E_C$ is the conduction band offset, $\epsilon$ is the relative dielectric constant for (Al)GaN.

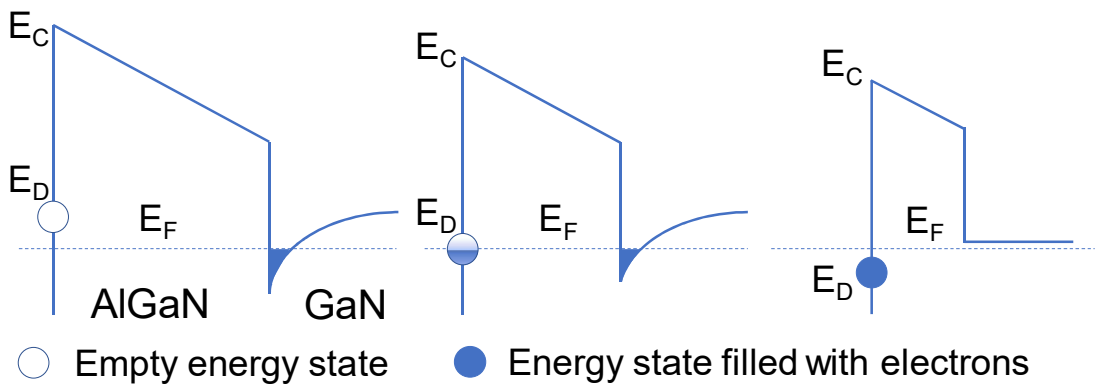



**Figure 2.2:** Energy band diagrams depicting ionization of surface donor states for different barrier thickness, (a) All the surface states at energy level $E_T$ are ionized for thick barriers, (b) Partial ionization of surface states can be seen as the barrier thickness approaches critical thickness, (c) For buffer thickness below critical value the position of Fermi level restricts ionization of surface states resulting in a depletion of the 2-DEG channel.

Considering the case for an ideal surface without any surface traps, Ibbetson et al. concluded that the 2-DEG can exist as long as the AlGaN barrier is thick enough to allow valence band to reach the Fermi level at the surface [Ibbetson *et al.* 2000]. In this case, the electrons can transfer from the valence band to the 2-DEG channel leaving behind a surface hole gas.

### 2.1.3 Relevance in computational modeling:

2-DEG denotes the primary current carrying channel in AlGaN/GaN HEMT devices, which according to above discussion shows dependence on polarization field in the epitaxial layers and on surface properties. In order to estimate the device performance, it is of critical importance to accurately predict and reproduce the source of 2-DEG. Any computational framework should in principle incorporate polarization charges as well as surface donor traps to account for the 2-DEG charge. In addition to this, a proper method needs to be identified for determining properties of these surface traps, i.e., trap concentration and activation energy.

## 2.2 GAN HEMT DESIGN – SUBSTRATE AND DIFFERENT EPITAXIAL LAYERS

### 2.2.1 Substrate

Unavailability of large sized free standing GaN substrates requires growth of GaN buffer on foreign substrates. For any material to work as substrate for growth of GaN buffer following conditions should be satisfied:

- It should have a minimal lattice mismatch with the GaN buffer, resulting in a minimized density of defects in the GaN buffer. In addition to this, it should have a thermal expansion coefficient closest possible to that of GaN. A larger difference in thermal expansion coefficient of GaN and substrate can result in cracks in the GaN layer.
- As the GaN HEMT devices are expected to operate at higher power levels, heat removal is of paramount importance in these devices. Hence, the substrate should have a higher thermal conductivity to support heat dissipation.
- Choice of substrate is also influenced by the cost factor, leading to an increased focus on device fabrication on Silicon substrate.

Based on above parameters, GaN is most commonly grown on three materials, Sapphire, SiC and Silicon. Table 2.1 compares these substrate materials with reference to the parameters discussed above. According to these parameters, SiC is the material of choice with reference to its better lattice match with GaN and having an excellent thermal conductivity. However, cost of production is prohibitively high for GaN growth on SiC wafers, restricting development of these devices on SiC substrate. Sapphire has an acceptable lattice/thermal mismatch with GaN and is a cost-effective solution in comparison to SiC, however, its poor thermal conductivity limits device performance and will lead to increased thermal management cost. Silicon being a widespread semiconductor is the most cost-effective solution for growth of GaN based devices. However, a higher lattice mismatch and difference in thermal expansion coefficient of GaN with Si makes the GaN buffer growth challenging. In addition to this, it also introduces defects in the GaN buffer which are responsible for several reliability concerns, like, DC-RF dispersion, gate/drain lag, and ambient light exposure dependent characteristics.

**Table 2.1:** Properties of substrate materials with respect to GaN [Kaminski *et al.* 2014].

| *Substrate properties* | *SiC* | *Sapphire* | *Silicon* |
|---|---|---|---|
| ***Lattice mismatch*** | *+3.5 %* | *-16 %* | *-17 %* |
| ***Thermal mismatch*** | *+33 %* | *-25 %* | *+116 %* |
| ***Thermal resistance*** | *0.3x* | *3x* | *0.9x* |

### 2.2.2 Back barrier

Back barriers are epitaxial layers inserted between the GaN channel and GaN buffer/substrate and serve a primary objective of modifying the energy band conditions to improve channel confinement in GaN channel layer. Having an improved channel confinement serves the purpose of mitigating short channel effects as gate length is reduced to support higher frequency operation [Palacios *et al.* 2006]. In addition to this, back barrier layer is also employed to mitigate the lattice mismatch issue between GaN buffer and substrate so as to minimize dislocation density. The material choice for back barrier thus depends on the energy band conditions and lattice constant of the material with respect to GaN. Some of the most commonly used back barrier layers are as follows:

***InGaN back barrier:*** Channel confinement in AlGaN/GaN HEMTs can be improved by raising the conduction band in buffer region with respect to the channel region. This can be achieved by use of high band gap materials or by using p-type buffer layers. However, these techniques have a negative impact on device performance due to traps introduced by them [Palacios *et al.* 2006]. Palacios *et al.* suggested a different approach to improve channel confinement by use of a low band-gap material in the channel [Palacios *et al.* 2006]. Using an ultra-thin (< 2 nm) $In_{0.1}Ga_{0.9}N$ layer combined with lower In composition (~0.1), Palacios *et al.* have reported growth of a high quality InGaN layer with minimized trap concentration [Palacios *et al.* 2006]. The epi-layer arrangement with InGaN back barrier layer, as described in [Palacios *et al.* 2006], is reproduced in Fig. 2.3(a) and its impact on polarization charge as well as energy band diagram is depicted in Fig. 2.3(b).

With use of this structure, Palacios *et al.* reported a significant improvement in pinch-off characteristics and ~50% increase in the output resistance [Palacios *et al.* 2006]. However, use of a lower band gap material has a negative impact on breakdown voltage of the device, leading to a limited output power. In addition to this, Lee *et al.* have also reported use of a thin (~3.3 nm) InGaN back barrier layer to improve channel confinement allowing them to scale gate length from 250 nm down to 70 nm with a limited threshold voltage roll-off of about 0.3 V [Lee *et al.* 2011b]. According to Lee *et al.*, AlGaN back barriers reduce the thermal conductivity of the structure besides inducing polarization field in the GaN channel. On the other hand, with InGaN back barrier, polarization induced electric field resides in the InGaN layer and provides an effective conduction band offset.

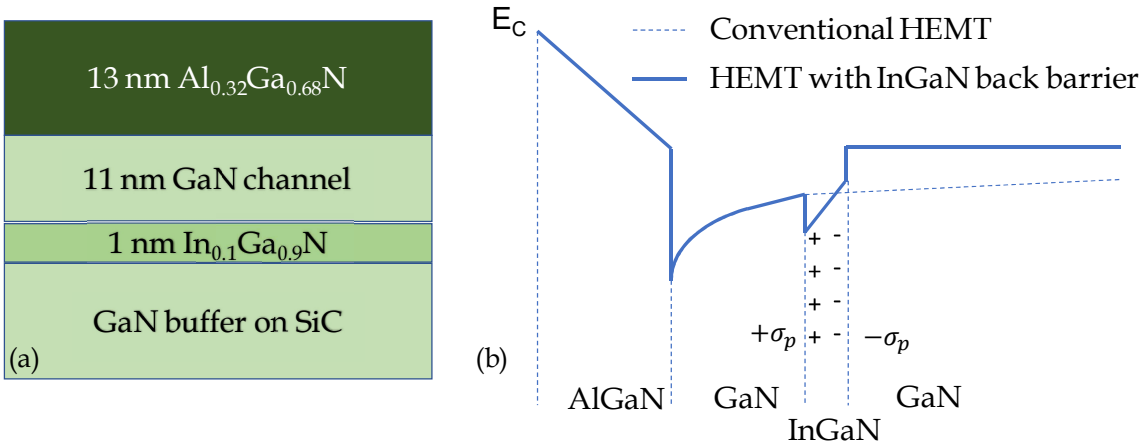



**Figure 2.3:** (a) Epitaxial layer arrangement depicting use of an $In_{0.1}Ga_{0.9}N$ back barrier layer combined with a thin GaN channel layer to improve channel confinement [Palacios *et al.* 2006]. (b) InGaN induced polarization charges and its impact on conduction band energy within the GaN buffer region.

***AlGaN back barrier:*** In addition to InGaN back barrier, AlGaN back barriers are widely employed to result in an energy band offset leading to improved channel confinement. In addition to providing conduction band offset, graded AlGaN back barrier layers are known to mitigate dislocations/defects in GaN buffer layer. In [Bahat-Treidel *et al.* 2008], Bahat Triedel *et al.* have demonstrated devices with double hetero-junction with second hetero-junction defined by AlGaN back barrier having low Al composition near the interface with GaN channel (< 0.1). However, presence of strong polarization fields in AlGaN back barrier layers can result in formation of parasitic channels. In order to counter this effect, the AlGaN back barrier layers are linearly graded over a thicker region to minimize polarization doping, thereby preventing formation of a parasitic channel [Bahat-Treidel *et al.* 2008]. The devices with AlGaN back barrier resulted in a reduced threshold voltage ($V_{th}$) shift with increase in drain bias voltage ($V_{DS}$) as compared to devices where AlGaN back barrier was not present [Bahat-Treidel *et al.* 2008]. In addition to this, use of AlGaN back barrier also improves sub-threshold leakage, punch through voltage and scaling of punch through voltage with gate to drain distance ($L_{GD}$) [Bahat-Treidel *et al.* 2008].

The above discussion concludes that short channel effects and punch through voltage in AlGaN/GaN HEMTs can be effectively improved by inserting a back barrier beneath the GaN channel. The back barrier thus employed essentially introduces an energy barrier in the GaN channel thereby improving the channel confinement.

***Relevance in computational modeling:*** In order to reproduce the impact of back barriers on device characteristics, it is important for any computational framework to take into account and accurately model the impact of these epitaxial layers on the conduction band energy along with their impact on polarization field/doping in the buffer region.

### 2.2.3 The GaN channel

GaN channel holds the 2-DEG in AlGaN/GaN HEMTs and is very critical to control the channel transport properties and buffer leakage. Unlike the doped buffer/substrate in Si-MOS devices, the buffer in AlGaN/GaN HEMTs is required to be resistive/semi-insulating. However, the growth conditions for GaN are susceptible to unintentional doping (UID) of GaN leading to negative impact on mobility and channel confinement. This n-type UID is attributed to introduction of oxygen impurity during the growth process [Chung *et al.* 1992]. While oxygen impurity is omnipresent in the system, growth conditions can be optimized to reduce the oxygen concentration. Resistive films are obtained by reducing reaction temperature and/or reducing

chamber pressure [Keller *et al.* 2001]. This is attributed to compensation of electrons by deep acceptors and incorporation of carbon in GaN buffer. Keller *et al.* proposed a 2-step technique for growth of GaN buffer. The GaN buffer region near the substrate/GaN interface can be grown at low pressure to compensate for higher concentration of oxygen donors by higher concentration of deep acceptors. On the other hand, the GaN channel layer can be deposited at atmospheric pressure to result in low density of point defects thereby improving the channel transport properties [Keller *et al.* 2001]. Thus, the growth conditions are optimized to result in a reduced UID especially in the buffer region while maintaining high film quality in the channel region.

In addition to the growth conditions, intentional doping in the GaN buffer is often employed to control its resistivity. Iron (Fe)/Carbon (C) are most commonly used dopants in the GaN buffer, known to improve resistivity of GaN buffer resulting in a reduced leakage and improved breakdown voltage [Bahat-Treidel *et al.* 2010]. However, doping of GaN buffer by C/Fe is also known to result in performance degradation due to increased ON-resistance and a higher DC-RF dispersion [Uren *et al.* 2012, Verzellesi *et al.* 2014a, Uren *et al.* 2015]. These parameters suggest GaN buffer designing to be an important design aspect to be considered for development of AlGaN/GaN HEMT devices with high breakdown voltage and optimized performance.

### 2.2.4 Spacer layer

As the channel in AlGaN/GaN HEMT devices is present even in absence of doping in AlGaN barrier layer, the only design parameters available to improve channel carrier concentration is by increasing Al mole fraction in the barrier layer, thereby increasing the conduction band energy offset between AlGaN and GaN. However, increasing the Al mole fraction leads to a reduced mobility in the channel because of alloy disorder scattering and as reported in [Keller *et al.* 2001] the crystal quality may degrade as well. In order to counter this effect while improving the power density of AlGaN/GaN HEMTs, Shen *et al.* demonstrated that insertion of a thin (~1 nm thick) AlN film between GaN channel and AlGaN barrier can simultaneously improve sheet charge density ($n_S$) and channel electron mobility ($\mu$) thereby improving the $n_S.\mu$ product [Shen *et al.* 2001a].

The energy band discontinuity introduced by AlN spacer, due to polarization induced dipole in the AlN layer, is responsible for increase in $n_S$ [Shen *et al.* 2001a]. In addition to this, Shen et al. also observed an increase in mobility from ~1200 $cm^2/V.s$ to 1540 $cm^2/V.s$ by insertion of an AlN spacer while all the other device parameters were kept same. Improvement of mobility with AlN spacer was attributed to reduced penetration of electron into the AlGaN buffer due to energy difference introduced by AlN spacer and due to reduced alloy disorder scattering [Shen *et al.* 2001a].

### 2.2.5 Barrier layer

The barrier layer in AlGaN/GaN HEMTs is responsible for creating the energy band conditions necessary for formation of 2-DEG channel. The barrier layer design thus significantly affects $n_S$. On the other hand, barrier layer properties also define the interface between AlGaN barrier and GaN channel. As channel is formed near this interface, it significantly affects the channel electron mobility. As improving the channel electron density and mobility is a primary requirement to increase current density of the device, proper designing of barrier layer is important. While AlGaN layer with varying composition and thickness is most commonly used design tool to achieve optimum channel carrier density and mobility, several other options have also been explored in the past to replace AlGaN as a barrier layer.

***Aluminum Nitride (AlN)***: Increasing the Al composition in barrier layer results in an increase in the polarization induced 2-DEG density. The maximum possible $n_S$ that can be achieved for binary system with AlN as barrier on a GaN channel is limited to ~$6 \times 10^{13}$ $cm^{-2}$ [Cao *et al.* 2007]. In an earlier work by Cao *et al.* [Cao *et al.* 2007], it was concluded that it was possible

to achieve these high carrier densities by growth of ultra-thin AlN layer (~ 2-6 nm thick) using Molecular Beam Epitaxy (MBE). However, the increase in channel electron density was accompanied by a reduction in electron mobility. Cao *et al.* observed a design window in which high electron mobility (~1000-1600 $cm^2/V.s$) could be observed simultaneously with high 2-DEG density (~2-4 x $10^{13}$ $cm^{-2}$) and concluded with a 3.5 nm AlN to be the best candidate for achieving high $n_S$ simultaneously with high mobility.

***Aluminum Indium Nitride (AlInN)***: According to Kuzmik et al. [Kuzmík 2001], use of AlGaN as a barrier results in two fundamental limitations: (1) Total stress induced by AlGaN layer due to lattice mismatch and piezoelectric effects results in reduced device reliability, (2) Reduction in barrier thickness is required with reduction in gate length to suppress short channel effects, however, thin AlGaN barrier layers results in surface depletion effects, resulting in reduced $n_S$.

In order to counter these effects, Kuzmik et al. in [Kuzmík 2001] proposed use of AlInN as an alternative to AlGaN barrier layer. AlInN layers show reduced surface depletion effects, enabling thickness reduction to much lower values as gate length is decreased. In addition to this, $Al_{0.83}In_{0.17}N$ can be grown lattice matched to GaN layer, reducing the strain in AlGaN layer and hence improving the device reliability. In [Medjdoub *et al.* 2006], Medjoub *et al.* were able to achieve a 2-DEG density of 2.5 x $10^{13}$ $cm^{-2}$ with a mobility of ~1170 $cm^2/V.s$ with use of an AlInN barrier layer. In addition to this, no reduction in $n_S$ was observed for AlInN as thin as 10 nm, enabling barrier layer scaling to improve gate control and counter short channel effects. However, with a similar barrier layer, having reduced thickness of ~5.5 nm, Lee *et al.* observed influence of short channel effects for gate lengths below 50 nm [Lee *et al.* 2011a]. In addition to this, these structures showed a reduced channel electron mobility (~480 $cm^2/V.s$), which has been attributed to alloy disorder scattering and interface roughness [Kuzmík *et al.* 2006].

The fabrication difficulties combined with negative impact of these barrier layers on channel electron mobility has forced device engineers to rely on AlGaN as the material of choice for barrier layer. However, with improvement in growth conditions of these barrier layers, a shift from AlGaN towards AlN or AlInN can be anticipated.

### 2.2.6 Cap layer

Terminating the AlGaN surface with different cap layers has been widely studied and considered for performance improvement in AlGaN/GaN HEMT devices. Use of a cap layer serves following purpose:

1. It is expected to reduce the impact of surface states [Shen *et al.* 2004]
2. It can be used for polarization engineering to enhance device performance [Kanamura *et al.* 2010].

According to Shen *et al.* [Shen *et al.* 2004], use of a thicker cap layer has the ability to reduce the impact of surface states on device performance. As the surface states affect the surface potential, their impact on 2-DEG can be reduced by increasing distance between the surface and the channel in the gate-drain and the gate-source access regions. Shen *et al.* employed the same principal by having a thick GaN cap layer (~250 nm) in the access regions, while under the gate region the GaN cap was removed [Shen *et al.* 2004]. With this structure, Shen *et al.* were able to demonstrate devices with suppressed DC-RF dispersion effects [Shen *et al.* 2004]. However, use of a GaN cap increased gate leakage and reduced breakdown voltage of the device. Arulkumaran et al. presented a systematic study on use of different GaN cap layers in AlGaN/GaN HEMT devices and demonstrated that use of even 3 nm thin i-GaN cap layer can effectively result in suppression of the current collapse phenomena in these devices, indicating reduced impact of surface traps on device characteristics [Subramaniam *et al.* 2005]. This impact of GaN cap layer on device characteristics is commonly attributed to improved surface morphology leading to

reduced surface defects [Subramaniam *et al.* 2005, Charles *et al.* 2018]. Kanamura *et al.* reported in [Kanamura *et al.* 2010] that by use of a triple cap layer structure consisting of a 2 nm thick AlN cap layer sandwiched between 2 nm thick n-GaN cap layers a smooth surface morphology can be obtained along with an improved 2-DEG density. While the top n-GaN cap layer provided a smooth surface morphology, the piezoelectric effect between AlN and n-GaN layer resulted in an increase in 2-DEG density.

***Surface passivation by dielectric:*** In addition to terminating the surface by a thin/thick cap layer, surface passivation by a suitable dielectric is often practiced in AlGaN/GaN HEMT devices to improve its RF characteristics. According to Hashizume *et al.* in [Hashizume *et al.* 2017], surface passivation in AlGaN/GaN HEMTs improves long-term stability and controls current collapse in AlGaN/GaN HEMTs, thereby improving the microwave performance. Using PECVD deposited $SiN_x$ in the access region, Green et al. were the first to report any noteworthy reduction in current collapse in AlGaN/GaN HEMT devices [Green *et al.* 2000]. According to [Hashizume *et al.* 2002, Hashizume *et al.* 2004], this can be attributed to generation of nitrogen radicals during the PECVD process which reduces formation of defects related to Nitrogen vacancies at $SiN_X$/AlGaN interface. Moreover, surface passivation enables use of field plates, which helps in relaxing electric field at the gate edge and also reduces current collapse phenomena as was discussed previously. In addition to SiN passivation, several other dielectrics have been reported to passivate the AlGaN/GaN HEMT device surface, like, AlN [Tsurumi *et al.* 2010], $Al_2O_3$ [Jo *et al.* 2015], $SiO_2$ [Arulkumaran *et al.* 1998], SiON [Arulkumaran *et al.* 2004].

## 2.3 DEVICE DESIGN FOR HIGH BREAKDOWN VOLTAGES

While the epitaxial layer arrangement, as discussed above, is important design aspect to improve device performance, the voltage handling capacity of the device can be improved by considering the lateral and vertical design parameters affecting electric field distribution in the device. In order to achieve high breakdown voltages in AlGaN/GaN HEMT devices, lateral device dimensions, especially gate to drain distance ($L_{GD}$), have been traditionally considered as the primary design parameters. However, the improvement in breakdown voltage saturates after reaching a threshold $L_{GD}$ value. This is expected to be caused by field crowding near the gate edge and/or vertical GaN buffer breakdown. These limitations have led to two primary design axes for HEMT design with respect to voltage handling capacity of the device. One of the design axis deals with lateral electric field relaxation while the second axis deals with vertical field relaxation. With respect to lateral electric field relaxation use of field plates is a widely accepted technique. On the other hand, for vertical field relaxation, compensation doping in GaN buffer is commonly adopted. These techniques are discussed in detail as follows:

### 2.3.1 Lateral field relaxation: Employing field plates

In AlGaN/GaN HEMT devices, avalanche breakdown is considered to be caused by electric field crowding near the drain side gate edge. The electric field in these conditions leads to a field peak near the drain side edge of gate, limiting the breakdown voltage of the device. An efficient method to relax this electric field peak is by use of a field plate above the gate electrode that is electrically connected to either gate [Zhang *et al.* 2000, Karmalkar *et al.* 2001, Wu *et al.* 2004, Dora *et al.* 2006] or source [Saito *et al.* 2003] electrode or a combination of both [Saito *et al.* 2007]. Field plates enable extension of depletion region and hence result in a relaxation of electric field peak near the gate edge. Design of field plated GaN HEMTs is extensively discussed in work by Karmalkar *et al.* in [Karmalkar *et al.* 2001]. According to Karmalkar *et al.*, in absence of a field plate the electric field is confined is a narrow region near gate edge, where the field peak is observed. Use of a field plate redistributes the electric field between two peaks, one near the gate edge and another near the field plate edge. The similar concept was extended to use of multiple (n) field plates to redistribute electric field between (n+1) peaks resulting in an increased breakdown voltage [Xing *et al.* 2004]. In addition to improving breakdown voltage, field plates are also known for reducing impact of surface traps on RF performance of the device. Earlier works have

established that having field plates can reduce DC-RF dispersion and dynamic ON-resistance [Koudymov *et al.* 2005, Saito *et al.* 2007, Saito *et al.* 2018]. Further, Koudymov *et al.* suggested in [Koudymov *et al.* 2005] that current collapse removal in AlGaN/GaN HEMT is caused by interaction between field plates and surface states thereby resulting in faster trapping/de-trapping of surface states. This results in suppression of impact of surface traps on RF performance of the device. However, the number of field plates along with the field plate dimensions is constrained by its negative impact on parasitic capacitances and hence on RF performance of the device. Use of field plates increases the parasitic capacitances and hence hampers the operating frequency of the device [Wu *et al.* 2004]. Use of a field plate in the device introduces a new variable in the lateral design space, i.e., field plate length ($L_{FP}$). An increase in $L_{FP}$ is expected to improve breakdown voltage of the device as the electric field redistributes between the two peaks [Saito *et al.* 2003]. However, $L_{FP}$ is limited by an increase in peak electric field value near the field plate edge.

### 2.3.2 Vertical field relaxation: Buffer designing

By increasing $L_{GD}$ and $L_{FP}$, lateral field relaxation can be achieved in HEMT devices. However, the improvement in breakdown voltage is limited by vertical breakdown of the GaN buffer [Borga *et al.* 2018] whose conductivity is defined by the unintentional doping introduced during GaN growth. This unintentional doping needs to be compensated to increase the GaN buffer resistivity, thereby reducing leakage and improving breakdown voltage. While Iron (Fe) & C both behave as compensating agent for this UID, however, due to absence of memory effect and possibility to achieve steep doping profiles, C is the dopant of choice for achieving highly resistive GaN buffers. Possibility of improving breakdown performance of the device with C-Doping of GaN buffer has been suggested in several earlier works [Bahat-Treidel *et al.* 2010, Hilt *et al.* 2011, Verzellesi *et al.* 2014a].

However, doping with carbon increases DC-RF dispersion observed in AlGaN/GaN HEMT devices along with an increase in DC resistance [Bahat-Treidel *et al.* 2010, Uren *et al.* 2012, Verzellesi *et al.* 2014a, Chini *et al.* 2016]. This is attributed to acceptor type traps introduced by carbon dopants in GaN. Behavior of C as acceptor traps in GaN buffer is also supported by the experimental observation of yellow luminance [Lyons *et al.* 2010, Lyons *et al.* 2014].

## 2.4 GAN RELIABILITY

Due to extreme operating conditions combined with lattice mismatch induced strain, AlGaN/GaN HEMT devices are continuously subjected to electrical and physical stress leading to several reliability concerns. This section discusses major contributing factors to the reliability challenges in AlGaN/GaN HEMT devices.

### 2.4.1 Traps

Traps are intermediate energy states, introduced by impurities, defects or dangling bonds, where electrons/holes can jump if provided with sufficient energy. These traps can capture either electrons or holes based on their electronic properties. Owing to the growth conditions for AlGaN/GaN HEMT devices on foreign substrates like silicon, sapphire or SiC, several dislocations/defects are introduced in the GaN buffer. These defects/dislocations manifest themselves as trap sites [Subramani *et al.* 2018]. In addition to this, impurity atoms such as Si, O, C etc. are also known to introduce trap sites in GaN. In addition to this, surface traps are well known in these devices and are also considered as a major source of channel electrons as discussed in section 2.1.2. As traps can significantly impact the charge distribution within the device and show time/light dependent behavior, they are a major source of several reliability concerns in AlGaN/GaN HEMT devices.

***DC-RF dispersion:*** It is a commonly observed phenomena and a major performance bottleneck in AlGaN/GaN HEMT devices. It is defined as the deviation in RF performance of the device as compared to that predicted by DC performance, wherein the device shows lower RF performance figures. Several earlier works relate this dispersion or current collapse phenomena to traps on the device surface [Vetury *et al.* 2001, Meneghesso *et al.* 2004a]. According to Meneghesso *et al.*, the major arguments supporting role of surface traps in current collapse phenomena are:

(a) Suppression of dispersion effect by SiN surface passivation, and

(b) Reduction in dispersion by adding $p^+/n^+$ layers on access regions between gate-source and gate-drain [Meneghesso *et al.* 2004a].

In addition to this, suppression of current collapse with use of field plates and its dependence on conductivity of dielectric [Koudymov *et al.* 2005] further supports the argument that surface traps are responsible for dispersion.

Mechanism behind impact of surface states on current collapse phenomena can be explained by considering the virtual gate concept as explained in [Vetury *et al.* 2001]. Charges trapped in the access regions act as virtual gates and modulate the underlying depletion region. These trapped charges can be modulated either by electrons injected by gate or hot electrons in the channel region overcoming the barrier and getting trapped on the surface. Now with an abrupt change in gate/drain voltage, these trapped charges respond with their respective time constants for capture/emission phenomena. This results in a current collapse which recovers with time [Binari *et al.* 2001, Meneghesso *et al.* 2004a, Tirado *et al.* 2007].

Apart from surface traps, traps in the GaN buffer also affect DC-RF dispersion/current collapse. In order for a 2-DEG channel to be confined near the AlGaN/GaN interface, the traps in GaN buffer can be acceptor in nature. Donor traps in GaN buffer would result in a leaky buffer and further the positive charge carried by ionized donor traps would pull down the energy bands resulting in a weaker confinement of electrons in the 2-DEG. Acceptor traps in GaN buffer can capture channel hot electrons and deplete the channel due to negative charge carried by ionized acceptors. In addition to this, C-Doping of GaN buffer, which is a well-known technique for improving breakdown voltage in AlGaN/GaN HEMT devices, also causes an increase in DC-RF dispersion. This behavior of C-Doping in GaN is also attributed to carbon introducing traps sites in the GaN buffer [Lyons *et al.* 2010, Uren *et al.* 2012, Lyons *et al.* 2014, Verzellesi *et al.* 2014a].

Further, with the help of a simulation based study supported with experimental observations, Faqir et al. were able to show that presence of traps in the cap, barrier and buffer layers were able to explain all the degradation modes observed in AlGaN/GaN HEMT devices [Faqir *et al.* 2008]. The degradation modes included gate-lag amplification, drop in reverse gate leakage current and dc drain current ($I_D$) collapse. Drop in reverse gate leakage was caused by traps in all the three layers, while dc $I_D$ collapse was caused by buffer traps. Gate lag was controlled by cap and barrier traps.

***Gate leakage current:*** Since the AlGaN/GaN HEMT structures are widely used with Schottky gated structure, surface traps can significantly affect gate leakage in these devices. As these traps are donor in nature and carry a positive charge in ionized states, their presence can significantly reduce the energy barrier and hence increase the gate leakage [Saito *et al.* 2005]. This high leakage current can also significantly bring down the avalanche breakdown voltage due to increased carrier injection.

In addition to above mentioned effects, traps are also responsible for following phenomena observed in AlGaN/GaN HEMT devices [Binari *et al.* 2001, Tirado *et al.* 2007, Li *et al.* 2018, Sayadi *et al.* 2018]:

- Trans-conductance frequency dispersion
- Current collapse in drain characteristics
- Gate and drain lag transients
- Light sensitivity
- Restricted microwave output
- Threshold voltage shift
- Dynamic ON-resistance

### 2.4.2 Impact of physical and electrical stress:

AlGaN/GaN HEMT devices are expected to be subjected to electrical stress due to higher operating voltages. On the other hand, presence of converse polarization and strain in AlGaN layer imposes physical stress on the device as well. A correlation between the electrical and physical stress was discussed by Joh *et al.* in [Joh *et al.* 2008]. Through step stress experiments, Joh et al. demonstrated presence of a critical bias voltage beyond which the AlGaN/GaN HEMT devices showed electrical degradation. The observations suggested that the degradation was higher in the OFF state as compared to semi-ON state or power state. The degradation mechanism in this case was linked to the crystallographic defect formation in AlGaN/GaN HEMT devices and is discussed as follows. According to hypothesis suggested by Joh et al. in [Joh *et al.* 2008], the electric field exerts a mechanical strain in the AlGaN barrier layer. Since electric field is higher at the drain side edge of gate, a higher mechanical strain is applied on this end, which is further dependent on applied gate bias voltage. This view was also supported by evidence of crack and pit formation on drain side edge of gate on application of high drain bias voltages for stress time in range of 6h to 1000h [Chowdhury *et al.* 2008]. This strain adds to the strain caused due to lattice mismatch between AlGaN and GaN layers, resulting in a higher elastic energy. As this elastic energy exceeds critical value, crystallographic defects are formed. These crystallographic defect sites can manifest themselves as trapping centers and result in electrical degradation of device. Further, the elastic energy resulting from combination of electrical stress induced strain and strain due to lattice mismatch will be proportional to vertical electric field. Hence, a dependence of critical voltage required for electrical degradation on gate bias voltage was observed [Joh *et al.* 2008]. In addition to this, for $V_{DS}$ = 0 V state, a dependence of critical voltage on gate length was observed. In this case, critical voltage decreased with gate length. This was attributed to an effective increase in overall mechanical strain under gate edge as the source end and drain end are brought closer to each other [Joh *et al.* 2008]. In $V_{DS}$ = 0 V case, electrical field or strain at the source end of gate is comparable or greater than that at the drain side edge of the gate.

Above hypothesis suggests OFF state stress to be detrimental to device performance in AlGaN/GaN HEMTs. On the other hand, a reliability study by Meneghesso et al. in [Meneghesso *et al.* 2008], suggests hot electron effects combined with traps on device surface or in the deep GaN buffer to be detrimental to the device performance. According to hot electron theory, semi-ON state is the most favorable for generation of hot electrons and hence should be the most detrimental stress condition for AlGaN/GaN HEMT device. Meneghesso et al. presented a detailed reliability study in presence of hot electrons with the help of Electro-luminescence analysis of devices with and without SiN passivation and subjected to different electrical stress conditions, viz., OFF-state, ON-state and semi-ON state [Meneghesso *et al.* 2008]. Based on these studies, Meneghesso et al. concluded that hot electrons and their subsequent trapping/de-trapping in the traps is a major phenomenon affecting reliability of GaN HEMT devices. Further, the hot electron effect is maximum in the semi-ON condition when electric field is high, and channel has sufficient electrons to gain energy and behave as hot electrons. In addition to this, based on the surface study, it was further suggested that degradation involves the AlGaN surface and surface passivation had a positive impact on device reliability with respect to hot-electron degradation. These observations suggest surface traps and hot electrons to be responsible for reliability concerns such as $g_m$ degradation, gate lag, current collapse and threshold voltage shift. However, these observations contradict the observations of Joh et al. which state OFF-state stress

to be most critical for reliability of AlGaN/GaN HEMTs [Joh *et al.* 2008]. On the other hand, both the studies suggest generation of traps and subsequent trapping of electrons to be responsible for performance degradation.

### 2.4.3 Punch through effect in GaN buffer

Punch through or drain induced barrier lowering is a common effect observed in FETs for shorter channel lengths. Punch through effect is primarily caused by a weaker control of gate over the channel. This requires scaling of barrier layer with reduction in gate length to increase gate control over the channel. However, in addition to barrier layer design, properties of GaN buffer can also significantly affect the short channel effects. In a simulation based study in [Uren *et al.* 2006], Uren et al. suggested that properties of GaN buffer can also significantly affect the punch through effect observed in AlGaN/GaN devices. According to Uren et al., effective doping in buffer controls the punch through voltage and increase in output conductance. Here effective doping is defined as the difference of acceptor trap concentration ($N_A$) and donor trap concentration ($N_D$) in GaN buffer. Here donor trap concentration takes into account the impurity atoms introduced during growth of GaN buffer and result in n-type doping of GaN buffer [Uren *et al.* 2006]. On the other hand, acceptor traps take into account the compensation of this n-type doping for maintaining a semi-insulating GaN buffer. With this study Uren et al. concluded that for GaN buffer to be able to support shorter channel lengths, a sufficiently higher deep acceptor trap concentration is required in GaN buffer to confine carriers in the channel.

## 2.5 COMPUTATIONAL ANALYSIS AND OPTIMIZATION OF ALGAN/GAN HEMT DEVICES: CHALLENGES AND OPPORTUNITIES

Although AlGaN/GaN HEMT devices have established themselves in the power and RF domain, still certain performance bottlenecks need to be addressed in order to tap the full potential of these devices. With the device structure and design optimizations discussed above, it can be fairly concluded that a significant improvement in device performance can be obtained through structural modifications in AlGaN/GaN HEMT devices. These structural optimizations can be carried out at several levels including optimization of epitaxial stack, lateral design parameters, surface treatment and buffer designing. In order to explore this vast domain of device optimization with several design axes, computational models are an effective tool to predict device performance accelerating the technology development at low cost. However, computations of AlGaN/GaN HEMT devices is not a trivial problem and should take care of several important parameters as has been discussed above and are further listed as following:

- Introduction of epitaxial layers to the device stack modifies two important device properties, (i) Conduction band energy, which in turn affects the channel confinement and can significantly alter trap occupation dynamics, and (ii) Can result in polarization doping in the structure leading to formation of parasitic channels. Computational model should take care of these two factors in order to evaluate impact of any epitaxial layer on the device performance.

- 2-DEG channel: As discussed above, 2-DEG channel results from polarization in AlGaN/GaN devices which acts in combination with surface donor traps. Any computational framework should thus account for polarization charges in the device as well as should consider device performance in presence of surface donor traps.

- Buffer growth related parameters: GaN buffer in AlGaN/GaN HEMT devices is one of the most important design parameters as it controls the leakage and breakdown performance of the device and is also responsible for containing the 2-DEG channel. However, the GaN buffer is source of certain performance bottlenecks arising primarily due to presence of traps in GaN buffer. In addition to this, doping of C/Fe, done to compensate for UID in GaN buffer, also introduces traps in the GaN buffer. It is thus

important to consider impact of these traps on DC/RF performance of the device. Moreover, determining the nature of traps introduced by C/Fe doping is a topic of interest and needs careful investigation to optimize breakdown voltage of the device while maintaining DC/RF performance.

- Lattice and carrier heating: Device operation at higher electric currents combined with poor thermal conductivity of substrate/buffer results in self heating of the device. In order to verify its operation as power semiconductor device, it is important to consider impact of device heating on device performance. In addition to this, presence of high electric field gradient in the device can result in high energy electrons or hot electrons. These hot electrons in combination with traps on device surface and GaN buffer can significantly alter device characteristics. Thus, while considering traps in the device, it is important to consider the hot electrons in the device.

- Device geometry: As it will be discussed in the next chapter, certain device geometry related parameters can significantly affect the device performance and need to be carefully modeled in order to have an accurate estimation of the device performance. For example, placement of gate finger over the MESA etch region can result in formation of a side diode which can significantly affect gate leakage characteristics, as will be discussed in detail in chapter 3.

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