Declaration

I hereby declare that the work presented in this Thesis titled *Sliding Mode Control Strategies to Improve Energy Efficiency and Power Factor of Power Converters* submitted to the Indian Institute of Technology Jodhpur in partial fulfillment of the requirements for the award of the degree of Doctor of Philosophy, is a bonafide record of the research work carried out under the supervision of Professor Deepak M. Fulwani. The contents of this thesis in full or in parts, have not been submitted to, and will not be submitted by me to, any other Institute or University in India or abroad for the award of any degree or diploma.

Nupur Rathore
P14VSS005

Certificate

This is to certify that the thesis titled *Sliding Mode Control Strategies to Improve Energy Efficiency and Power Factor of Power Converters*, submitted by *Nupur Rathore (P14VSS005)* to the Indian Institute of Technology Jodhpur for the award of the degree of *Doctor of Philosophy*, is a bonafide record of the research work done by her under our supervision. To the best of my knowledge, the contents of this report, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. Deepak M. Fulwani
Ph.D.Thesis Supervisor

Acknowledgments

This thesis would not have been possible without the support of many people. I would like to take this opportunity to extend my sincere gratitude towards all those who made this dream turn into reality. First and foremost, I would like to express my deepest gratitude to my Ph.D. Thesis Supervisor, Professor Deepak M. Fulwani. He had always been so supportive of my professional as well as personal journey during the years of my stay at IIT Jodhpur. I am grateful to him for his continuous efforts to inculcate the positive motivation in me and his continual guidance, generous support and patience, especially during the times of my slow progress. I thank him for believing in me in times when I didn't believe in myself. I feel blessed to having known a person who personifies professional morals and ethics. He gave me ample opportunities for the relevant exposure at conferences, despite limited resources. He will always be somebody I look upto in career for he has been the greatest influence in shaping up my world of academic and research, morals and ethics.

My special words of thanks also go to Professor Akshay Kumar Rathore for providing his continuous support, guidance and encouragement, going out of his way. He has been such a source of inspiration and taught me another aspect of life, that, hard work and positive attitude towards work and life can take you a long way. I owe a lot of gratitude to him for always being there for me and I feel privileged to be associated with a person like him in my life.

It has been a pleasure to share the same lab as my seniors Dr. Suresh Singh, Dr. Ram Niwas Mahia and Dr. Aditya Raw Gautam. They set the thriving environment in the lab. I want to thank them for their continuous guidance and moral boosting to make me believe this is achievable. A very warm thank to my laboratory colleagues, Shivam, Rammohan, and Poonam for keeping the environment of the lab lively, and also for their support. I also wish to thank Vinod Kumar, Kumar Gourav and Rammohan for their help and support in the development of hardware and its implementation during their engagement in the sponsored research projects under Professor Fulwani.

I fall short of words to thank my juniors Shruti and Mohit, for being there whenever duty called or not. Life would have been a little less fun without them.

I owe my deepest gratitude towards my better half Sudeep for his eternal support and understanding of my goals and aspirations. He has been my strength during my days of struggle. Without his help, I would not have been able to complete much of what I have done and become who I am.

My heart felt regard goes to my father in law, mother in law, brother in law, sister in law and little Jai for their love and moral support. They have been extremely supportive of my work and always encouraged me to give my best.
Last but not the least, I want to give much love to my parents and brother Prasanjeet. I wish to thank for the patience, support and love which they ushered on me, and for bearing with me even when I was not spending any time with them. To you I owe EVERYTHING.

Nupur Rathore
Ph.D. Student

List of Figures

Figure	*Title*	*page*
1.1	An ideal switch and it's switching waveform (voltage, current, and power)	2
1.2	Switching waveform for a practical switch (voltage, current, and power)	3
1.3	Sources of power loss in a synchronous buck converter [Qahouq *et al.*, 2007].	4
1.4	Plots for typical buck converter [Qahouq *et al.*, 2007].	5
1.5	Variation of losses in a converter with load [Erickson and Maksimovic, 1995].	6
1.6	Mode hopping with load [Erickson and Maksimovic, 1995], [Zhou *et al.*, 1997].	7
1.7	Three control modes converter and their efficiency as functions of output current. [Huang *et al.*, 2006].	8
1.8	The operation principle of the conventional burst mode [Lee *et al.*, 2013].	9
1.9	Types of sampling. (a) Fixed time period and variable threshold, (b) Variable time period and fixed threshold, (c) Variable time period and variable threshold.	14
1.10	Concept of Sliding mode control	16
1.11	Front end circuitry of a typical electronic equipment.	19
2.1	Isolated Half Bridge Converter	26
2.2	Switching waveform for a Half Bridge Converter	26
2.3	(a).Block diagram for classical implementation of SMC. (b).Block diagram for Event-triggered implementation of SMC.	32
2.4	Hysteresis modulation based SMC (HM-SMC).	32
2.5	(a).Block diagram for HM-SMC. (b).Block diagram for ET-SMC.	33
2.6	Comparison of the fixed size sliding band for HM-SMC (in blue) and load adaptive sliding band for ETSMC (in red).	33
2.7	Voltage Regulation for SMC and ETSMC and the corresponding switching signal	35
2.8	Evolution of error for SMC and ETSMC and occurrence of events	36
2.9	ETSMC and Load Variation: Event density for load change	36
2.10	ETSMC and Load Variation: Load variation with corresponding variation in switching signal	36
2.11	Experimental setup	37
2.12	Experimental demonstration of Classical SMC and ETSMC: output voltage and switching actions.	38
2.13	Experimental results for the proposed theory: output voltage and switching actions under variable input.	38
2.14	Experimental results for the proposed theory: output voltage and switching actions under variable load conditions.	39
2.15	Experimental results for the proposed theory: Switch voltage and switching actions under variable load at Load 300W.	39
2.16	Experimental results for the proposed theory: Switch voltage and switching actions under variable load at Load 100W.	40
2.17	Experimental results for the proposed theory: Saving in losses with respect to load conditions.	40
3.1	(a) Uncompensated (b) Compensated	45
3.2	A circuit of LFR as a two-port network.	46
3.3	PFC based on a boost converter	47

3.4 Event-triggered SMC for PFC 50
3.5 Principle of HM-SMC 51
3.6 Power factor correction for SMC and ETSMC and the corresponding switching signal 51
3.7 Adaptive band for Event-triggered SMC for PFC 52
3.8 Fixed band for HM-SMC 52
3.9 Experimental setup 53
3.10 Experimental validation. CH1: Rectified AC Input Voltage V_1 (50 V/div). CH2: Inductor Current I_L (100 mA/div). CH3: Switching Pulses 54

4.1 Block diagram of switching converter emulated as ASLFR 58
4.2 PFC based on a boost converter 59
4.3 Region of Existence 62
4.4 Adaptiviy of r to load resistance variation 65
4.5 Adaptiviy of r to input voltage variation 65
4.6 Adaptiviy of r to reference voltage variation 65
4.7 Representing a combination load as equivalent resistive load $R_{eq} = \frac{V_o}{I_o}$ 66
4.8 System response and R_{eq} profile for a CPL load 66
4.9 Output Voltage waveform under load change 67
4.10 %THD in input current for the three controllers. 67
4.11 Experimental setup 68
4.12 Response of ASLFR based controller to Test Case-I. CH1: Rectified AC Input Voltage V_1 (40 V/div). CH2: Inductor Current I_L (500 mA/div). CH3: output capacitor voltage V_o (100 V/div). Time base 10 ms/div. 69
4.13 Input Current, Input Voltage and Output Voltage waveform for Test Case-I 69
4.14 Harmonic spectrum of the input current for the two loads of Test Case-I 70
4.15 Response of ASLFR based controller to Test Case-II. CH1: Rectified AC Input Voltage V_1 (40 V/div). CH2: Inductor Current I_L (200 mA/div). CH3: output capacitor voltage V_o (100 V/div). Load Resistance 300 Ω and V_{ref} 150 V. 70
4.16 Input Current, Input Voltage and Output Voltage waveform for Test Case-II 71
4.17 Response of ASLFR based controller to Test Case-III. CH1: Rectified AC Input Voltage V_1 (40 V/div). CH2: Inductor Current I_L (200 mA/div). CH3: output capacitor voltage V_o (100 V/div). Time base 20 ms/div. Load Resistance 300 Ω and V_{in} 100 V. 71
4.18 Input Current, Input Voltage and Output Voltage waveform for Test Case-III 72
4.19 Permissible and measured 3^{rd} Harmonic current at different load operating points. 72
4.20 Single stage Power factor correction for Classical and Event-triggered ASLFR. 73
4.21 Switching Pulses corresponding to σ change. 74
4.22 Evolution of error for Classical and Event-triggered ASLFR. 74
4.23 Input Current for the two cases. 74
4.24 Permissible and measured Harmonic current for 150 W load. 75
4.25 Event-triggered ASLFR adoption at different load levels. 75
4.26 Permissible and measured 3^{rd} harmonic at different load conditions. 76

5.1 Power circuit of the modular three-phase ac-dc converter using Ćuk rectifier modules. 79
5.2 Equivalent circuit of the isolated PFC based Ćuk converter when referred to the primary side 80
5.3 Eigen value plot: variation in load 87
5.4 Eigen value plot: variation in α 87
5.5 Eigen value plot: variation in line voltage 88
5.6 Adaptiviy of r to load resistance variation 89
5.7 Adaptiviy of r to input voltage variation 89
5.8 Adaptiviy of r to reference voltage variation 90
5.9 %THD in Phase A input current for the two controllers under comparison. 90
5.10 Experimental setup 91

5.11 Three-phase source currents at 1kW 93
5.12 Unity power factor correction in Phase A 93
5.13 Harmonic content of input current 1kW 93
5.14 System response to Test Case-II: Load change from 500W to 750W. Input Phase Voltage V_{sa} (100 V/div), Input Current I_{sa} (5 A/div), Output voltage V_o (200 V/div), Load current I_o (1 A/div), Time base 20 ms/div. 94
5.15 System response to Test Case-II: Load change from 750W to 500W. Input Phase Voltage V_{sa} (100 V/div), Input Current I_{sa} (5 A/div), Output voltage V_o (200 V/div), Load current I_o (1 A/div), Time base 20 ms/div. 94
5.16 System response to Test Case-III: Input Phase Voltage V_{sa} (100 V/div), Input Current I_{sa} (2 A/div), Output voltage V_o (200 V/div), Time base 50 ms/div. 95
5.17 System response to Test Case-IV: Input Phase Voltage V_{sa} (100 V/div), Input Current I_{sa} (2 A/div), Output voltage V_o (200 V/div), Time base 50 ms/div. 95
5.18 Harmonics current as a function of harmonic order and output power versus IEC 61000-3-2 Class A limits. 96

6.1 PFC based on a boost converter 103
6.2 Dual loop control structure 104
6.3 Frequency domain plots for open-loop transfer function and closed-loop gain of the current-loop: (a) magnitude and (b) phase. 105
6.4 Frequency domain plot for open-loop transfer function and closed-loop gain of the volatge-loop: (a) magnitude and (b) phase. 106
6.5 Load transient operation results with proposed ISM based controller 108
6.6 Plot of the switching function s 108
6.7 Steady state response using nominal controller. 109
6.8 System response using nominal controller against the external disturbance. 109
6.9 System response using nominal controller +ISMC against the external disturbance. 110
6.10 Steady state result for reduced parameters using nominal control. 110
6.11 Steady state result for reduced parameters using nominal with ISM based control. 111
6.12 A Z source converter 111
6.13 Pole zero map of control-to-capacitor-voltage transfer function for a symmetrical full order and reduced order ZSC 113
6.14 Dual loop control structure 114
6.15 Current-loop frequency domain plot for open-loop transfer function and closed-loop gain: (a) magnitude and (b) phase. 115
6.16 Voltage-loop frequency domain plot for open-loop transfer function and closed-loop gain: (a) magnitude and (b) phase. 115
6.17 Pole zero map with $L_2 < L_1$ full order and reduced order ZSC 116
6.18 Effect of asymmetry due to reduction in sensed inductor L_1 size 117
6.19 Effect of asymmetry due to reduction in unmodeled inductor L_2 size 118
6.20 System response to external disturbance in the input channel 118
6.21 System response to external disturbance in the generated reference current 119
6.22 Transient response to load change 119
6.23 Switchng variable for load variation in ZSC 120

List of Tables

Table	*Title*	*page*
2.1	System Parameters	34
3.1	Classification of Equipment According to IEC610000-3-2 (2014)	43
3.2	Harmonic limits for Class D equipments	44
3.3	System Parameters	53
4.1	System Parameters	64
4.2	Comparison of simulation results	68
5.1	System specification and parameters	80
5.2	Comparison of simulation results	91
5.3	Experimental Set-up Component Specifications	92
6.1	System Parameters	105
6.2	System Parameters of Z source converter	113

List of Symbols

Symbol	Description
β	constant even number
$\alpha_1,\ \alpha_2,\ \alpha_3$	Class $-\kappa_\infty$ functions
γ	$-\kappa$ function
L	Lipschitz constant
σ	ETSMC design parameter
t_i	Sequence of triggering instants
T_i	Inter execution time
$C_1,\ C_2,\ C_f,\ C_o,\ C_{in}$	Capacitors
$L_1,\ L_2,\ L_f,\ L_o$	Inductors
$R,\ R_1,\ R_2,\ R_L$	Resistors
D	Effective duty cycle
n	Transformer ratio
V_o	Output Voltage
V_{in}	Input Voltage
c	Coefficient matrix
s	Switching surface
$\tilde{e}$	Difference between state and its reference
e	Difference between last triggered and present state
V	Lyapunov function
α	Tuning parameter
Ω	Sliding band
A	System matrix
B	Input matrix
$a,\ b,\ \lambda,\ \mu,\ \Gamma,\ \beta$	positive constants
Δ	sliding band size
ψ	Uncertainty
ψ_m	Matched Uncertainty
u_o	Nominal Control
u_n	Non-linear ISM control
η	Reachability condition positive value
G	Sliding surface design matrix

List of Abbreviation

Abbreviation	Full form
AC	Alternating Current
ASLFR	Adaptive Sliding mode based Loss Free Resistor
BJT	Bipolar Junction Transistor
CCM	Continuous Current Mode
CEC	California Energy Commission
CMC	Current Mode Control
CoC	Code of Conduct
CPU	Central Processing Unit
CSCI	Climate Saver Computing Initiative
DC	Direct Current
DCM	Discontinuous Current Mode
DCR	Direct Current Resistor
DoE	Department of Energy
DPWM	Digital Pulse Width Modulation
EC	European Commission
EISA	Energy Independence and Security Act
EOF	Efficiency Optimized switching Frequency
EPA	Environment Protection Agency
ESR	Equivalent series resistance
ETC	Event Triggered Control
ETSMC	Event Triggered Sliding Mode Control
FET	Field Effect Transistor
HCM − BM	Hysteresis Control Mode-Burst Mode
HM	Hysteresis Mode
HM − SMC	Hysteresis Mode based Sliding Mode Control
ISMC	Integral Sliding Mode Control
IGBT	Insulated-Gate Bipolar Transistor
LFR	Loss Free Resistor
LQR	Linear Quadratic Regulator
MPPT	Maximum Power Point Tracking/Tracker
MOSFET	Metal-Oxide Semiconductor Field Transistor
PC	Personal Computer
PFC	Power Factor Correction
PFM	Pulse Frequency Modulation
PSM	Pulse Skipping Modulation

Abbreviation	Full form
PT	Pulse Train
PWM	Pulse Width Modulation
QSMC	Quasi Sliding mode Control
RMS	Root Mean Square
SCM	Skip Cycle Modulation
SLFR	Sliding mode based Loss Free Resistor
SMC	Sliding Mode Control
THD	Total Harmonic Distortion
VM	Voltage Mode
VSS	Variable Structure System
ZCS	Zero Current Switching
ZSC	Z-Source Converter
ZVS	Zero Voltage Switching