

Decomposable OFETs with Cellulose-based Substrate and Gate Dielectric

The proliferation of disposable electronics has been surged by the increasing need for portable and efficient devices that are user-friendly and easily discarded into the environment. Impact of E-waste can be effectively suppressed by developing devices that can be decomposed in soil or water without creating any hazardous constituents after their lifespan. Apart from using nature-inspired gate dielectrics, the primary step for demonstration of biodegradable devices and systems is to use a substrate that is intrinsically biodegradable or decomposable in natural environments such as soil or water. After the life span, biodegradable devices will physically break down into non-harmful constituents that have less threat to the environment. Paper is one of the most abundantly available biodegradable substrates which offers required thermal strength and flexibility for the fabrication of OFET devices. Despite these advantages, the high surface roughness of the available paper substrates requires the use of planarization techniques prior to their utilization in device fabrication. To support biodegradability, plastic substrates were replaced by commercially available paper substrates to demonstrate decomposable flexible OFETs, in an effort to produce biodegradable and eco-friendly electronics. In this chapter, solution-processed OFETs were demonstrated on a paper substrate using CEC as primary gate dielectric and TIPS-Pentacene: PS to form an active layer, both dielectric and substrate offer eco-friendliness from process and material aspects. Moreover, a thick planarizing layer of polyvinyl alcohol (PVA) is used to achieve high surface smoothness and less absorbent surface. In comparison to natural protein dielectrics, devices with cellulose and its derivatives exhibit high thermal stability, flexibility, and good stability under a wide range of humidity levels due to their inherent stable characteristics. High electrical, and operational stability along with good transistor properties in extremely humid conditions were achieved in these devices. Most importantly, these devices were successfully decomposed in environment confirming excellent biodegradability which is highly essential for eco-sustainable electronics. These findings are recently been published (G. Konwar, S. Rahi, et al., 2023).

7.1 INTRODUCTION

Over the past few decades, flexible electronics fabricated on thin plastic substrates has been investigated as a viable low-cost technology for large area, conformable, and stretchable electronic systems due to the reduction in overall product weight in a significant way (Ma et al., 2020). However, the utilization of plastic substrates in flexible electronics is not a sustainable approach for the future advancement towards biodegradable and eco-friendly electronics as the plastic substrate remains non-biodegradable in the environment (Chatterjee & Sharma, 2019). For any system, the 90% of the overall weightage is based on the used substrate, on top of which other thin functional layers are deposited. For the development of disposable flexible devices, cellulose-based materials have been explored as functional layers for a variety of applications like transistors, batteries, and supercapacitors, due to their cost-effectiveness, abundant availability, lightweight, as well as biocompatibility and biodegradability or composability in nature (Park et al., 2018). Ongoing research suggests that disposable cellulose-based electronics may effectively substitute non-biodegradable devices across various applications, without compromising functionality and performance of them. Among cellulose-based substrates, paper is most suitable

one due to its available property of cost-effectiveness, recyclability, flexibility, and foldability (Jeong et al., 2018; Lien et al., 2014). Moreover, paper can be easily degraded in environment with the help of various fungus and bacterial reactions in water and soil due to the presence of a high amount of cellulose fibre in it. In addition, its eventual mass can be greatly reduced upon combustion, (Lien et al., 2014; Yoon et al., 2017) which can be an effective method to reduce the mass of E-waste produced by paper based flexible electronics. Organic transistors, which are probably the most crucial device component for flexible electronics, have been successfully developed on a variety of paper substrates including commercial photo paper, and starch paper (Jeong et al., 2018; Zocco et al., 2014) to achieve biodegradability. Recently from our groups, paper substrate was utilized with other polymer dielectric for the demonstration of high-performance OFETs, however, the decomposability was not discussed (Konwar, Raghuwanshi, et al., 2024). To achieve high performance and low voltage operation in organic transistors, gate dielectric plays a very crucial role. Hybrid gate dielectric combinations of inorganic/organic bilayer are often used to achieve high-performance organic transistors (Ortiz et al., 2010), however, these combinations are not completely degradable highlighting the need for pristine layers of natural materials with a high dielectric constant (k). Cellulose-based materials have been explored as gate dielectric in transistors (Cunha et al., 2022; Gaspar et al., 2023) essentially to enhance eco-friendliness and also to add stability in transistor performance in humid environment and high operating temperatures. Organic transistors operating at low voltages < 3 V have been demonstrated with cellulose based materials acting as a solid-state electrolyte gate dielectric in transistors (Gaspar et al., 2023), which helps in the formation of EDL due to migration and accumulation of mobile ions at the electrode and dielectric interfaces upon application of external electric field. This phenomenon helps in enhancing the gate capacitance density significantly, which effectively lowers the operating voltage in transistors. The migration of ionic mobiles and effective capacitance density are influenced by various factors including frequency, humidity, and temperature (Bonardd et al., 2018; Cunha et al., 2022; Jose et al., 2021) and is strongly dependent on the frequency. The capacitance of these dielectrics is high at very low frequencies, but sharply decreases at high frequencies as the dipoles cannot follow the changes in the electric field (Bonardd et al., 2018). Moreover, it had been observed that both humidity and temperature significantly affect the dielectric properties specifically at low frequencies (Jose et al., 2021). The capacitance increases due to the adsorption of water molecules in a humid environment, leading to enhancement in ionic conduction. The k value of cellulose-based dielectrics is found to increase upto annealing temperature of 50 °C, possibly due to the reduction of dipole-dipole interaction and an increased motion of polar groups and water dipoles (Cunha et al., 2021; Jose et al., 2021). An improvement in electrical performance of transistors with cellulose-based dielectrics had been reported upon heating upto temperatures of 50 °C, though a degradation in performance had been observed upon heating at higher temperatures due to the water release leading to loss of ionic conductivity, and also due to issues like adhesion to the semiconductor surface (Cunha et al., 2021).

In this chapter, flexible p-channel organic transistors with CEC as a gate dielectric in combination with paper substrate were reported. Reports on OFETs with unique material combinations of cellulose based gate dielectric and substrate are rare to find in the literature. A blend of TIPS-pentacene with polystyrene (PS), which has been an excellent choice for the demonstration of air-stable organic transistors for exploration of novel strategies, is used for formation of active layer as an example case for these biodegradable transistors. Fabricated flexible biodegradable transistors exhibited high performance for -5V operation with excellent saturation in the output characteristics along with remarkable environmental, operational, electromechanical, and thermal stability. Upon thermal annealing, the performance of devices did not degrade till temperature of 60 °C, indicating suitability for practical operating environments. Moreover, devices exhibited decent stability upon exposure to very high humidity. Two distinctly different approaches were applied to investigate biodegradability, i.e. decomposition in soil and combustion in fire. For decomposition in soil, devices were immersed in water-rich soil, leading to significant decomposition in about 20 days. Moreover, the combustion of devices in fire, one of the quickest methods for degradation, led to a significant reduction in mass of more than 75%,

leaving ashes primarily consisting of the remains of Ag bottom gate electrode and Au source/drain electrodes. Our results on demonstration of flexible devices with full decomposability in soil and high combustibility can be a significant step towards fully biodegradable flexible electronics to minimize the effects of e-waste on environment and soil.

7.2 EXPERIMENTATION

7.2.1 Device Fabrication and Characterization

A biodegradable paper substrate (PowerCoat HD 230 paper from Arjowiggins, surface roughness of <20 nm as per specifications) was used for device fabrication. Firstly, 3×4 cm size pieces of the paper substrate pasted on glass were cleaned with heavy N_2 blow. A polyvinyl alcohol (PVA) layer was deposited on the top of the paper substrates to enhance the smoothness. PVA layer was formed using solution processing with an 8 wt. % solution in deionized (DI) water, by spin coating at 1000 rpm for 60 s and followed by 10 minutes of annealing at 60 °C. Paper surface roughness was reduced by ~ 3.5 nm after coating the thin PVA layer as discussed in a previous report (Konwar, Raghuwanshi, et al., 2024). A 100 nm thick Ag layer was deposited using thermal evaporation to form the bottom gate electrode. 8 wt. % CEC in DMF was prepared by stirring for 24 hours at 60 °C and spin-coated at 2000 rpm for 60 s over Ag, followed by annealing at 50 °C for 48 hours to form approximately $\sim 650 (\pm 80)$ nm thick gate dielectric layer. Thickness values were measured by Dektak XT surface profiler. For the active layer, semiconductor polymer blend was prepared as reported earlier and drop cast on gate dielectric layer. Finally, 100 nm thick Au contacts were deposited by thermal deposition through shadow mask for top source/drain electrodes.

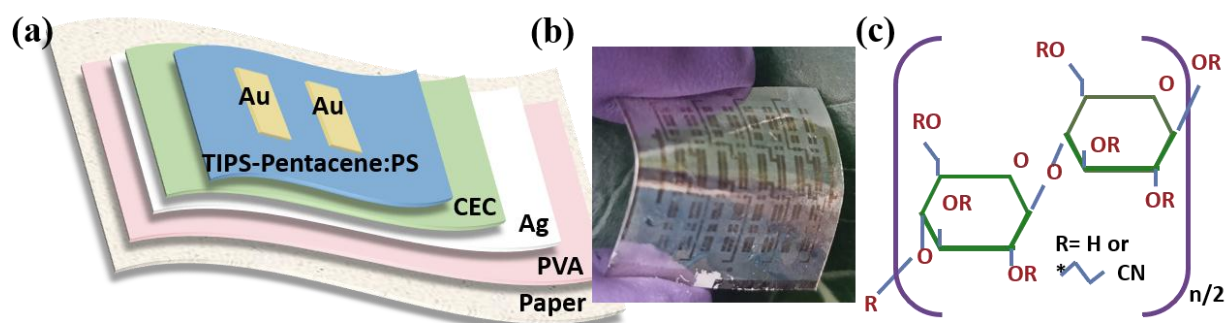


Figure 7.1 : (a) Schematic of fabricated organic transistor with cellulose based substrate and dielectric, i.e. paper and CEC, and (b) digital image of the substrate with array of organic transistors. (c) Chemical structure of CEC dielectric.

Figure 7.1 (a) and (b) show the device schematic with a real image of a fabricated transistor on paper substrate, respectively. Figure 7.1 (c) shows the chemical structure, which is synthesized from alkali cellulose and acrylonitrile by Michael addition, as reported in the literature (B. Wang et al., 2019). C_i for this CEC dielectric was measured through MIS structure ITO/CEC/TIPS-pentacene: PS/Au fabricated by the same process as of transistors. In addition, MIS structures ITO/CEC/Au were also fabricated for comparison of capacitance of dielectric. The capacitance versus frequency (C - f) measurements were done using a broadband dielectric spectrometer (BDS). Electrical characteristics of transistors were obtained in ambient conditions using Keithley 4200 SCS parameter analyzer. Performance parameters including process transconductance ($k_p = \mu \cdot C_i$), and V_{TH} were extracted from $(I_{DS})^{1/2}$ vs V_{GS} plot in saturation region of the device. Moreover, SS was directly obtained from transfer plot. The C_i value obtained from MIS structure was used to extract the μ and D_{it} values. To investigate the reliability of electrical characteristics during operation, devices were characterized for cyclic and bias-stress stability, to study the variation due to continuously changing and constant input gate voltage respectively. Effect of humidity exposure was extensively studied for these devices at different time duration up to relative humidity (RH) of ~ 80 %. For cyclic stability test, time-dependent current on-off

switching under voltage sweep between $V_{GS} = -5$ V and $V_{GS} = 5$ V was studied with various sweeping time delays under lab ambient and extreme humid conditions (RH $\sim$ 100 %). For bias-stress, a constant voltage bias of $V_{GS} = V_{DS} = -5$ V was applied to investigate the changes in the drain current. For electromechanical stability, devices were bent at various bending radius from 12 mm to 5 mm, and changes in the performance were studied. To investigate the effect of annealing on electrical performance, devices were annealed at temperatures of 40, 60, 80, and 100 °C respectively for 10 minutes, and changes in the performance were recorded. For studying the shelf life, variation in electrical characteristics in normal atmospheric ambient up to 7 weeks was studied.

7.2.2 Degradation Strategy

The primary objective of this study was to investigate the decomposability of these paper-based devices in the situations where they are discarded in soil or landfills. Though mimicking the exact condition for landfill was not possible, the investigation was carried out using soil of a typical countryside which is used to plant grass, trees, and farming due to availability of various microorganisms and nutrients. For this experiment, 250 g of dry soil was taken in a glass beaker and mixed with about 150 ml of water to make it semisolid facilitating easy immersion of the paper-based devices vertically. This mixture was very similar to the soil created for planting the paddy crops, which has a very high-water content. The paper substrate containing array of transistors was diagonally immersed with the help of a tweezer in a way so that about $\sim$ 15 % of top corner of the substrate is above the soil and remaining part is immersed inside. This ratio was not important; however, the aim was to leave a corner of the substrate for pulling it later from the soil and see if remaining part is decomposed due to biodegradation. To confirm the soil quality, i.e. and presence of necessary microorganisms and nutrients for plant life, some coriander seeds were also sowed on the top of the soil alongside the substrate in the same beaker. This beaker was kept in ambient conditions for 19 days after which further investigation was carried out to confirm its biodegradability. Being natural, the decomposition process takes its own course of time starting from nearly 20 days and even more.

On the other hand, combustion has been used as a method to quickly reduce the mass of the waste, though not preferred as a suitable way due to by-products such as smoke and heat. However, it can be applied to various plastic substrates where the first method, i.e. decomposability is not possible. To explore the combustibility of the paper devices, they were burnt directly with the help of a cigarette lighter. To compare this combustion with other flexible devices produced on conventional plastic substrates, ITO coated PET substrate with an array of transistors was used for the combustion experiment side by side with the paper devices. The percentage of weight loss from the remaining ashes after complete combustion for both types of devices were compared.

7.3 RESULTS AND DISCUSSION

7.3.1 Investigation of Film and Dielectric Properties of CEC

Figure 7.2 summarizes the film properties and dielectric properties of CEC dielectric. FTIR spectrum of dielectric film is shown in Figure 7.2 (a). In this spectrum, various absorption bands appear including 3580 cm^{-1} for stretching vibrations of -OH alcohol groups, 2930 cm^{-1} for C-H methyl and methylene groups; 2263 cm^{-1} for $\text{C}\equiv\text{N}$ (nitrile) group, 1430 cm^{-1} for CH_2 cellulose group, 1080 cm^{-1} for symmetrical and asymmetrical stretching vibrations of the ether groups (C-O-C). Both nitrile and ether groups are the main characteristics of CEC offering outstanding physical and chemical properties (Jia et al., 2015). The k value of CEC is increased with an increase in the polymer concentration of CEC due to the existence of strong $\text{C}\equiv\text{N}$ groups with high DS values (Cao et al., 2013). Further, the morphology of CEC gate dielectric was measured through AFM image, as shown in Figure 7.2 (b). The root mean square (RMS) roughness value of $3 (\pm 1)$ nm was found, confirming smoothness and suitability for low charge trapping. In general, smoother dielectric surface morphology is preferred for a better semiconductor: dielectric interface which helps in growing high-quality semiconductor film above the dielectric.

Figure 7.2 (c) shows the leakage current density vs applied voltage (J - V) across the same MISM structure. An acceptable leakage current density in the range of $< 10^{-6}$ A/cm² was obtained for -5 V to 5 V range. Figure 7.2 (d) shows the C - f plot with frequency varying from a low value of 0.1 Hz to a high frequency of 1 MHz for both MISM and MIM structures. As can be seen, a significantly high C_i value of 80 nF/cm² was obtained at 0.1 Hz, about 10 times higher than that obtained at 1 kHz, indicating the formation of EDL at low frequencies. C_i value is decreased with increased in frequency as a result of the slow polarization of the polar cyano groups present in the CEC dielectric, (Yan et al., 2023) however, at low frequency, complete dipole polarization results in a high C_i value (Bonardd et al., 2018).

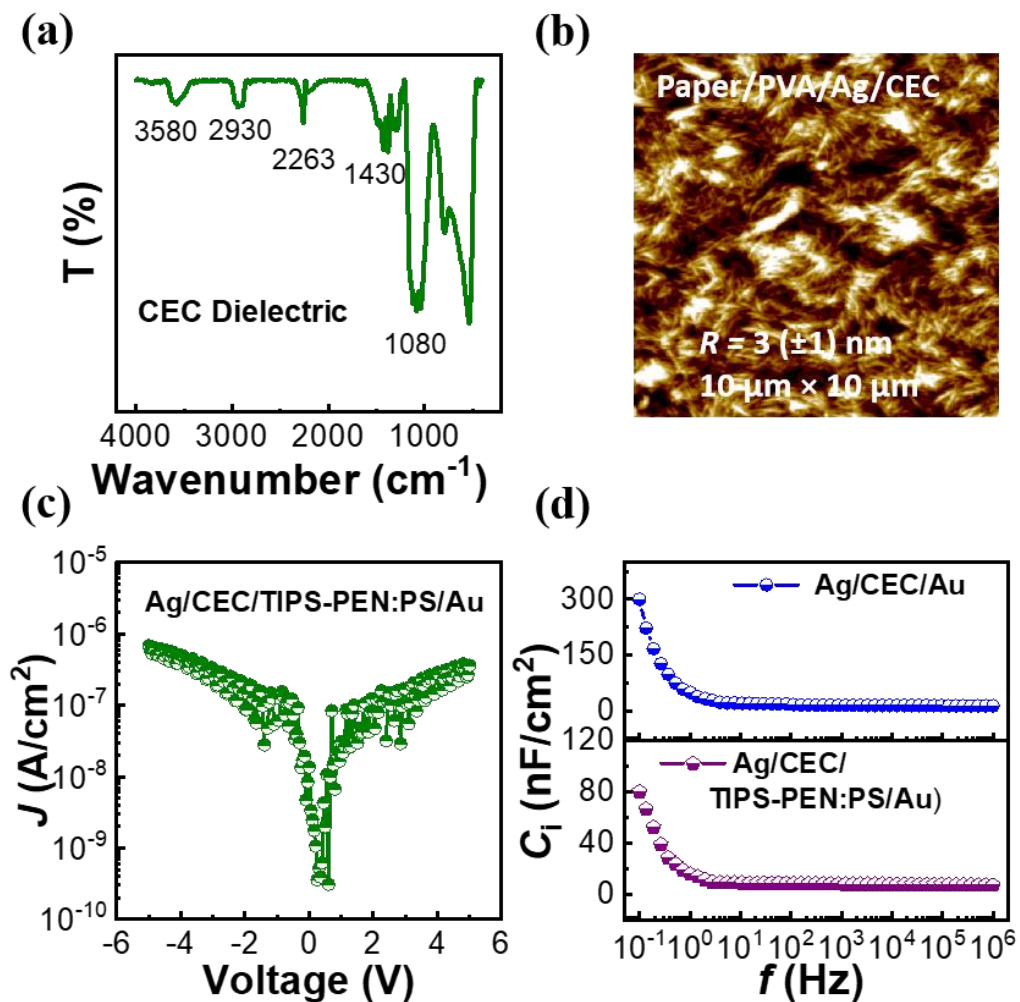


Figure 7.2 : (a) FTIR spectra to investigate bonding in CEC dielectric, (b) AFM image of top surface of CEC gate dielectric layer coated on Ag bottom gate electrode. (c) Leakage current density versus voltage (J - V) for MISM structure, and (d) C - f plot for the frequency range from 0.1 Hz to 1 MHz for both MIM and MISM structure.

For devices with solid state electrolyte gate dielectrics, the C_i value obtained at low frequencies is preferred for parameter extraction, to avoid the overestimation of μ and underestimation of D_{it} . Moreover, MIM structure with pristine CEC, yielded a very high value of 300 nF/cm² at 0.1 Hz and ~ 16 nF/cm² at 1 kHz. The k value for CEC dielectric was extracted to be 12.6 at 1 kHz from MIM structure, very similar to the earlier reported values extracted for 1 kHz (Faraji et al., 2016). Quite understandably, due to the presence of a phase separated dielectric layer of PS in series, the C_i obtained from MISM structure is lower. High C_i is one of the essential properties of dielectric materials for high performance organic transistors (Haase et al., 2019). k_p ($\mu \cdot C_i$), a fairly normalized performance parameter, was utilized to evaluate the performance of the transistors.

7.3.2 Transistor Performance

Typical transfer and output plots for a particular p-channel organic transistor with CEC gate dielectric are shown in Figure 7.3 (e) and (f) respectively for -5 V operation. Excellent transfer characteristics in saturation can be observed for V_{DS} of -5 V, in Figure 9.1 (e). Gate leakage current (I_G) is also added in the plots, which was in the range of 10^{-9} A. A remarkable saturation in the output characteristics was observed between V_{DS} of -4 to -5 V, for all the V_{GS} values (0 to -5 V, -1 V step), as shown in Figure 9.1 (f). A current crowding is seen in the output characteristics at low V_{DS} . The current crowding is generally a result of various parasitic leakage currents which are observed in these devices having large un-patterned gate electrodes and also due to bad contacts. Possible reasons for bad contacts in solution-processed organic devices include injection barrier between metal contacts and semiconductor and rough surface morphology of semiconductor. These current crowding effects can be minimized upon patterning the gate electrode and by having good source/drain contacts.

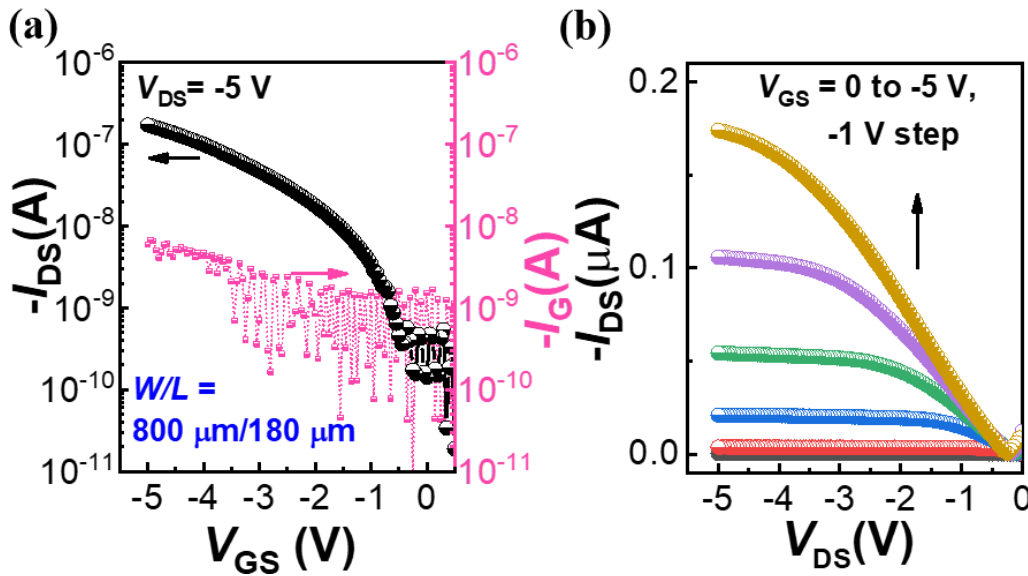


Figure 7.3 : (a) Transfer, and (b) output characteristics of a typical fabricated transistor on paper substrate. Gate leakage current (I_G) is also shown in transfer plot.

Moreover, negligible hysteresis was observed in the characteristics of these devices upon applying dual-sweep of voltage. All the performance parameters including k_p , V_{TH} , and SS were extracted from transfer characteristics in saturation regime using standard formulas as discussed earlier (Gargi Konwar et al., 2023; Raghuwanshi, Bharti, Varun, et al., 2016) and summarized in Table 7.1. An average V_{TH} of $-0.5 (\pm 0.3)$ V was achieved which is suitable for low-voltage operation. These devices exhibited maximum and average k_p values of 4.8 and $3.8 (\pm 1)$ $\text{nF V}^{-1} \text{s}^{-1}$ respectively. Considering the electrolyte gate dielectric, the field-effect mobility values were extracted using C_i value obtained at 0.1 Hz, i.e. 80 nF/cm^2 yielding average mobility values of $4.7 (\pm 0.8) \times 10^{-2} \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ for this case. A decently high I_{on}/I_{off} of $\sim 10^3$ and SS of $\sim 0.63 \text{ V/dec.}$, were obtained indicating very good p-channel performance. Corresponding D_{it} values were extracted from SS values and found to be $4.8 (\pm 2.7) \times 10^{12} \text{ cm}^{-2} \text{eV}^{-1}$. Lower values of SS and D_{it} are indicative of better dielectric-semiconductor interface, which has a key role in achieving low voltage operation (Raghuwanshi, Bharti, Varun, et al., 2016).

Table 7.1 : Summary of performance parameters for a set of OFET devices. Values of μ and D_{it} were extracted using C_i obtained at a frequency of 0.1 Hz.

C_i (nF cm^{-2})	k_p ($\text{nF V}^{-1} \text{s}^{-1}$)	V_{TH} (V)	I_{on}/I_{off}	SS (V/dec.)	μ ($10^{-2} \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$)	D_{it} ($10^{12} \text{ cm}^{-2} \text{eV}^{-1}$)
80	$3.8 (\pm 0.7)$	$-0.5 (\pm 0.3)$	$\sim 10^3$	$0.6 (\pm 0.3)$	$4.7 (\pm 0.8)$	$4.8 (\pm 2.7)$

7.3.3 Effect of Humidity and Cyclic Stability

Devices were comprehensively studied for performance variation upon exposure to high humidity, to investigate the moisture resistance. Figure 7.4 (a) shows the transfer characteristics of a particular device upon exposure to a high humidity (RH ~ 80 %) for total exposure time of 0 (pristine), 15, 30, 45, and 60 minutes. It was observed that though there was no significant variation in performance for short exposure time of 15 minutes, a degradation in device performance was observed for further exposure. To investigate it further the variation in I_{on} and SS are plotted, as shown in Figure 7.4 (b). It was found that very small changes of 2.4 % and 6.7 % in I_{on} and SS respectively were observed upon initial exposure for 15 minutes. However, upon further exposure, degradation in the device performance was observed. Upon 60 minutes of total exposure, 54 % reduction in I_{on} was seen whereas the SS increased from 0.59 to 1.19 V/dec. These observations are in line with the earlier reports according to which the initial exposure of humidity helps in small performance improvements due to water adsorption, following deterioration in performance upon further continuous exposure (Pereira et al., 2014). Initially, the adsorbed water dissociates into protons (H^+) and hydroxyls (OH^-), which causes high ionic conduction supporting the EDL. However, excessive adsorption of water molecules on the surface of semiconductor and at the dielectric: semiconductor interface causes a decay in performance as the adsorbed water molecules fill the interface and saturate the polarization of polar groups of dielectrics (Subbarao et al., 2015).

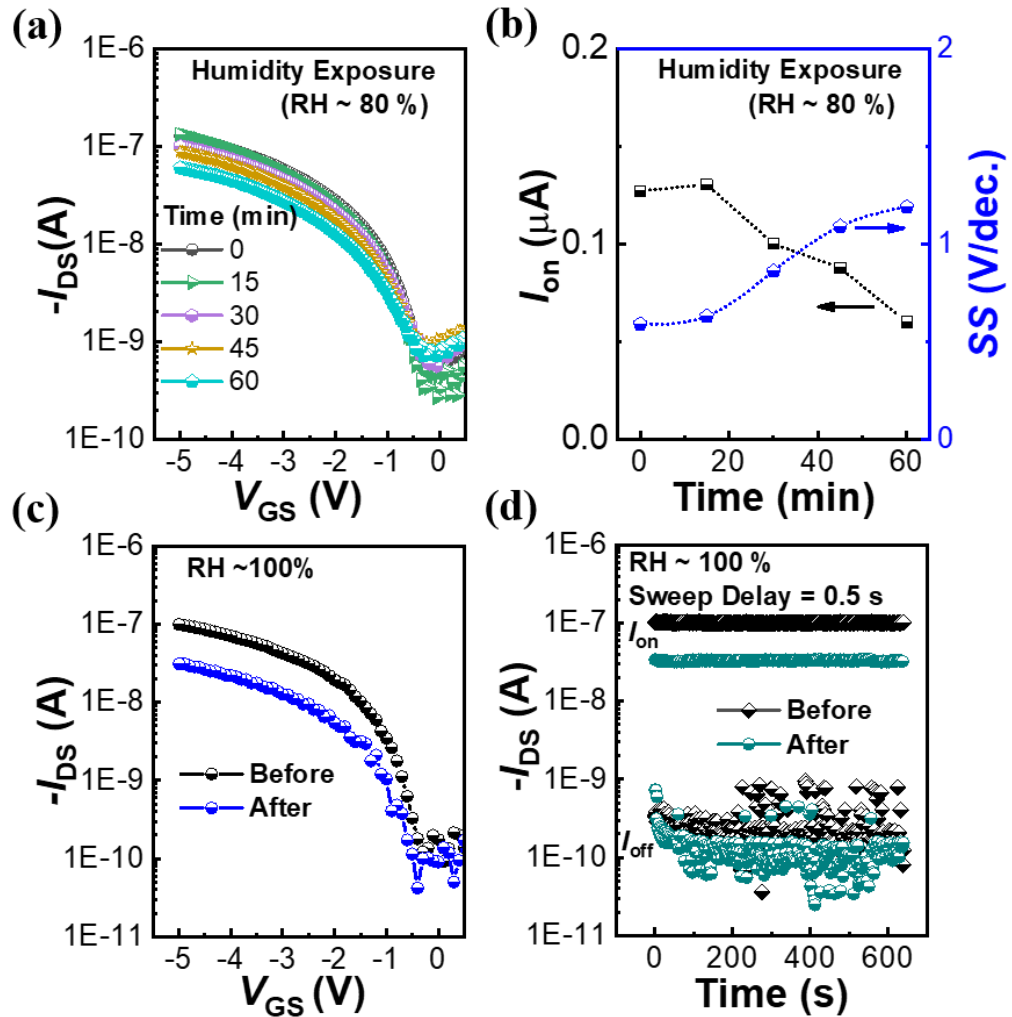


Figure 7.4 : Investigation of performance variation upon humidity exposure on devices. Change in transfer (a), and I_{on} & SS (b) at different humidity exposure times under RH of ~ 80%. Plots of transfer characteristics (c) and cyclic stability (d) before and after exposure of device to extremely humid conditions with very high humidity (~RH ~100 %). Cyclic stability was measured under application of a time-dependent voltage sweep between $V_{GS} = -5$ V and $V_{GS} = 5$ V with a sweep delay of 0.5 s for 10 minutes before and after humidity exposure.

In addition, the devices were exposed to extremely humid conditions with very high humidity (RH $\sim 100\%$) for sufficient time to observe the changes in the characteristics, as shown in Figure 7.4 (c). An expected shift in the characteristics was observed. Figure 7.4 (d) shows the results of cyclic stability measurements before and after exposure of humidity of RH $\sim 100\%$, in which I_{on} and I_{off} are recorded upon application of a continuous voltage pulse with V_{GS} of -5 V and 5 V for sweep delay of 0.5 s for 10 minutes . As it can be seen from this plot, $I_{\text{on}}/I_{\text{off}}$ of $\sim 10^3$ was maintained for entire duration of experiment indicating decent switching stability of fabricated devices before and after humidity exposure. Though the devices showed high cyclic stability with time, the performance shift seen during humidity exposure was also reflected in cyclic stability measurements. These results indicate the combination of high moisture resistance and the possible absence of moisture-based polarization effects up to a good extent for the proposed device. Similar natural dielectric-based devices such as with cyanoethylated pullulan (Lopinski et al., 2017), though done on rigid silicon substrates different from our case, were reported to show low degradation ($< 20\%$) in performance in lab environments of humidity. However, comparing the humidity resistance with any other report can be difficult considering the different device structures and operating conditions.

7.3.4 Operational and Bending Stability

Figure 7.5 summarizes the results of bias-stress stability and bending. For utility of these paper transistors in various real-world applications, high electrical stability during operation is essential. Figure 7.5 (a) shows the change in normalized drain current with time on applying a constant bias-stress at $V_{\text{GS}} = V_{\text{DS}} = -5\text{ V}$ for 4600 s . During this entire stress period, a negligible decay of less than 6% in I_{DS} was observed, indicating high bias-stress stability. The transfer characteristics of before and after bias stress are shown in the inset of Figure 7.5 (a). Variation in I_{DS} primarily occurs due to the trapping of charge carriers at dielectric: semiconductor interface which is common for organic transistors (Subbarao et al., 2015). Though, an increase in I_{off} was seen in the transfer characteristics, that can be merely due to the fluctuation in I_{off} levels in the range of $\sim 10^{-10}$ to $\sim 10^{-9}$ for these devices. These off-state leakages can be significantly reduced by achieving proper contact with the electrodes during characterization as well as by eliminating or minimizing the gate to source/drain electrodes by patterning or similar strategies during fabrication.

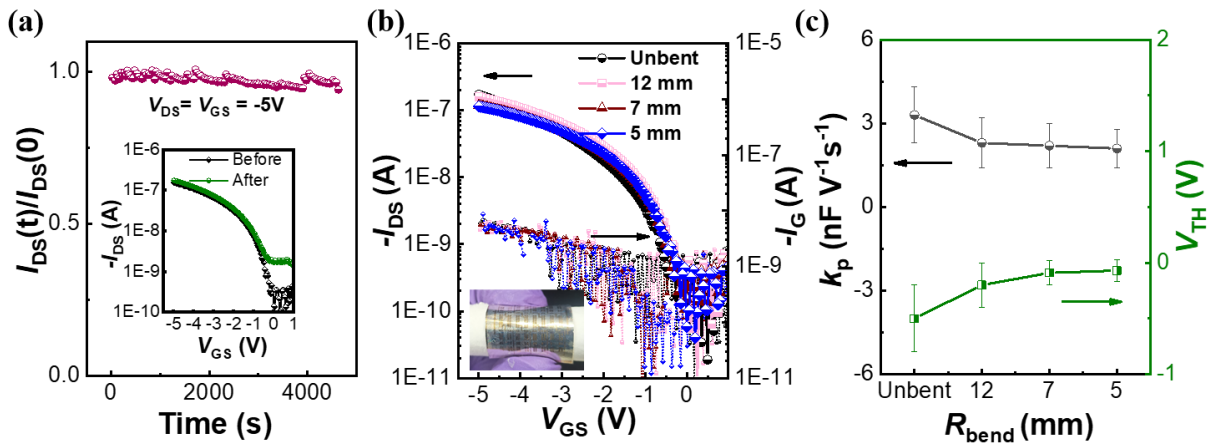


Figure 7.5 : (a) Electrical stability under constant bias of $V_{\text{GS}} = V_{\text{DS}} = -5\text{ V}$ for 4600 s . The decay in normalized drain current is shown. Transfer characteristics before and after bias-stress are shown in inset. (b) Transfer characteristics upon bending at different bending radius from 12 mm to 5 mm . A substrate under bending is shown in the inset. (c) Variation of k_p & V_{TH} upon bending.

Figure 7.5 (b) shows the transfer characteristics of a particular unbent device ($R_{\text{bend}} = \infty$) along with characteristics upon being subjected to bending with decreasing different R_{bend} of 12 mm , 7 mm , and 5 mm respectively. The inset shows the bending strategy which results in a tensile stress on the devices being on outer surface of the bending curve. These paper transistors were bent along the conducting channel so that there was no change in the channel length (L) of the device.

As can be seen in this plot, bending causes small variation in the transfer characteristics of these devices. To investigate it further, average of the crucial performance parameters k_p , and V_{TH} were plotted from multiple devices, as shown in Figure 7.5 (c). The average k_p value varies from 3.5 to 2.3 nF V⁻¹ s⁻¹ upon first bending cycle ($R_{bend} = 12$ mm). However, it is fairly constant upon further bending at R_{bend} of 7 and 5 mm with negligible variation in k_p from 2.3 to 2.1 nF V⁻¹ s⁻¹, indicating a decent stability in characteristics upon bending. As can be seen, most of the changes happen during the first bending ($R_{bend} = 12$ mm), followed by a negligible variation upon further bending. Summary of performance parameters of organic transistors upon bending is given in Table 7.2. As one of the main effects of bending is deterioration of dielectric: semiconductor interface (Raghuwanshi, Bharti, Varun, et al., 2016), the D_{it} values were also extracted showing a typical decay of interface upon bending. These results confirm good p-channel operation even after extreme bending with a very low R_{bend} value of 5 mm. Stability in characteristics upon bending in organic transistors can be attributed due to the properties of substrate, dielectric, dielectric: semiconductor interface, and other materials components used in fabrication. Paper substrate and CEC gate dielectric, both of which are used in fabrication of organic transistors in this case, have shown excellent electromechanical stability (Faraji et al., 2016; Jia et al., 2015). The variation in the transistor performance occurs primarily due to the generation of microcracks in the semiconductor film upon bending (Raghuwanshi, Bharti, Varun, et al., 2016).

Table 7.2 : Summary of performance parameters of bending study. D_{it} was extracted using G_i value obtained at frequency of 0.1 Hz.

R_{bend} (mm)	k_p (nF V ⁻¹ s ⁻¹)	V_{TH} (V)	I_{on}/I_{off}	SS (V/dec.)	* D_{it} (10 ¹² cm ⁻² eV ⁻¹)
12	2.3 (±0.9)	-0.2 (±0.2)	~ 10 ³	0.95 (±0.44)	7.43 (±3.71)
7	2.2 (±0.8)	0.09 (±0.1)	~ 10 ³	0.99 (±0.40)	7.82 (±3.38)
5	2.1 (±0.7)	-0.07 (±0.1)	~ 10 ³	1.07 (±0.48)	8.54 (±4.06)

7.3.5 Effect of Annealing on Transistor Performance

Effect of annealing temperature on transistor performance was studied with varying the temperature from 40 to 100 °C with a step of 20 °C. For the same, transistors were immediately characterized for electrical characteristics after being annealed at a particular temperature for 10 minutes. Figure 7.6 (a) shows the plots of transfer characteristics for pristine as well as after being annealed at various temperatures. An improvement in the drain current was observed for annealing at temperatures up to 60 °C, followed by a decrease in performance upon further increase in annealing temperature, i.e. at 80 and 100 °C. The changes in crucial performance parameters k_p and V_{TH} are directly extracted from the transfer curves of Figure 7.6 (a) and shown in Figure 7.6 (b). The V_{TH} is fairly constant while k_p is increasing upon annealing up to temperatures of 60 °C, as shown the plot of variation in k_p , & V_{TH} . These devices were again characterized after being rested for a day to see if there was any recovery, however, no recovery was observed, as can be seen from Figure 7.6 (a) & (b). This investigation indicates suitability for operation of these devices for temperatures up to 60 °C, which is more or less maximum temperature for real-life applications for wearable electronics. The thermogravimetric analysis (TGA) can be used to estimate the thermal durability of CEC material. As reported earlier, two phases of decomposition happen in CEC film (Jia et al., 2015). The first phase possibly occurs due to the rupture of cyanoethyl groups, which has a decomposition temperature of ~ 276 °C. The second phase of decomposition occurs at ~ 360 °C due to the damage to cellulose network. The improvement in the electrical characteristics at initial annealing temperatures and degradation upon annealing at higher temperatures is very much in agreement with the earlier reports (Cunha et al., 2021; Jose et al., 2021). As also discussed in the introduction section, the initial enhancement of performance can also be attributed to the increase in the k value of cellulose-based dielectrics upon annealing

at temperatures lower than 50 °C due to the reduction of dipole-dipole interaction and an increased motion of polar groups. Moreover, the degradation in performance upon heating at higher temperatures can be attributed to the loss of ionic conductivity caused by release of water molecules. Other possible causes of degradation in performance upon further annealing at higher temperatures can be reduced adhesion to the semiconductor surface the decomposition of CEC dielectric film due to the breakage of cyanoethyl groups and cellulose network and the formation of permanent cracks on semiconductor surface, and generation of defects in active layer, dielectric, and dielectric: semiconductor interface (Raghuwanshi et al., 2019). The degradation of CEC dielectric upon annealing had been earlier confirmed by thermogravimetric analysis (Jia et al., 2015).

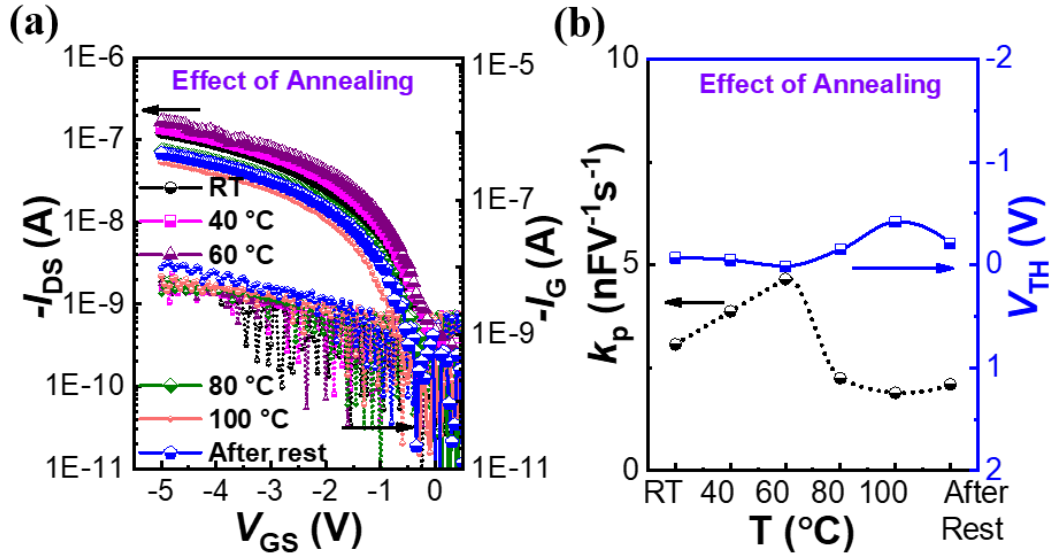


Figure 7.6 : Effect of annealing on device performance. (a) Transfer characteristics after annealing at various temperatures from 40 to 100 °C and being rested the device for one day. (b) Variation in k_p & V_{TH} with annealing temperature. A decay in performance is observed after 60 °C.

7.3.6 Effect of Environment on Transistor Performance

Figure 7.7 (a) and (b) show the results of shelf-life stability study of these paper transistors. The variation in the transfer characteristics with time up to 7 weeks upon exposure to normal ambient conditions is shown in Figure 7.7 (a), and the plots of extracted values of performance parameters k_p and V_{TH} are shown in Figure 7.7 (b).

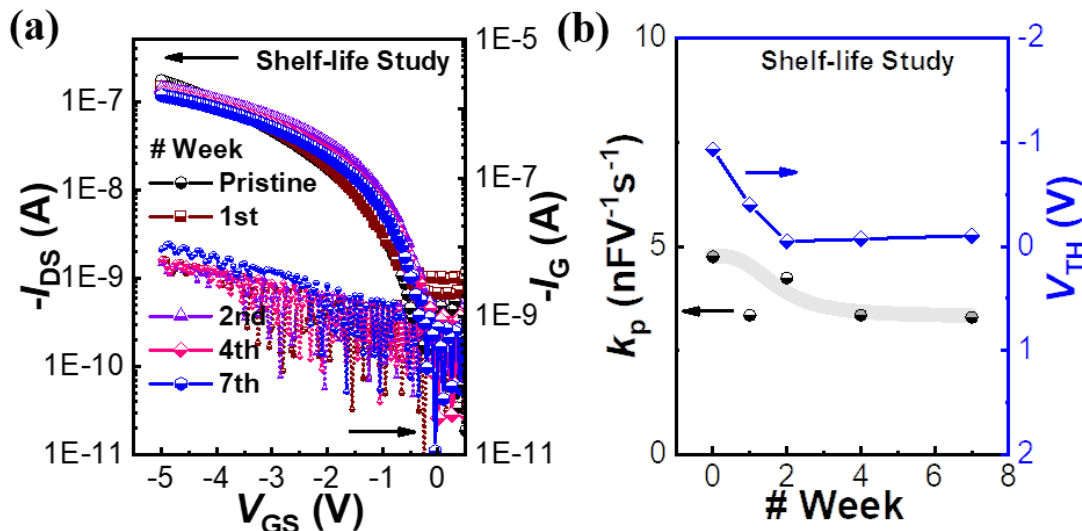


Figure 7.7 : Shelf-life study of the fabricated paper devices up to 7 weeks, shown through variation in transfer characteristics upon exposure to normal ambient conditions (c), and in performance parameters k_p & V_{TH} (d), for a particular transistor.

It was observed that k_p changes by about 31 %, whereas V_{TH} changes from -0.93 V for pristine to -0.10 V (0.83 V change) after 7 weeks of aging. Moreover, most of these changes occur during the initial 4 weeks of aging, followed by a fair stability after the same. The degradation of performance in ambient is mostly caused due to the effect of ambient humidity and temperature, and is typical for organic transistors (S. Rahi et al., 2022). Moreover, ambient conditions such as temperature and humidity are also known to affect the properties of cellulose due to its hygroscopic nature, due to which it absorbs water molecules on the surface resulting in change the dielectric properties,(Luo et al., 2023) leading to changes in the overall performance of the device. Moreover, adsorption of moisture can create traps on the surface of semiconductor leading to reduction in the device performance (Subbarao et al., 2015). These variations are not universal, and are bound to change as per the geographical locations and weather which have huge impact on day-to-day changes in ambient conditions. These devices exhibited good electrical characteristics up to 7 weeks, confirming decent air stability and shelf life, making them reliable applications.

7.3.7 Decomposition of Flexible OFETs in Soil

The investigation of biodegradability of fabricated transistors on paper substrate with CEC as gate dielectric was done by immersing the devices in water-rich soil at room temperature. The crucial steps of this investigation are summarized using digital pictures taken on day 1 and day 19 of experimentation, as shown in Figure 7.8.

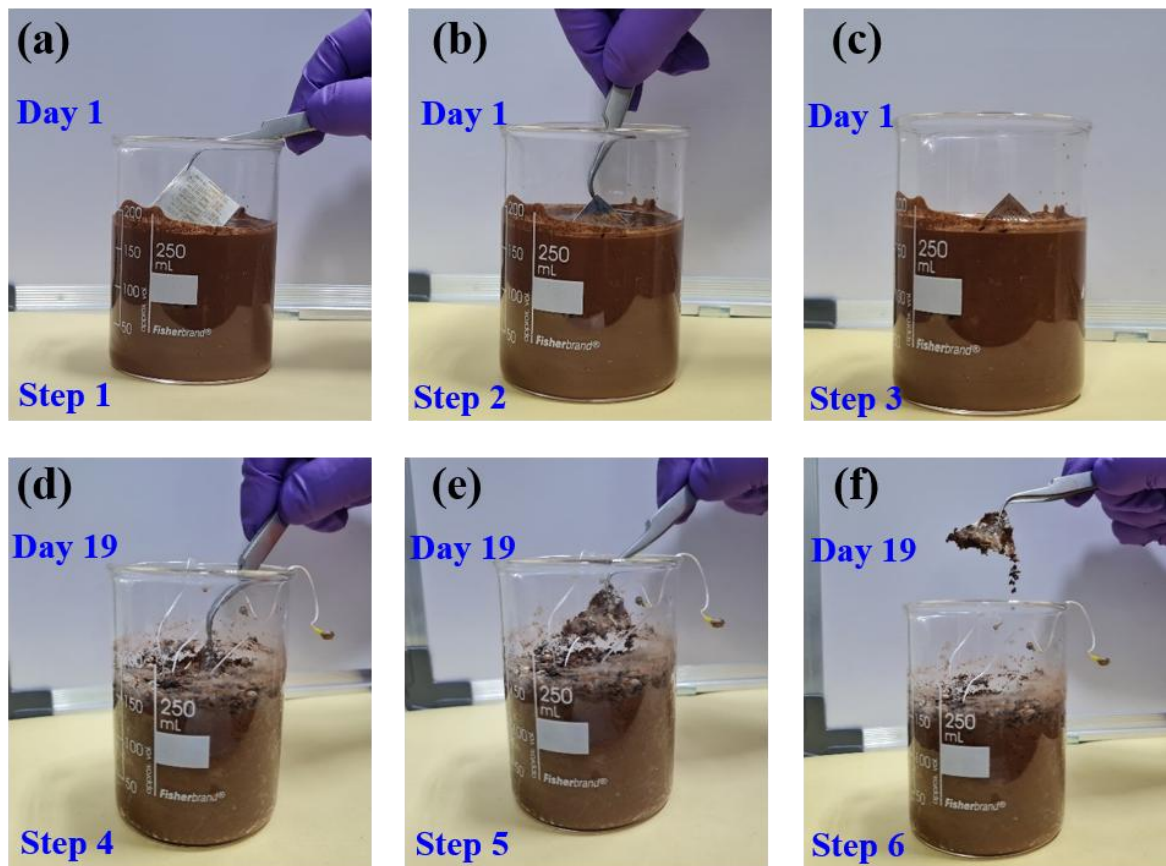


Figure 7.8 : Experimental investigation of decomposition of paper devices in soil. The sample was immersed diagonally in water-rich soil as illustrated sequentially in (a-c). Process of pulling out the substrate after 19 days is shown in (d-f), confirming the biodegradability of submerged part of the paper substrate with array of transistor devices.

As shown for step one on day 1 in Figure 7.8 (a), the devices were submerged diagonally in vertical direction in the semisolid soil which has capability to hold the substrate at any point when immersion is stopped. As shown in step 2 (Figure 7. 8 (b)), the substrate is submerged leaving a

top corner part of the substrate. As given in Figure 7.8 (c), step 3 shows the condition when tweezer is removed and substrate is left for settling into the soil. Figure 7.8 (d) shows the condition of the beaker after 19 days, along with the substrate ready to be pulled by the tweezer. As it can be seen, the coriander seeds were fully germinated indicating the presence of proper microorganisms for plants and confirming the quality of soil to be suitable for decomposition of substrate. Figure 7.8 (e) shows the process of the substrate being pulled out of soil with the help of the tweezer. In Figure 7.8 (f), the non-degraded part is shown completely out of the soil. As expected, most of the submerged part of the substrate was decomposed to become the part of the soil, whereas the part which was above the soil came out intact along with some part that was semi decomposed, which can be noticed in the picture. This semi-degraded part is from the region near the top surface of the soil, which is known to have a lesser amount of microorganisms compared to the part which is deeper inside. The degradation of paper-based devices in a soil environment primarily results from the breakdown of the structural integrity of the paper substrate. As the substrate decomposes, it facilitates the detachment and disintegration of the overlying thin organic layers such as the semiconductor and dielectric films. In contrast, non-biodegradable components like metal electrodes (e.g., Ag or Au) remain unaffected by microbial activity and persist as stable residues in the soil. Moreover, the decomposition of materials in soil is a biological process which is highly influenced by climatic factors including temperature, moisture content, and presence of oxygen, all of which can regulate the rate of decomposition (McClaugherty, 2001). Both temperature and moisture content are interrelated and the impact of temperature on decomposition is less pronounced under extreme moisture conditions. In this study, the experimentation was carried out at room temperature with the presence of adequate moisture which is needed for microbial activity to enhance the degradation mechanism. The water can easily penetrate the cellulose network and degrade its mechanical strength. Further, fungi and bacteria present in soil are considered to be the primary microorganism for cellulolytic degradation. Figure 7.9 shows the graphically illustration for microbial decomposition of cellulose in soil. Cellulase produced from the hydrolytic process of microorganisms, is the primary enzyme responsible for cellulose degradation.

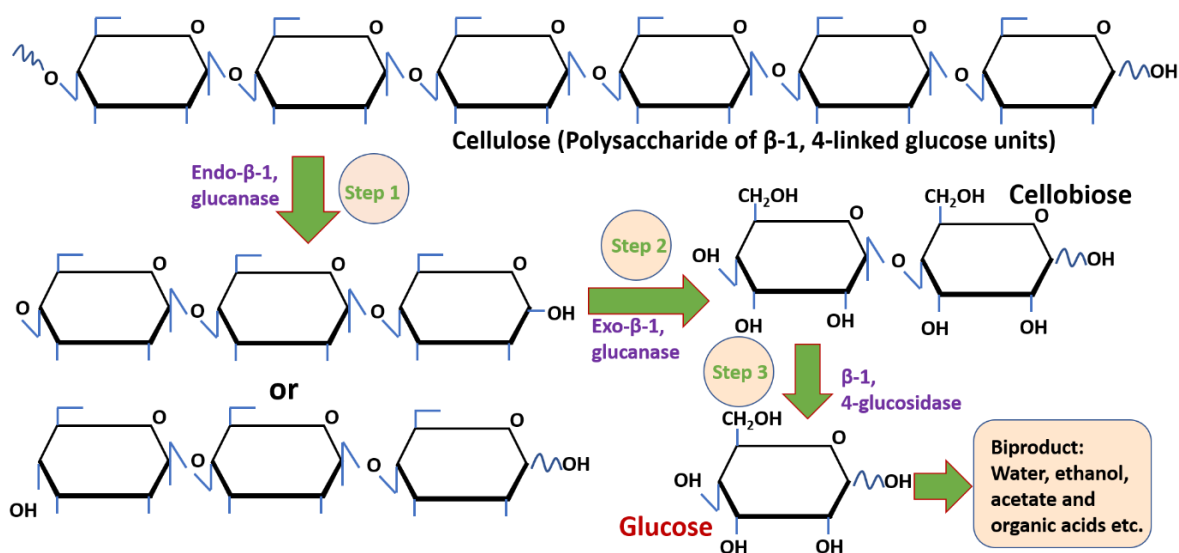


Figure 7.9 : Mechanisms for microbial decomposition of cellulose, the primary content of paper substrate, under soil environment. The cellulase enzymes presents in soil decompose the cellulose into glucose unit through the series of enzymatic reactions.

A series of enzymatic reactions happen to decompose the complex cellulose into free glucose molecules as shown in Figure 7.9, with the help of three cellulase enzymes i.e. endo- β -1,4-glucanase, exo- β -1,4-glucanase and β -1,4-glucosidase (Chandra et al., 2016; Juturu & Wu, 2014). In step 1, endo- β -1,4-glucanase hydrolyses the cellulose polymer, causing structural disruptions by breaking the internal bonds and expose individual polysaccharide chains. These exposed chains were then accessed by exo- β -1,4-d-glucanase either from the reducing or the non-reducing

end as shown in step 2, dividing them into two to four units to form tetra-saccharide or di-saccharide, like cellobiose. In the last step i.e., in step 3, these di, tri and oligo-saccharides were hydrolysed by β -1,4-glucosidase to form free glucose molecules (Juturu & Wu, 2014). It is difficult for enzymes alone to degrade complex crystalline cellulose structure efficiently; however, all enzymes together help in increasing the rate of hydrolysis. The free glucose unit is eventually converted to CO₂, water, ethanol or any organic acids depending upon the environmental conditions. The large amount of cellulose is broken down by cellulose-fermenting microorganisms in anaerobic environment of the soil (Eriksson, 1978). These cellulase enzymes degrade the other organic materials also in a significant way along with the degradation of paper substrates, making the organic devices biodegradable in the soil environment.

Table 7.3 : Summary of some recent reports on degradation of cellulose substrate-based devices through decomposition in soil

Substrate	Mechanism/Remarks	Time (days)	Ref.
Transparent paper	Decomposition due to microorganism in natural soil	40	(Gao et al., 2016a)
Nanopaper	More than 95% volume of the nanopaper sensor device was decomposed in soil	40	(Kasuga et al., 2019)
Cellulose	50% volume degradation in 20 days at 30 °C due to decomposition by microorganisms	-	(Tong et al., 2020)
Mulberry paper	Degraded in soil similar to copy paper, glucose content increased to 250 mg/dl in 14 days	14	(Qi et al., 2020)
Transparent cellulose paper	Degradation due to fungal growth, fungus produced in soil and sodium pyrophosphate mixture at 27 °C and 70 % RH, 2 weeks	80	(G. Li et al., 2020)
Nano-cellulose	Degradation in wet soil at room temperature	-	(Konganapuram Narasimma Bharathi et al., 2022)
Cellulose nanocrystal	Decomposition in natural soil upon exposure to sunlight at 35 °C, breakdown from the 7th day	-	(Thi et al., 2022)
PoweCoat HD 230 paper	Decomposition in water-rich soil, germination of coriander seeds for confirmation of presence of microorganisms	19	This work

Table 7.3 summarizes some recent results on degradation of cellulose paper-based devices through decomposition in soil. In year 2016, Gao et al reported biodegradation of transparent paper-based nanogenerator devices fabricated on transparent cellulose nanopaper (T-paper) and with polylactic acid (PLA) as electret which were decomposed almost completely in 40 days due to presence of microorganism in natural soil (Gao et al., 2016a). Similarly in 2019, Kasuga *et al.* reported the decomposition of more than 95 % of total volume of nanopaper based sensors in natural soil in 40 days. Another type of paper device i.e. mulberry paper based graphene strain sensor was degraded similarly to copy paper, as confirmed by the increase in glucose concentration to 250 mg/dl in 14 days in soil for both the substrates (Qi et al., 2020). Li et al chose to alter the properties of the soil by producing the fungus in fertile soil by mixing sodium pyrophosphate, and leaving it for two weeks at 27 °C and 70 % relative humidity, to enhance the biodegradation of cellulose in 80 days due to fungus, as reported in year 2020 (G. Li et al., 2020).

Interestingly, controlling the rate of degradation of paper by use of crosslinking agent was reported, specifically for the cases where cellulose is used in packaging (Konganapuram Narasimma Bharathi et al., 2022). Sunlight was also shown as an influencer in biodegradation (Thi et al., 2022). In this work, excellent decomposition of flexible organic transistors with the unique combination of paper substrate and CEC gate dielectric, both containing cellulose as primary structural element is reported. These devices were degraded in 19 days, which is in the lower side compared to most of the reports available in literature to date, confirming their high degree of biodegradability. Moreover, there is a scarcity of reports on demonstration of biodegradation in such a systematic manner, making this study very important for biodegradable electronics.

7.3.8 Combustion of Paper OFETs

The results of degradation process through combustion, which is the easiest way for reduction of mass of E-waste by converting it completely to ash or semi-burnt residues depending on the materials used in fabrication was studied as shown in Figure 7.10. The simple burning study for paper based devices is shown in Figure 7.10 (a, b, and c) representing the pristine state, burning process, and the final ash or residue respectively. Similarly, Figure 7.10 (d, e, and f) show the results of combustion study for a widely used typical flexible plastic substrate, i.e. ITO-PET, only for comparison. As can be seen, the paper based devices have reduced to ashes greatly, however, the plastic substrate resulted in a black rigid residue.

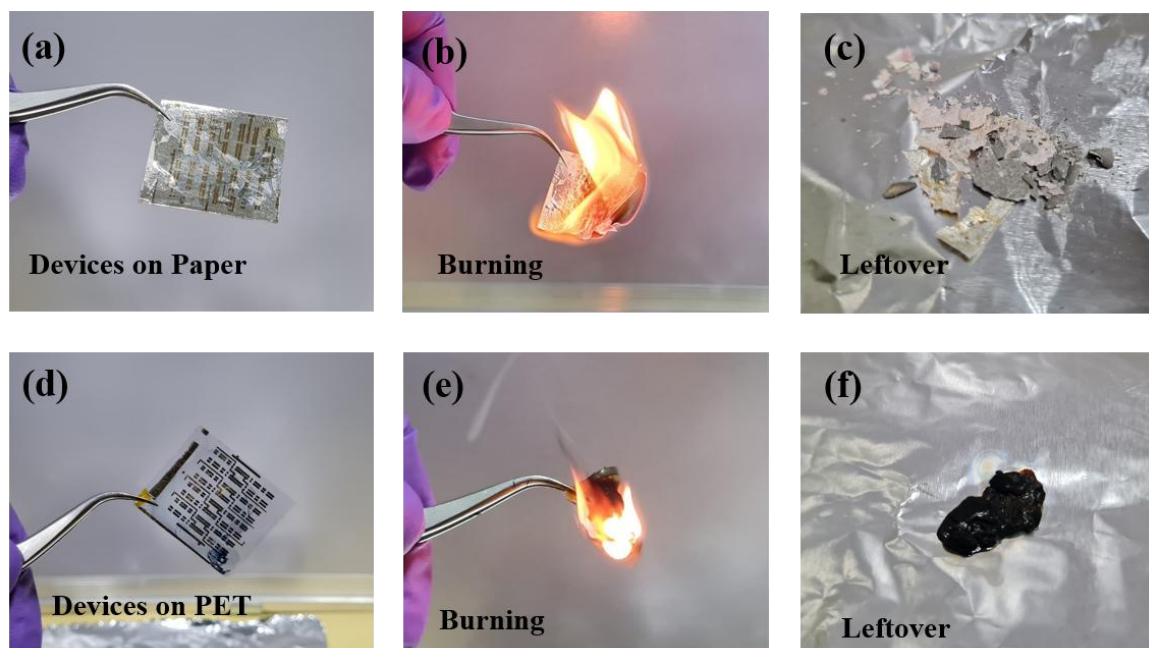


Figure 7.10 : A simple combustion strategy to degrade organic devices and calculate the loss of total mass from the leftovers. Step by step process to combust the devices with remaining ashes for (a-c) paper and (d-f) PET substrates.

Table 7.4 : Summary of results for combustion of devices on PET and Paper substrate.

Substrate	Time	Initial weight (mg)	Final weight (mg)	% of weight loss
PET	~8 s	132.4	100	24.2
Paper	~12 s	152.8	37.3	75.5

The time taken for combustion and percentage of weight loss including the initial and final weight for both paper and ITO-PET based devices is summarized in Table 7.4. It is important to highlight that though PET based devices combusted in 33% quicker time (~8 s) compared to the paper based devices in our case (~12 s) due to the presence of non-flammable Ag bottom gate

conducting layer in paper devices, the mass of the paper devices significantly reduced after combustion compared to the plastic (PET) counterpart. A 75% reduction in mass of paper devices was observed, whereas the mass of PET based devices was reduced to 25% only highlighting the unsuitability of combustion as degradation of plastic based devices. The leftover residue of PET based devices was a rigid blackish substance, probably requiring other complex strategies for further degradation. This exploration indicates that paper based devices are excellent candidates for eventual biodegradation through time taking processes like decomposition as well as quick strategies like combustion. Our results confirm that paper based electronics can be a suitable alternative to plastic based flexible electronics for reduction of the overall carbon footprints in the environment.

7.4 CONCLUSION

Fully biodegradable organic transistors were demonstrated with a unique device structure using cellulose based substrate and gate dielectric, i.e. paper and CEC. These devices exhibited excellent p-channel characteristics for -5 V operation due to CEC acting as solid-state electrolyte gate. Comprehensive exploration of humidity exposure on device performance was investigated indicating decent stability of characteristics upon initial exposure, however, a degradation was observed upon extreme exposure with RH~100. High cyclic stability was observed before and after exposure to humidity with devices maintain the on/off current ratios for the entire duration measurements. Moreover, excellent bias-stress stability was achieved. High bendability of devices was confirmed upon application of tensile stress through bending along the channel for the bending radius of 12, 7, and 5 mm. The shelf-life measurements 7 weeks indicated that most of the degradation in the performance occurs in initial weeks followed by a decent stability in ambient. An improvement in the device performance was observed upon annealing at temperatures up to 60 °C, followed by reduction in performance upon further increase in annealing temperature up to 100 °C, indicating the suitability for operation of these devices for wearable electronics applications. Moreover, high biodegradability was demonstrated by the successful decomposition of the fabricated devices in the water rich soil within 19 days, due to the microorganisms present in soil environment. In addition, a simple combustion strategy was also performed to investigate the reduction in mass compared to typical plastic substrates. Due to high performance and biodegradability, these paper-based devices can offer huge potential towards the future flexible and green electronics, and can help in minimizing the impact of E-waste on environment and ecology.

...