6
Novel Observations on Jitter in Chain of CMOS Inverters

As an extension and application of the two different modeling techniques proposed in the earlier chapters, it provides novel observations and relevant implications at the system-level timing analysis. It is a transition from modeling at the driver level in previous chapters to a more complex multi-stage analysis. This chapter presents a comprehensive investigation and novel observations on the jitter behavior in chains of CMOS inverters, underscoring their practical significance. Building on the foundational work presented in [Illikkal *et al.*, 2022] and [Tripathi *et al.*, 2020], this study introduces fresh insights and notable findings. This study can be broadly applied across various subsystems and systems, thereby underscoring their practical significance.

6.1 Introduction

It is evident that the CMOS inverter has many applications as one of the basic building blocks and is used in almost every electronic subsystem; its timing uncertainty affects the performance of the system. There are many applications of the chain of inverters in high-speed VLSI systems, such as clock networks or as a delay line, input-output drivers, buffers, ring oscillators, etc [Razavi, 2024a], [Razavi, 2024b] [Tripathi *et al.*, 2019a] and [Chen *et al.*, 2003]. Hence, it is essential to model the timing uncertainty in the chain of CMOS inverters, which arises due to various noise sources. Several methods can be found in the literature to estimate the jitter for a chain of CMOS inverters, using analytical or semi-analytical approaches. The work in [Kim *et al.*, 2018] and [Kim *et al.*, 2017] presents an analytical approach based on piece-wise linear approximation of the I-V curve of transistors. It derives a PSIJ transfer function for a single CMOS inverter. Then the output of the inverter is linearly stacked to obtain the PSIJ transfer function for a chain of inverters. The work in [Chen *et al.*, 2003] presents an analysis of the impact of PSN and GBN on signal propagation through a buffer chain. Closed-form formulas are derived to estimate the corresponding change in delay. In [Wang and Kwasniewski, 2016], the analysis of jitter is done based on the propagation delay of the inverter. It derives PSN-based jitter sensitivity expression to estimate jitter at every stage in the chain. The study in [Tripathi *et al.*, 2019a] introduces a versatile approach to analyze power supply-induced jitter (PSIJ) in both Chains of CMOS inverters and tapered buffers having poor performance due to the presence of multiple deterministic noise sources. Using the Thomas algorithm, generalized semi-analytical relationships are derived to estimate PSIJ. This method can be used in scenarios involving uniform inverter sizes, tapered buffers, and the influence of both on-chip and off-chip interconnects. This work in [Sun *et al.*, 2020] presents a target impedance-based concept that establishes a relationship between output jitter of the circuit and

parameters of the power distribution network (PDN). The study analytically derives output jitter depending on PDN parameters by establishing a relationship between time domain voltage ripple and PDN parameters, defining target impedance curves for specific circuits. Multiple target impedance curves are defined using these relationships and given the transient switching current and jitter specifications. In [Illikkal *et al.*, 2022], a novel observation on jitter was reported considering only power supply noise source. It says that power supply-induced jitter does not necessarily increase with the number of inverter stages.

It was an intuitive belief that Total Intrinsic Error (TIE) accumulates progressively with the number of stages in a circuit, leading to a consistent increase in jitter [Kim *et al.*, 2018]. Later, it was demonstrated that this is not true and it will follow a constant zig-zag pattern [Illikkal *et al.*, 2022]. However, looking into these conventional understandings, this work aims to investigate to present a deeper and more comprehensive study on jitter in a chain of CMOS inverters. It uses a semi-analytical methodology to estimate jitter under the influence of power supply and ground noise. It is based on estimating the small-signal noise transfer function. It uses the slope-based method to model the jitter at the output of every inverter stage, which requires only one bit of simulation for jitter estimation, making it computationally efficient while delivering insightful results.

6.2 Effect of Noise on Jitter in a Chain of Inverters

The presence of any noise sources affects the output response of CMOS inverters, which can be reflected in the form of variations in the voltage of logic levels of the signal and variations in the transition edges of the signal. These effects may cause the rising and falling edges to shift from their ideal positions or transition at slower or faster rates. Overall, under the influence of noise, the performance of the CMOS inverter can become worse, which can further lead to the violation of the timings of the entire system. A schematic of the Chain of CMOS Inverters is depicted in Figure 6.2.1, with a load C_L, affected by supply noise (PSN: $v_{n_s}(t)$) and ground-bounce noise PSN: ($v_{n_g}(t)$). A holistic description of performance degradation because of the presence of noise is presented in Chapter-1. Since the circuit shown in Figure 6.2.1 consists of N number of CMOS inverters, while observing the pattern of jitter at every stage shows an interesting phenomenon that resembles the type of noise and its frequency, a detailed explanation is provided in the upcoming sections.

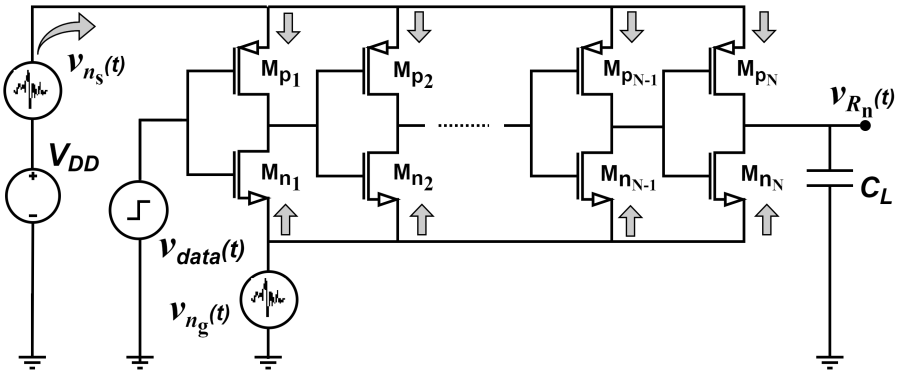


Figure 6.2.1: Chain of N CMOS Inverters.

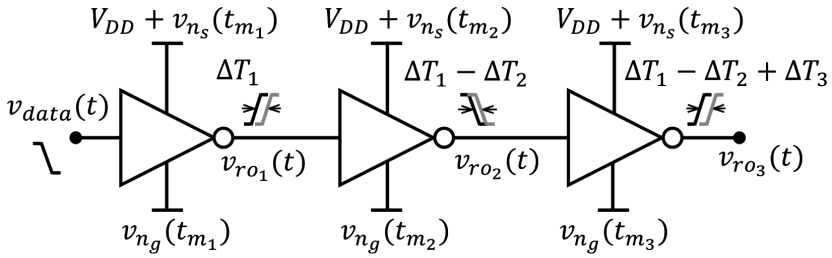


Figure 6.2.2: Chain of 3 CMOS Inverters.

6.2.1 Physical Insight of Jitter for Chain of CMOS Inverter

In this work, the slope-based method has been utilized to estimate the induced jitter at the output of every inverter stage [Tripathi *et al.*, 2020], [Tripathi *et al.*, 2017]. This method is based on the separation of large and small signal responses. The total response of the system ($v_{R_n}(t)$) is given as the sum of the large signal output response ($v_R(t)$) and small signal output response (i.e., noise response) ($v_{r_n}(t)$). The slope (α_N) of the output signal at the mid-point (t_m) of the transition edge is estimated when no noise is present in the circuit as

$$\alpha_N = \frac{d}{dt}\left(v_{R_N}(t)\right)\Big|_{t=t_m}. \tag{6.1}$$

Next, the time interval error (TIE) at the output in the presence of noise is estimated as

$$J_r = \frac{v_{r_n}(t_m)}{\alpha_N}, \tag{6.2}$$

where $v_{r_n}(t_m)$ is the small-signal output response of the inverter at the mid-point ($t = t_m$) of the rising/falling edge of the output. Figure 6.2.2 illustrates how the effect of noise in terms of jitter propagates from one stage to the next stage in the chain of inverters due to the noise present at the supply and ground terminals. Let us consider the falling edge of the input signal for the inverter chain, along with the different noise sources. With respect to the input transition edge, the corresponding rising/falling edge is shown at the output of every stage. The slope ($\alpha_{t_{m_1}}$) of the output at the first stage is positive at time instance (t_{m_1}) as it rises from level-low to level-high. Thus, assuming the noise response $v_{ro_1}(t_{m_1})$ to be positive, the TIE (J_{r_1}) at the output of the first stage will be positive, represented by ΔT_1 as:

$$J_{r_1} = \Delta T_1 = \frac{v_{ro_1}(t_{m_1})}{\alpha_{t_{m_1}}}. \tag{6.3}$$

After the timing instance of ($t_{m_2} - t_{m_1}$), the output response of second stage will be $v_{ro_2}(t_{m_2})$. Corresponding to the rising edge of the output response of the first stage, the output response of the second stage will have a negative slope ($-\alpha_{t_{m_2}}$). The TIE (J_{r_2}) will be negative because of the negative slope. Thus, the total TIE at the output of the second stage is estimated as:

$$J_{r_2} = \Delta T_1 - \Delta T_2, \tag{6.4}$$

where

$$-\Delta T_2 = -\frac{v_{ro_2}(t_{m_2})}{\alpha_{t_{m_2}}}. \tag{6.5}$$

From (6.4), it can be seen that the magnitude of TIE at the output of the second stage is reduced. Similarly, at the output of the third stage, because of the positive slope ($\alpha_{t_{m_3}}$) of the output response $v_{ro_3}(t_{m_3})$ the TIE (J_{r_3}) output will be positive. The total TIE at the output of the third inverter stage can be expressed as:

$$J_{r_3} = \Delta T_1 - \Delta T_2 + \Delta T_3 \tag{6.6}$$

where

$$\Delta T_3 = \frac{v_{ro_3}(t_{m_3})}{\alpha_{t_{m_3}}}. \tag{6.7}$$

From (6.6), it can be seen that the magnitude of the total TIE has increased at the output of the third stage. Similarly, the same pattern will be followed by jitter at all the successive stages.

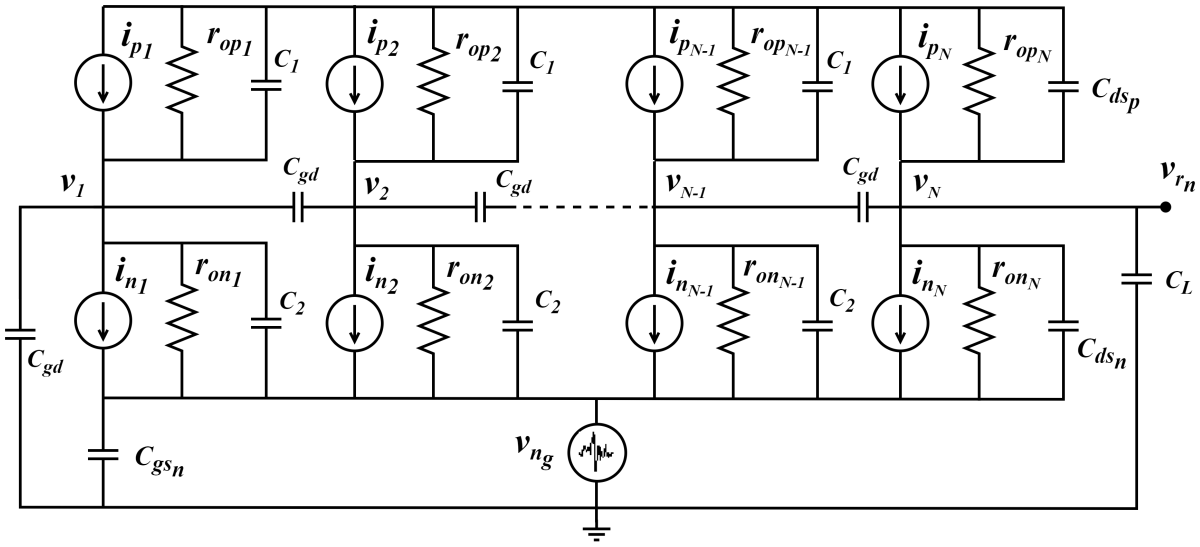


Figure 6.2.3: Small signal equivalent circuit of the inverter chain.

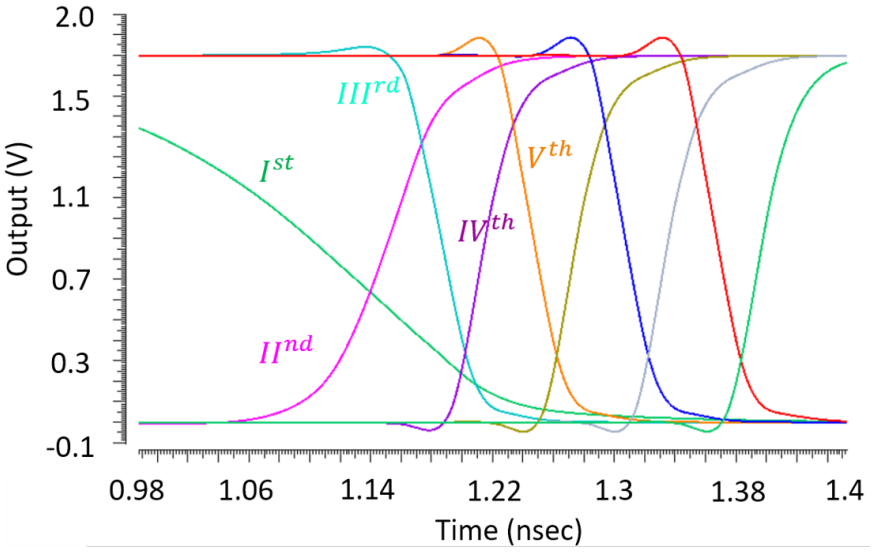


Figure 6.2.4: Output responses of each stage for a CMOS Inverter chain of 10 stages.

6.2.2 Output Response for a Chain of Inverters

For the development of the transfer function for the Nth inverter stage, N inverters of equal size are considered. The small-signal equivalent of the CMOS inverter chain having power supply and ground noise is shown in Figure 6.2.3. Here i_{p_N} (i.e., $g_{mp_N} v_{n_s}$), i_{n_N} (i.e., $-g_{mn_N} v_{n_g}$) are the small-signal current of pMOS and nMOS, respectively, and the respective small signal output resistance are r_{op_N} and r_{on_N}, for N^{th} inverter stage. C_1 is the sum of drain to source capacitance (C_{ds_p}) and gate to source capacitance (C_{gs_p}) of pMOS and C_2 is the sum of drain to source capacitance (C_{ds_n}) and gate to source capacitance (C_{gs_n}) of nMOS. First, the noise transfer function with respect to different noise sources for a single-stage and two-stage inverter chain is developed. Following this, the noise transfer function for N^{th} inverter stage has been derived. Here, a case of slow rising edge of the input signal is considered. In this case, both the transistors of single-stage inverter will conduct in saturation region at the mid-point ($V_{DD}/2$) of the output response [Bisdounis *et al.*, 1998]. Depending on the input rise/fall time and the sizing of the transistors at different stages of the inverter chain, the transistors will operate in different regions. In the case of the considered chain of inverters, for slow rising input signal, both the transistors (pMOS and nMOS) of the first and second stage inverter will conduct in saturation region at the mid-point of the output transition edge. As the output signal stabilizes, the transistors of all the other consecutive stages (from stage 3rd to all other stages) will conduct in an alternate manner and either (pMOS: saturation mode; nMOS: cutoff mode) or (pMOS: cutoff mode; nMOS: saturation mode). Figure 6.2.4 depicts the output response of inverter chain up to 10 stages in order to show the stabilization of the output response. It is observed that for the third stage, the nMOS is in saturation mode, and pMOS is in cutoff mode at the mid-point of the output transition edge. Here, the noise response will be mainly due to the ground noise (v_{n_g}). Similarly, for the fourth stage, pMOS will be in saturation mode, and nMOS will be in cutoff mode; here, noise response will be due to the supply noise (v_{n_s}).

The output responses ($v_{r_{n_s}}$ and $v_{r_{n_g}}$) of the Nth inverter stage with respect to PSN (v_{n_s}) and GBN (v_{n_g}), respectively are as:

$$v_{r_{n_s}} = \left(\sum_{i=1}^{N-1} \left(\frac{\chi_{N-i}}{X_N} \prod_{j=1}^{i} \frac{A_{N-j+1}}{X_{N-j}} \right) + \frac{\chi_N}{X_N} \right) v_{n_s}, \tag{6.8}$$

$$v_{r_{n_g}} = \left(\sum_{i=1}^{N-1} \left(\frac{B_{N-i}}{X_N} \prod_{j=1}^{i} \frac{A_{N-j+1}}{X_{N-j}} \right) + \frac{B_N}{X_N} \right) v_{n_g}, \tag{6.9}$$

where

$$A_i = j\omega C_{gd} - g_{mp_i} - g_{mn_i} \tag{6.10}$$

$$B_i = \begin{cases} j\omega C_2 + g_{on_i} + g_{mn_i}, & \text{if} \quad i \leq N-1 \\ j\omega C_{ds_n} + g_{on_i} + g_{mn_i}, & \text{if} \quad i = N \end{cases}, \tag{6.11}$$

$$\chi_i = \begin{cases} j\omega C_1 + g_{op_i} + g_{mp_i}, & \text{if} \quad i \leq N-1 \\ j\omega C_{ds_p} + g_{op_i} + g_{mp_i}, & \text{if} \quad i = N \end{cases}, \tag{6.12}$$

$$X_i = \begin{cases} j\omega C', & \text{if} \quad i = N = 1 \\ j\omega(2C_{gd} + C) + g_{o_i}, & \text{if} \quad i = 1, N > 1 \\ j\omega(2C_{gd} + C) + g_{o_i} - \frac{A_i j\omega C_{gd}}{X_{i-1}}, & \text{if} \quad i < 1 < N \\ j\omega C' + g_{o_i} - \frac{A_i j\omega C_{gd}}{X_{i-1}} & \text{if} \quad i = N > 1 \end{cases}, \tag{6.13}$$

$$g_{o_i} = g_{op_i} + g_{on_i}, \quad g_{op_i} = \frac{1}{r_{op_i}}, \quad g_{on_i} = \frac{1}{r_{on_i}}, \tag{6.14}$$

$$C = C_1 + C_2, \quad C' = C_{gd} + C_{ds_p} + C_{ds_n} + C_L. \tag{6.15}$$

Let M be the number of stages after which the rise/fall pattern of the transmitted input data signal stabilizes. The closed-loop expression for the ith stage can written as:

$$v'_{r_n} = \frac{\chi_i}{X'_i} v_{n_s} + \frac{B_i}{X'_i} v_{n_g} \tag{6.16}$$

where

$$X'_i = \begin{cases} j\omega(2C_{gd} + C) + g_{o_i}, & \text{if} \quad M < i < N \\ j\omega C' + g_{o_i}, & \text{if} \quad i = N \end{cases}. \tag{6.17}$$

A detailed derivation can be found in [Tripathi *et al.*, 2020].

6.2.3 Estimation of Jitter

To apply the slop-based method for a chain of inverters, as shown in Figure 6.2.1, the analysis is divided into two parts. First, the TIE for the first M stage is estimated using (6.2). Further, for the $(M+1)^{\text{th}}$ stage (till the input data signal is unstable and all the transistors are in saturation, as depicted in Figure 6.2.4), the TIE can be estimated as:

$$J_{r_{(M+1)}} = \frac{v'_{r_n(M+1)}}{\alpha_{(M+1)}} + J_{r_M} \tag{6.18}$$

using the similar procedure, the TIE for i^{th} stage can be written as:

$$J_{r_i} = \frac{v_{r_n(i)}}{\alpha_i} + J_{r_{(i-1)}}, \quad i > M \tag{6.19}$$

The output jitter for N^{th} stages can be written as:

$$J_N = max(J_{r_N}) - min(J_{r_N}) \tag{6.20}$$

6.3 Discussion of the Results

This section presents some simulations as well as experimental results, considering several examples. These examples validate the observations and demonstrate the physical significance of jitter at various stages of the inverter chain, shown in Figure 6.2.1. For the analysis of jitter, the power supply and ground bounce noise are considered.

6.3.1 Analytical Results

In this section, the analytical results are compared with the simulation results to validate the proposed method. The simulation results are obtained using the SPIC-based simulator. The analytical results are obtained using MATLAB. First, the chain of inverters is designed using a 180 nm CMOS technology node of United Microelectronic Corporation (UMC) with 10 equal-sized inverters; after this, the number of stages in the chain has been increased to 150. A power

supply of 1.8 V is applied to the inverter chain. A slow input data signal having a data rate of 240 Mbps is considered.

Example-1:

In this example, only PSN source with amplitude of 40 mV and frequency of 533 MHz is considered. Figure 6.3.1 depicts the output jitter at each inverter stage.

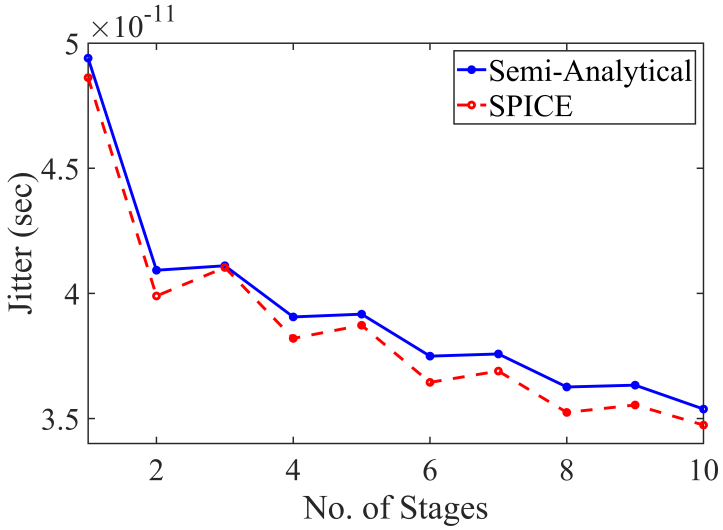


Figure 6.3.1: Jitter pattern with different stages in the chain of inverters in the presence of PSN estimated at two different frequencies of noise.

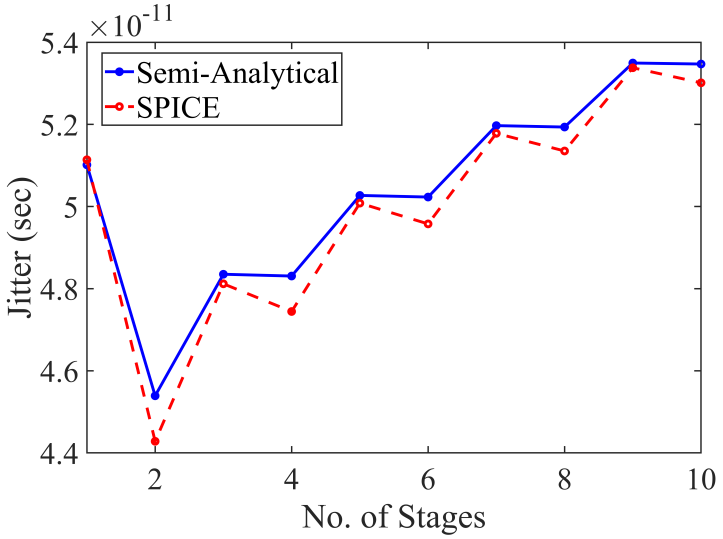


Figure 6.3.2: Jitter pattern with different stages in the chain of inverters in the presence of GBN estimated at two different frequencies of noise.

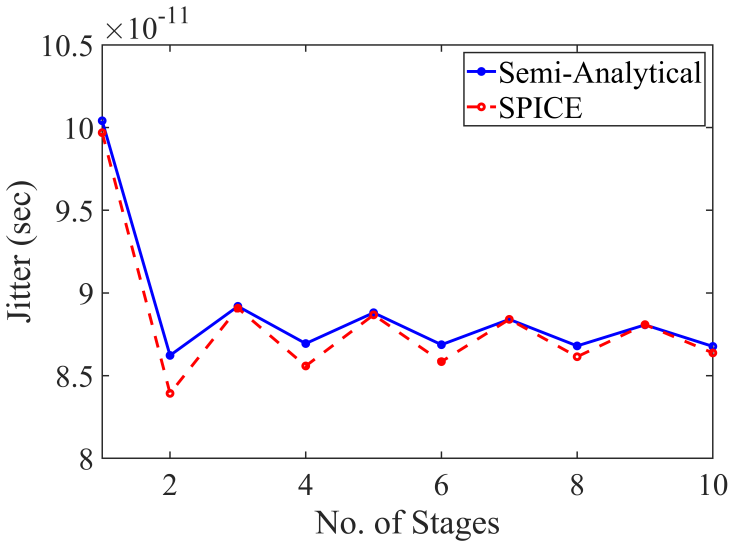


Figure 6.3.3: Jitter pattern with different stages in the chain of inverters in the presence of GBN estimated at two different frequencies of noise.

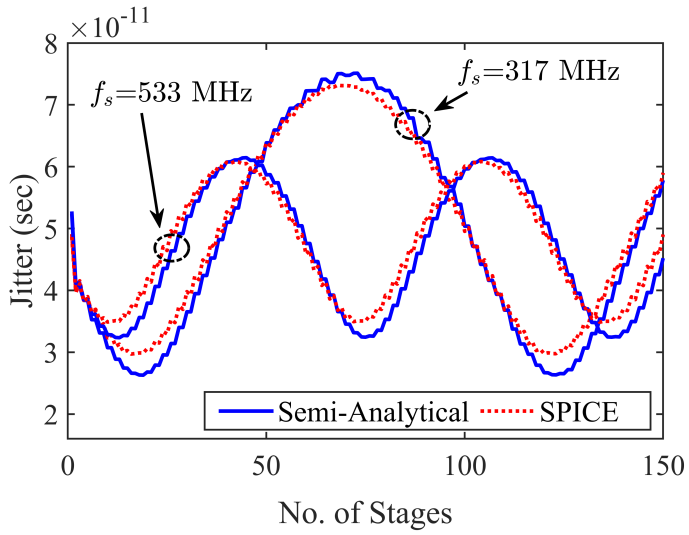


Figure 6.3.4: Jitter pattern with different stages in the chain of inverters in the presence of PSN estimated at two different frequencies of noise.

Example-2:

In this example, both PSN and GBN sources, having the same amplitude and frequency of 40 mV and 533 MHz, respectively, are considered. Figure 6.3.2 depicts the output jitter at each inverter stage.

Example-3:

In this example, only GBN source with amplitude of 40 mV and frequency of 533 MHz is considered. Figure 6.3.3 depicts the output jitter at each inverter stage.

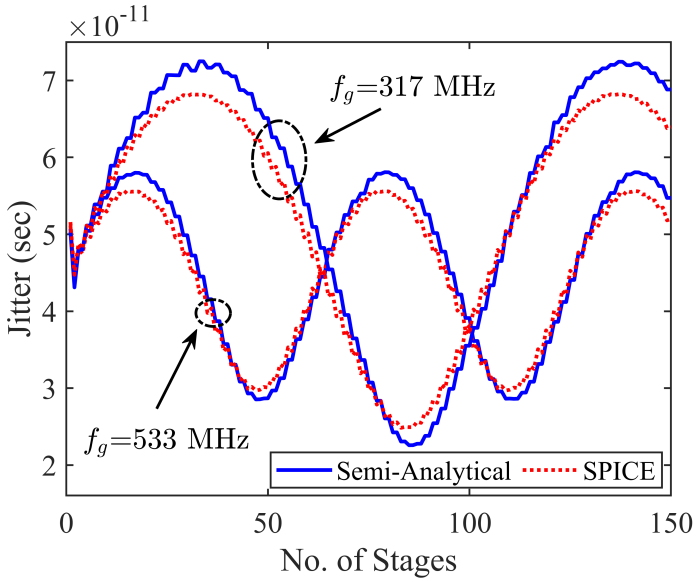


Figure 6.3.5: Jitter pattern with different stages in the chain of inverters in the presence of GBN estimated at two different frequencies of noise.

Example-4:

In this example, only PSN with amplitude of 40 mV. Figure 6.3.4 depicts the output jitter at each inverter stage. Jitter values are estimated considering two different frequencies of noise 317 MHz and 533 MHz.

Example-5:

In this example, only GBN with amplitude of 40 mV is used. Figure 6.3.5 depicts the output jitter at each inverter stage. Jitter values are estimated considering two different frequencies of noise 317 MHz and 533 MHz.

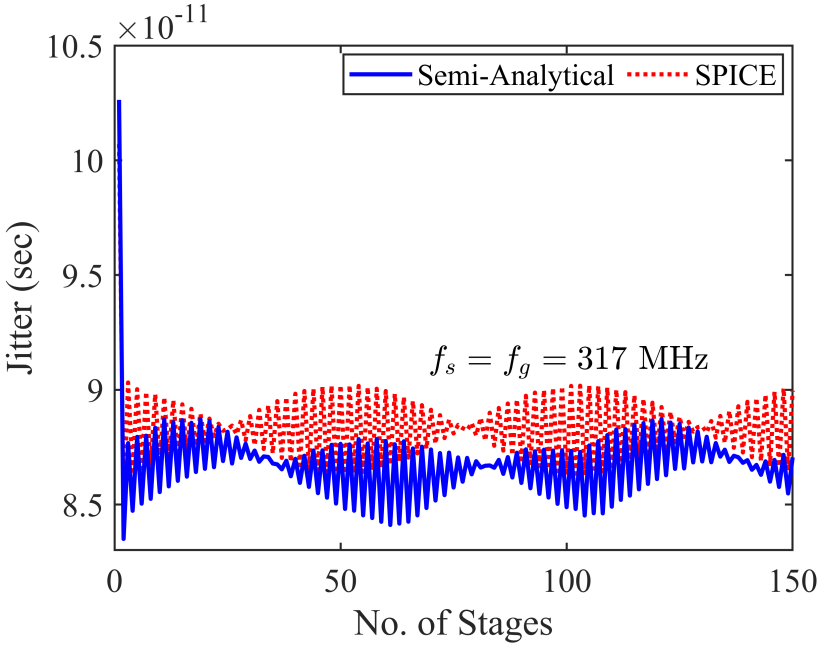
Example-6:

In this example, both PSN and GBN are considered. Both noise sources have the same amplitude (40 mV) and the same frequency. Jitter values are estimated considering two different frequencies of noise 317 MHz and 533 MHz. Figure 6.3.6 depicts the output jitter at each inverter stage.

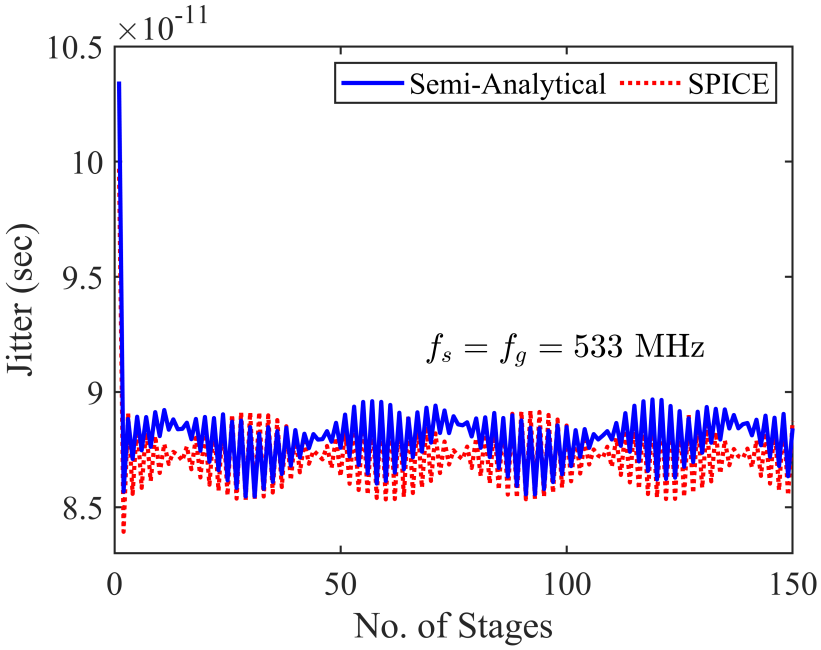
It follows a zig-zag sinusoidal pattern, similar to the sinusoidal noise, and at higher frequencies of noise, it completes more cycles. Jitter is found to be less at high-frequency noise as compared to low-frequency noise.

6.3.2 Experimental Setup and Measurement Results

For the experiment purpose, a similar type of connection has been prepared, as shown in Figure 6.3.7. An experimental setup was prepared using hex inverter ICs (SN74HC04N from Texas Instruments). The inverter chain is designed with 100 same-sized inverter stages using these ICs. Figure 6.3.8 depicts the measurement setup used.



(a)



(b)

Figure 6.3.6: Jitter pattern with different stages in the chain of inverters in the presence of PSN and GBN, estimated at two different frequencies of noise (a) for $f_s = f_g = 317$ MHz and (b) for $f_s = f_g = 533$ MHz.

A DC power supply of 5 volts is applied using a regulated power supply EDU36311A by Keysight. The input data signal, having a frequency of 3 MHz, is applied using a function generator DDS300 (300 MHz dual channel) by Aplab. The power supply noise is generated as a si-

nusoidal having peak-to-peak amplitude of 500 mV and frequency of 4.317 MHz, using function generator AFG3021B (single channel) by Tektronix. The ground noise is generated as a sinusoidal with a peak-to-peak amplitude of 500 mV and frequency of 4.317 MHz using function generator DDS300 (from the second channel).

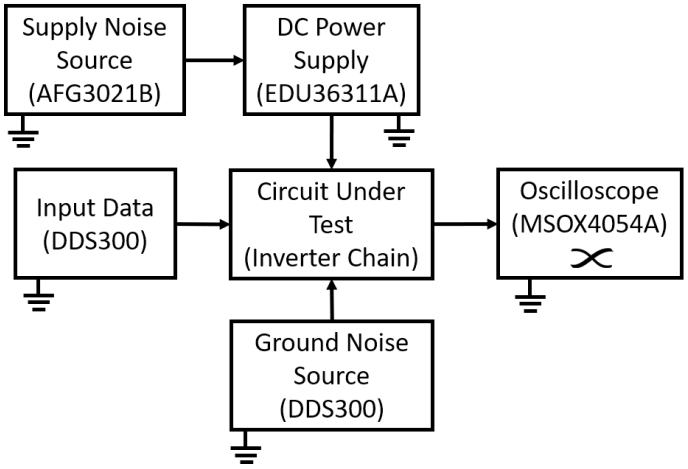


Figure 6.3.7: Block diagram representation of the measurement setup

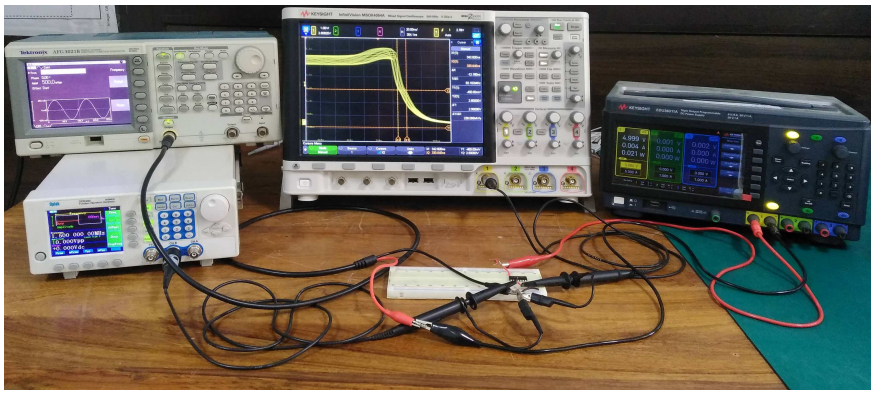


Figure 6.3.8: Photograph of measurement setup.

Example-7:

The inverter chain is designed with 10 same-sized inverter stages using the ICs. A DC power supply of 5 Volt is applied using a regulated power supply. The input data signal, having a frequency of 1.5 MHz, is generated. The power supply noise is generated as a sinusoidal having peak-to-peak amplitude of 500 mV and frequency of 4.317 MHz applied at the supply terminal along with DC power source. And the ground noise is generated as a sinusoidal with peak-to-peak amplitude of 500 mV and frequency of 4.317 MHz and applied at the ground terminal. Figure 6.3.9(a) and 6.3.9(b) represent the jitter obtained at each stage of the inverter chain constructed using hex-inverter IC STM74HC04 and SN74HC04N, respectively.

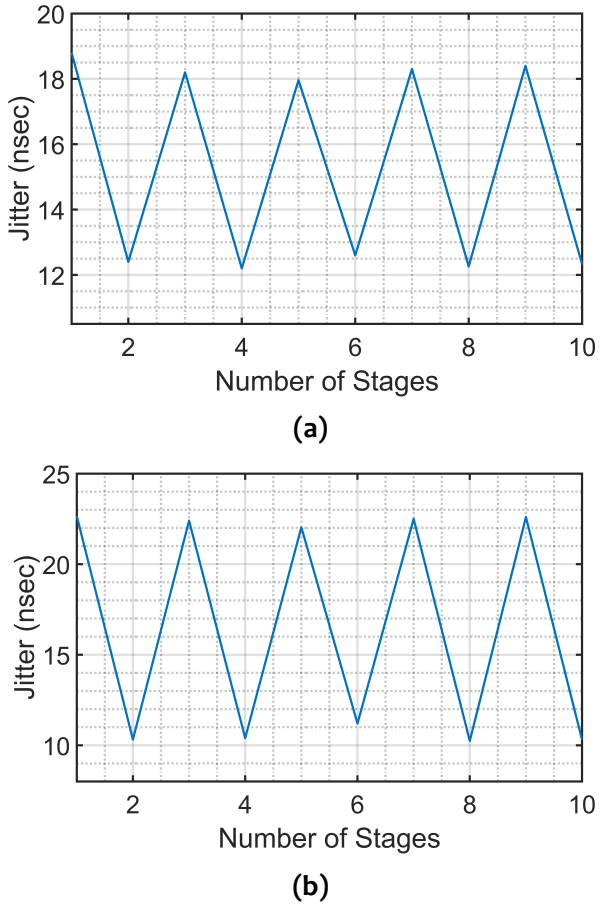


Figure 6.3.9: Jitter at different stages of inverter chain with IC (a) STM74HC04, and (b) SN74HC04N.

6.4 Summary

The effect of power supply and ground-bounce noise on the output response of a chain of CMOS inverters is analyzed, highlighting several observations. The slope-based method is used to estimate jitter at the output of every inverter stage in the chain. It is observed that the total estimated jitter exhibits a zig-zag pattern with the number of stages. When only one noise source, either PSN or GBN, is present in the circuit, this pattern resembles an increasing or decreasing staircase-like trend as the number of stages increases. However, when PSN and GBN are simultaneously present, the jitter maintains a uniform zig-zag pattern across stages. These observations are validated by comparing the results obtained from the semi-analytical approach and EDA tool, as well as the measurement setup. The proposed method is proved to be accurate and efficient, as it requires only one-bit simulation in the absence of noise. In contrast, the conventional method (using the SPICE-based simulator) requires simulation of hundreds of bits to estimate it. A significant speed-up in jitter estimation time is reported using the proposed method over EDA simulator. The proposed method may also apply to various noise sources and device technologies. This work not only redefines the understanding of jitter behavior in high-speed circuits but also offers a practical and efficient framework for its estimation, paving the way for enhanced design and optimization of VLSI systems.