4
SICL Based Amplifier Circuit

4.1 INTRODUCTION

An amplifier circuit is an essential component in modern RF front end systems, designed to amplify weak signals over a broad frequency range while minimizing noise and distortion. The architecture typically involves a combination of active devices, such as transistors (e.g., GaAs or GaN FETs), and passive components, including capacitors, and transmission lines. These elements are carefully configured to achieve optimal gain, bandwidth, linearity and stability. The active device in an amplifier is usually biased using a DC bias network to ensure proper operation within its linear region. Stability is a critical consideration in amplifier design, requiring techniques such as resistive loading, feedback networks, and stabilization circuits to prevent unwanted oscillations. The amplifier's gain is optimized through the use of matching networks and feedback loops, ensuring consistent performance across the frequency range. Impedance matching networks are employed at both the input and output end to minimize signal reflections and maximize power transfer. For high-frequency applications, high linearity is also important, especially in communication systems where signal distortion must be minimized. Bias optimization and linearization networks are commonly employed to maintain linearity across the amplifier's operating range. These networks often incorporate microstrip transmission lines, along with capacitors and inductors. Many circuit designers have adopted SIW and microstrip technology for the amplifier circuit [Eom and Lee, 2017],[Sabzi *et al.*, 2020b],[Othman *et al.*, 2007],[A and S, 2008]. However, SIW-based structures occupy a large area and they cannot be directly connected with any SMD components since it is a single conductor line. For the integration of the components, SIW requires a transition with microstrip lines which are prone to surface waves and radiation losses at millimeter wave frequencies. Moreover, some of the authors have reported the amplifier circuit based on CMOS technology but they adopted specialized fabrication techniques which is a costly procedure [Cruz *et al.*, 2015],[Cao *et al.*, 2008]. Here, SICL technology has been adopted which is the most favorable technology for low-cost PCB technique and helps to realize low-profile self-shielded lines at millimeter wave frequencies as discussed in chapter 1 [Gatti *et al.*, 2006]. [Baghel and Mukherjee, 2020], [Krishna and Mukherjee, 2021], [Liu *et al.*, 2013] [Shukla and Mukherjee, 2019],[Shukla and Mukherjee, 2023],[Krishna and Mukherjee, 2018b].

The main aim is to design a high gain amplifier with the help of mounting pads for the integration of a transistor, capacitors and a stepped impedance matching network in SICL environment at 24 GHz. In this chapter, a SICL-based single-stage amplifier circuit is designed using Taconic TLY-5 substrate which has low loss tangent ($\tan\delta = 0.0009$), and low cost (U.S. dollar 0.035 per square centimeter).

Figure 4.1 shows the 3-D view of the proposed amplifier, where the top and bottom conductors behave as a ground plane, the inner conductor as the middle strip representing the RF path along two side strips representing via pads. In addition, the mounting pads are introduced on the top conductor layer. As shown in Figure 4.2, the circuit consists of several elementary blocks such as SICL to GCPW transition, matching networks, and a 2-Port active device including a DC

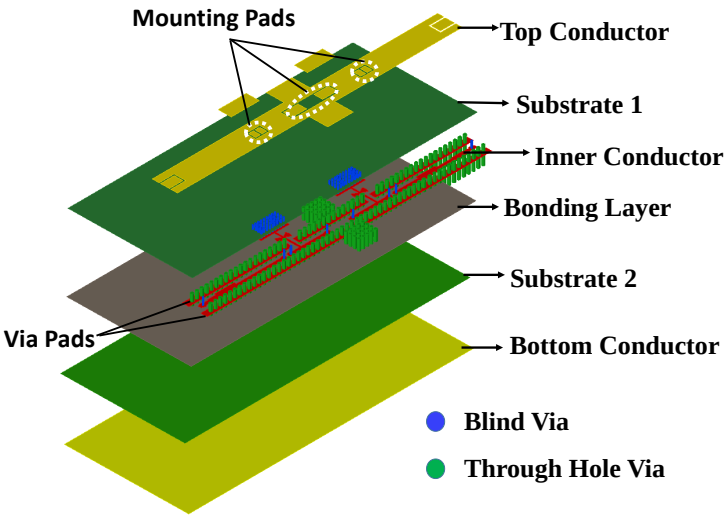


Figure 4.1 : 3-D view of the proposed amplifier.

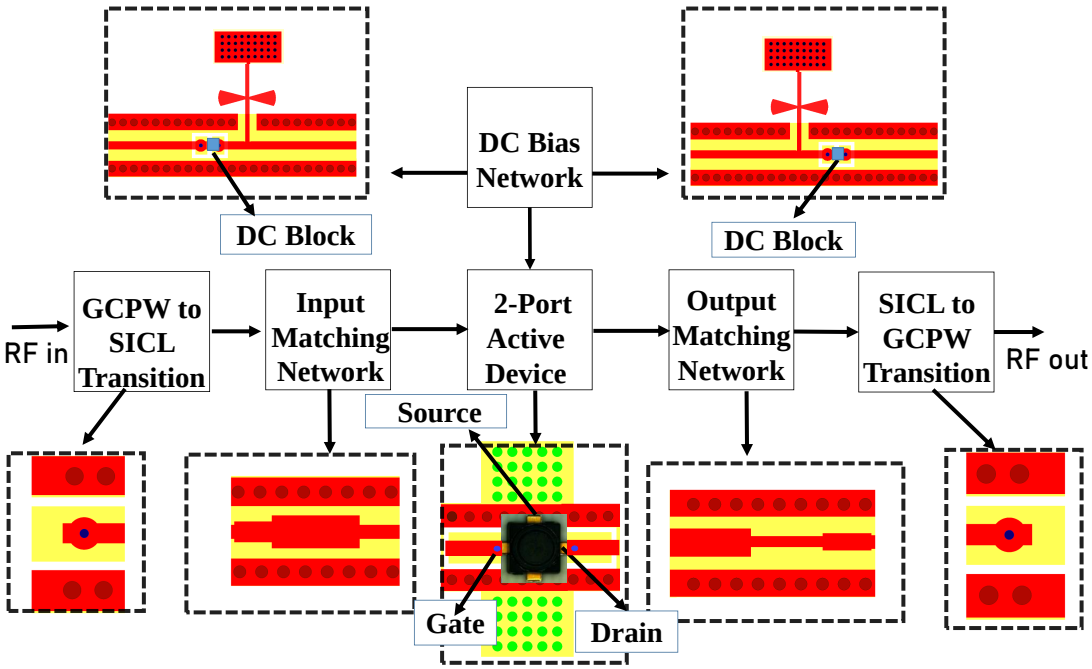


Figure 4.2 : Block diagram of the proposed amplifier circuit.

bias network.

The details of the design procedure for the proposed amplifier is shown in Section 4.2 . The results and discussion of the amplifier circuit are presented in Section 4.3.

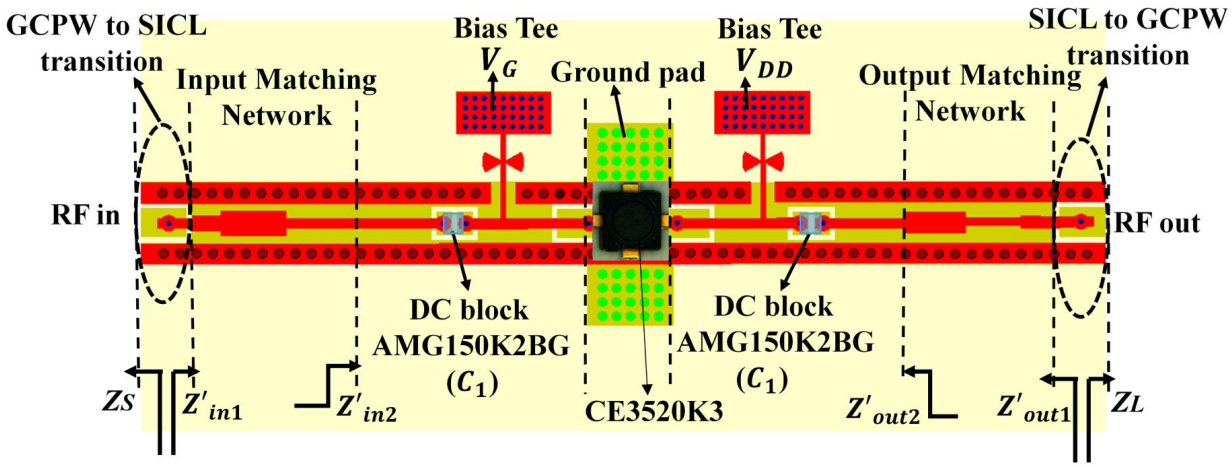


Figure 4.3 : Physical layout of the proposed amplifier circuit.

4.2 DESIGN PROCEDURE OF PROPOSED AMPLIFIER CIRCUIT

As shown in Figure 4.3, the proposed amplifier circuit is designed with two 0.25 mm thick Taconic TLY-5 (laminate) (ε_r=2.2, tanδ = 0.0009) based substrate along with bond layer Taconic FR28 prepreg (ε_r = 2.8, tanδ = 0.0014). It is realized with single-stage common source (CS) topology. In this circuit, the California Eastern Laboratories (CEL's) CE3520K3 GaAs FET transistor is used.

4.2.1 Description and DC Analysis of CE3520K3

The CE3520K3 model represents a non-linear, noise-inclusive model specifically designed for the Micro-X package pHEMT transistor, following the Angelov model extraction methodology. It is tailored for microstrip applications, primarily targeting amplifier designs [Modelithics, 2017]. The model has been optimized for operation at 2V and 10 mA and has undergone validation with Taconic TLY substrate, including 20 mil height, at high frequencies of up to 26 GHz as discussed in chapter 1. The technical features of the CE3520K3 model as given below:

Technical Features:

- **Substrate Considerations:** The model was validated on substrates with a dielectric constant ε_r = 2.2 and height H = 20 mil using microstrip technology.
- **Operational Parameters:**
  1. **Temperature:** The model is validated across a backside ambient temperature range of 25°C to 85°C.
  2. **Substrate Thickness (H):** Adjustable between 4 and 30 mils.
  3. **Dielectric Constant (ε_r):** Ranges from 2 to 10.

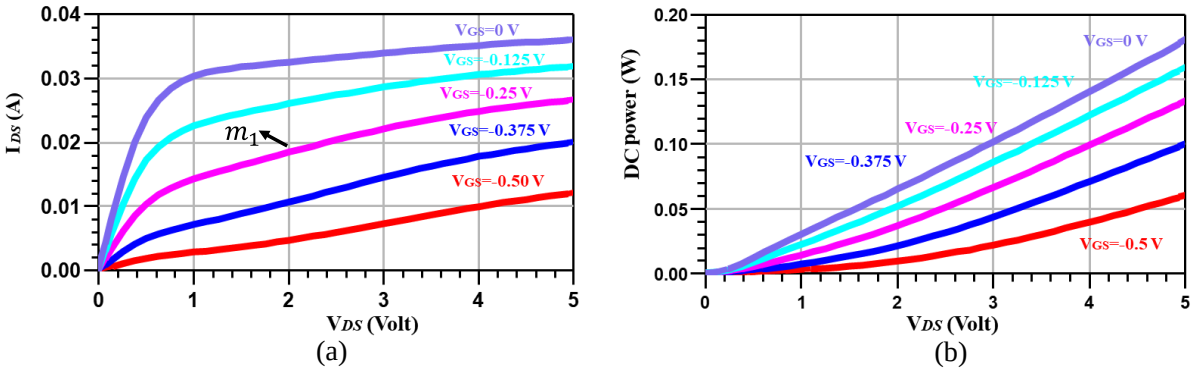


Figure 4.4 : (a) I-V characteristics of CE3520K3; (b) Response of DC power.

4. **Interconnect Metal Thickness:** Set to 1.7 mil.

5. **Loss Tangent (tanδ):** The default value is 0.003.

The model was thoroughly validated with through measurements in the 0.5 to 24 GHz range, using a common-source configuration. It includes considerations for package-related effects, providing a comprehensive and reliable simulation environment for amplifier designs in the higher frequency applications [Laboratories, CEL].

The CE3520K3 transistor model is selected for the SICL based amplifier circuit at 24 GHz. Figures 4.4(a) and 4.4(b) show the simulated I-V curve and DC power dissipation graph of the transistor model CE3520K3 in ADS where the simulated operating voltage of the transistor is chosen at m_1 which denotes $V_{DS} = 2$V, $V_{GS} = -0.25$ V and $I_{DS} = 18$mA and DC power dissipation is around 0.03 W.

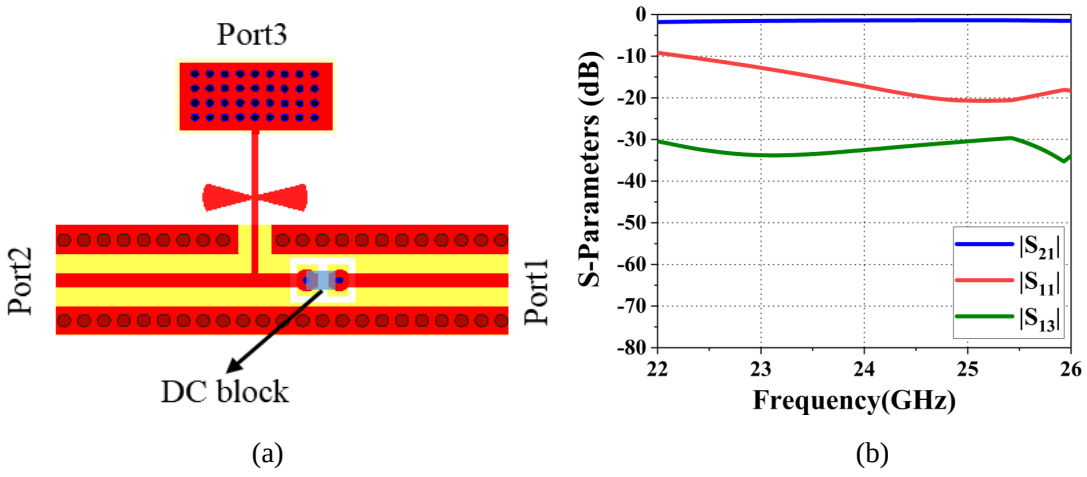


Figure 4.5 : (a) Physical layout of bias tee;(b) Response of DC bias tee circuit.

4.2.2 Design of DC bias circuit

The proposed DC bias circuit uses a butterfly stub with a quarter-wavelength high-impedance transmission line as RF choke in the DC circuit. Due to the parasitic capacitance effect of the lumped inductor, it is difficult to realize the RF chokes at higher frequencies. In the proposed circuit, the placement of the butterfly stub at the middle layer of the embedded microstrip structure eliminates the possible chance of spurious radiation. It also increases the isolation between Port 1(RF) and Port 3 (DC). Further, single-layer ceramic capacitors (DC blocks) are integrated into mounting pads, which are introduced on the top layer of the SICL line. Figure 4.5(a) and 4.5(b) shows the physical layout of bias tee and its response, where the butterfly structure with a quarter-wave high-impedance transmission line plays an important role in blocking the RF signal from Port 1 and 3 in the frequency range of 22-26 GHz.

4.2.3 Stability Analysis

In a two-port network as shown in Figure 4.6, stability is measured using parameters k and $|\triangle|$ which are defined as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\triangle|^2}{2\,|S_{12}S_{21}|} \tag{4.1}$$

where

$$|\triangle| = |S_{11}S_{22} - S_{12}S_{21}| \tag{4.2}$$

and

For unconditional stability of the transistor, k must be greater than 1, and $|\triangle|$ must be less than 1 [Pozar, 2011]. At 24 GHz, we verified Eq.(4.1)- (4.2) using the S-parameters value of the two-port network and obtained the value of k and $|\triangle|$ as 1.8 and 0.2, respectively. With the help of equations, K, and $|\triangle|$ graph are plotted as shown in Figure 4.7 which has clarified that the proposed network is unconditionally stable at the frequency band of DC-26 GHz.

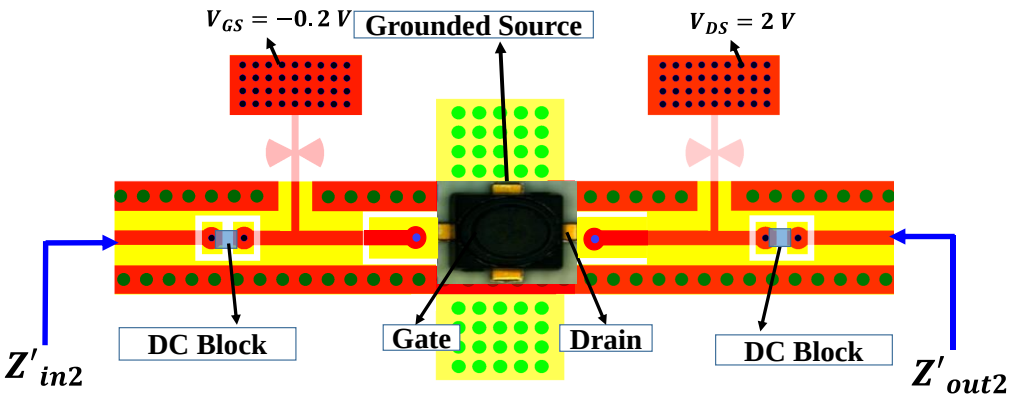


Figure 4.6 : Physical layout of two-port network for stability check.

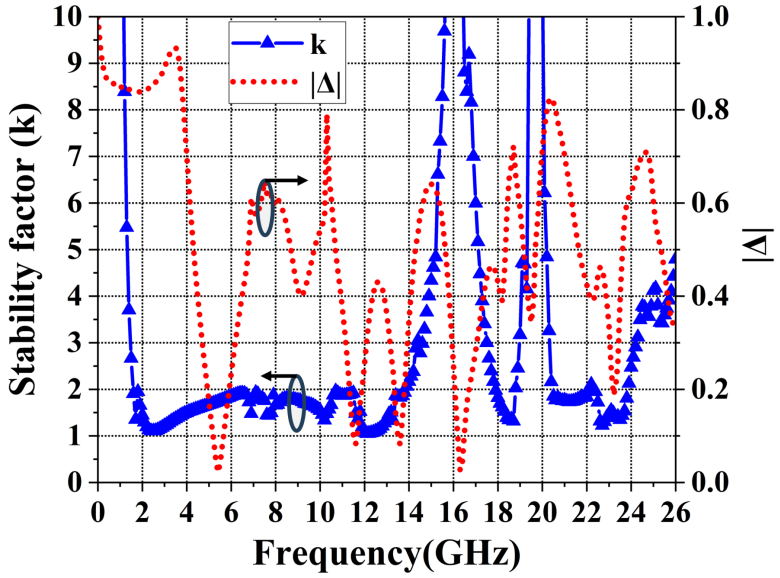


Figure 4.7 : Response of Stability factor (k) and (|△|.

Table 4.1 : Parameters of input and output impedance's through de-embedding technique

Parameter	Value
Z'_{in1}	≈ 50 Ω
Z'_{in2}	31+j*39 Ω
Z'_{out1}	≈ 50 Ω
Z'_{out2}	9-j*0.915 Ω

4.2.4 Design of matching networks

1. **Design and Analysis of input matching network**

With the help of de-embedding techniques, the input impedance (Z'_{in2}) of the 2-Port network (bias tee and transistor) as shown in Figure 4.6, are extracted in ADS which is shown in Table 4.1. In the amplifier circuit, a stepped impedance matching network has been introduced in the SICL environment. This networks need to be designed for better impedance matching with gain enhancement of the amplifier circuit at higher frequencies. For the design of the proposed input matching network, the ideal transmission line (ITL) matching network (MN) design is followed as shown in Figure 4.8 [Steer, 2019].

$$\Gamma'_{in2} = \frac{Z'_{in2} - Z_{03}}{Z'_{in2} + Z_{03}} \tag{4.3}$$

$$\Gamma_2 = \frac{Z_2 - Z_{02}}{Z_1 + Z_{02}} \tag{4.4}$$

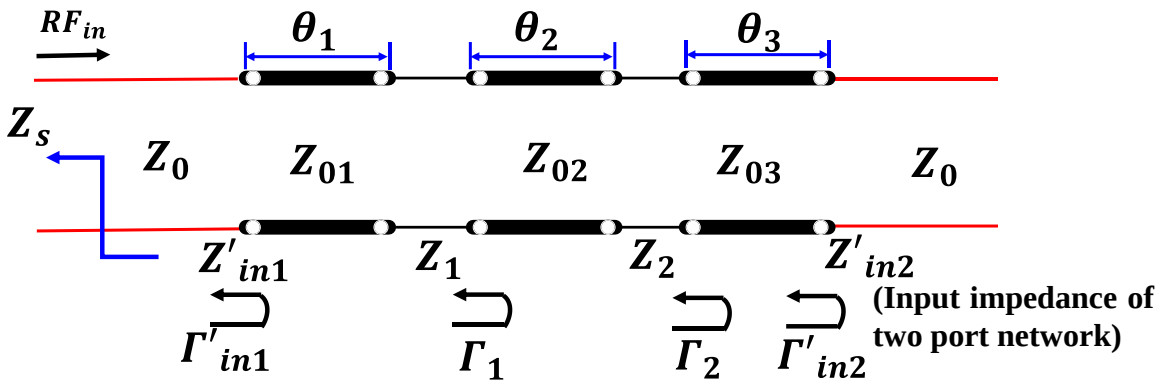


Figure 4.8 : Equivalent ideal transmission line (ITL) of input matching network.

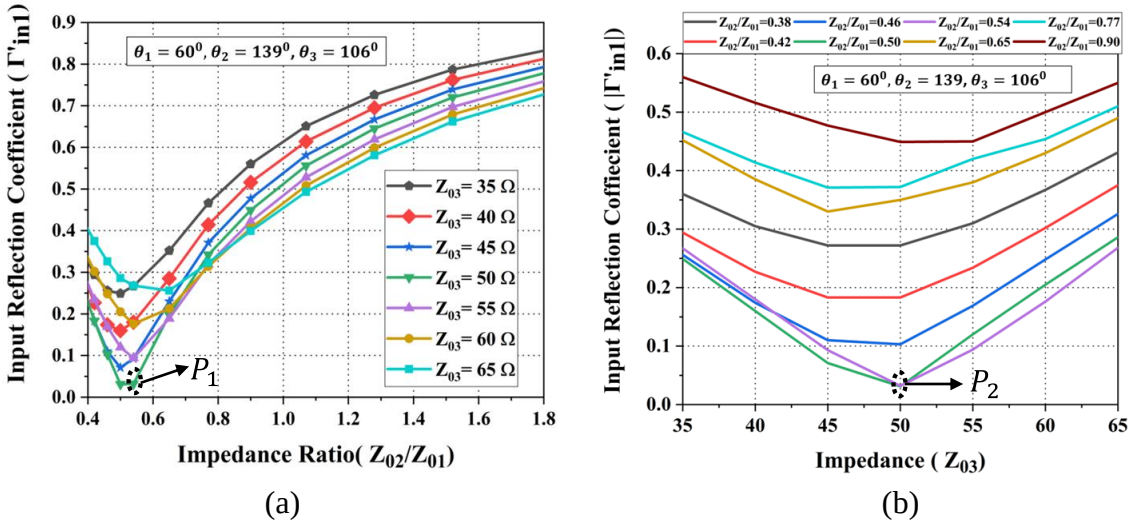


Figure 4.9 : (a) Response of input reflection coefficient with impedance ratio (Z_{02}/Z_{01}); (b) Response of input reflection coefficient with impedance (Z_{03}).

$$\Gamma_1 = \frac{Z_1 - Z_{01}}{Z_1 + Z_{01}} \tag{4.5}$$

$$\Gamma'_{in1} = \frac{Z'_{in1} - Z_0}{Z'_{in1} + Z_0} \tag{4.6}$$

Eq.(4.3)-(4.5) show the reflection coefficients for the three stepped impedance sections of Z_{03}, Z_{02}, and Z_{01} with their input impedance of Z_2, Z_1, and Z'_{in1}, respectively. The net input reflection coefficient (Γ'_{in1}) seen from the input is as follows in Eq.(4.6). With the help of Eq.(4.3)-(4.6), the graph between the net input reflection coefficient (Γ'_{in1}) and impedance

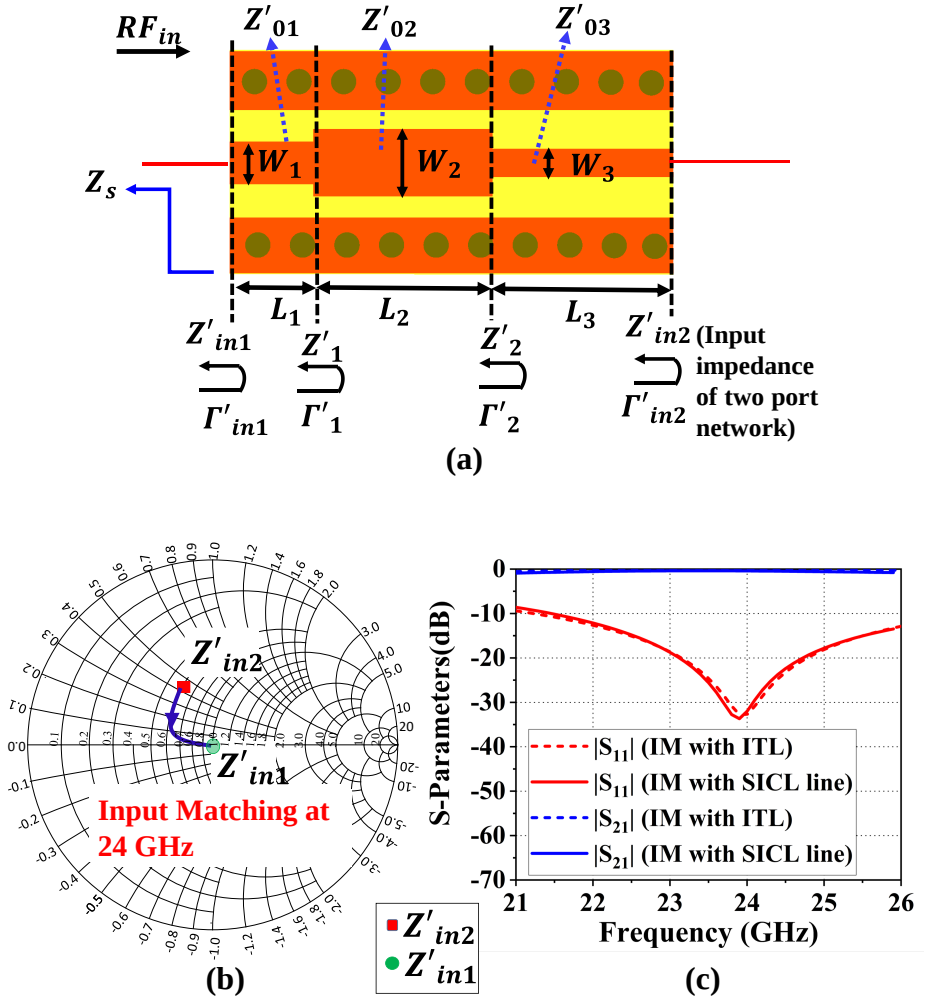


Figure 4.10 : Illustration of input matching network; (a) Physical layout with SICL line dimensions of $W_1 = 0.67$ mm, $W_2 = 1.07$ mm, $W_3 = 0.45$ mm, $L_1 = 1.2$ mm, $L_2 = 2.8$ mm, $L_3 = 2.83$ mm; (b) Impedance transformation with smith chart (c) Response of equivalent ideal transmission line (ITL) based input matching and SICL based input matching network.

ratios (Z_{02}/Z_{01}) with different specific impedance values of Z_{03} are plotted as shown in Figure 4.9(a). Next, the graph has been plotted between the net input reflection coefficient (Γ'_{in1}) and impedance (Z_{03}) with varying impedance ratios (Z_{02}/Z_{01}) using ADS software and MATLAB as shown in Figure 4.9(b).

The optimized values of the stepped impedance are chosen such as Z'_{01} = 34 Ω, Z'_{02}= 19 Ω and Z'_{03} = 54 Ω by the optimum points P_1 and P_2 as shown in Figure 4.9 (a) and (b). Its inner conductor line width and length with the dimensions of W_1, W_2, W_3, L_1, L_2, L_3 are shown in Figure 4.10(a) which have been optimized to match the performance of each section with the ideal transmission line (ITL) input matching network. The proposed input matching network shows the impedance transformation from Z'_{in2} to Z'_{in1} using the three-stepped impedance section of SICL lines on the Smith chart as shown in Figure 4.10(b). Figure 4.10(c) shows the good agreement of the simulated results between both the input matching (IM) networks.

2. **Design and Analysis of output matching network**

In a similar manner, using de-embedding techniques, the output impedance (Z'_{out2}) of the

2-port network is extracted in ADS, as presented in Table 4.1. A stepped impedance output matching network is implemented within the SICL environment in the amplifier circuit. These networks are designed to achieve improved impedance matching and to enhance the gain of the amplifier circuit at higher frequencies. The design process for the proposed output matching network follows the ideal transmission line (ITL) matching network approach, as illustrated in Figure 4.11 [Steer, 2019].

$$\Gamma'_{out2} = \frac{Z'_{out2} - Z_0}{Z'_{out2} + Z_0} \tag{4.7}$$

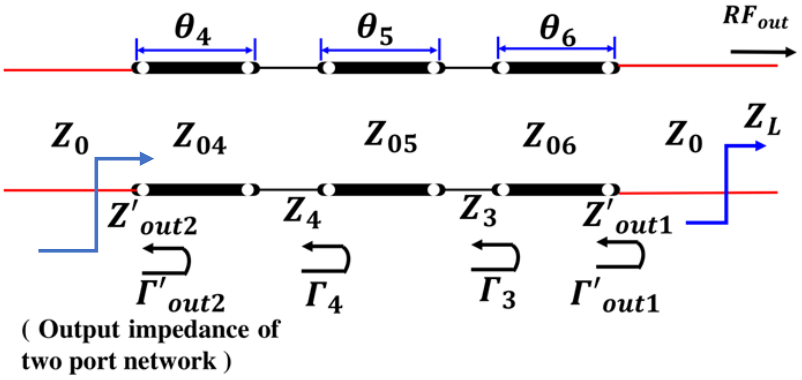


Figure 4.11 : Equivalent ideal transmission line (ITL) of output matching network.

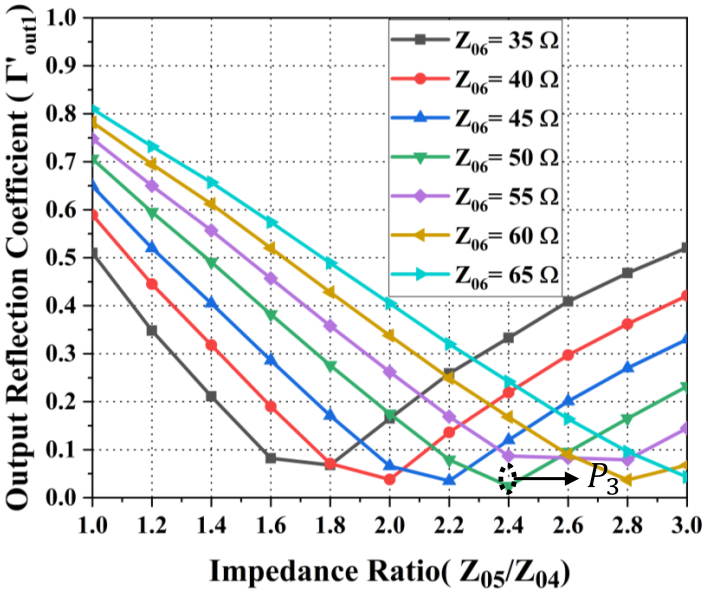


Figure 4.12 : Response of output reflection coefficient with impedance ratio (Z_{05}/Z_{04}).

$$\Gamma_4 = \frac{Z_4 - Z_{04}}{Z_4 + Z_{04}} \tag{4.8}$$

$$\Gamma_3 = \frac{Z_3 - Z_{05}}{Z_3 + Z_{05}} \tag{4.9}$$

$$\Gamma'_{out1} = \frac{Z'_{out1} - Z_{06}}{Z'_{out1} + Z_{06}} \tag{4.10}$$

The SICL-based output matching network is realized with the help of plots as shown in Figure 4.12. The optimized values of the stepped impedance are chosen such as $Z'_{04} = 26\ \Omega$, Z'_{05}=

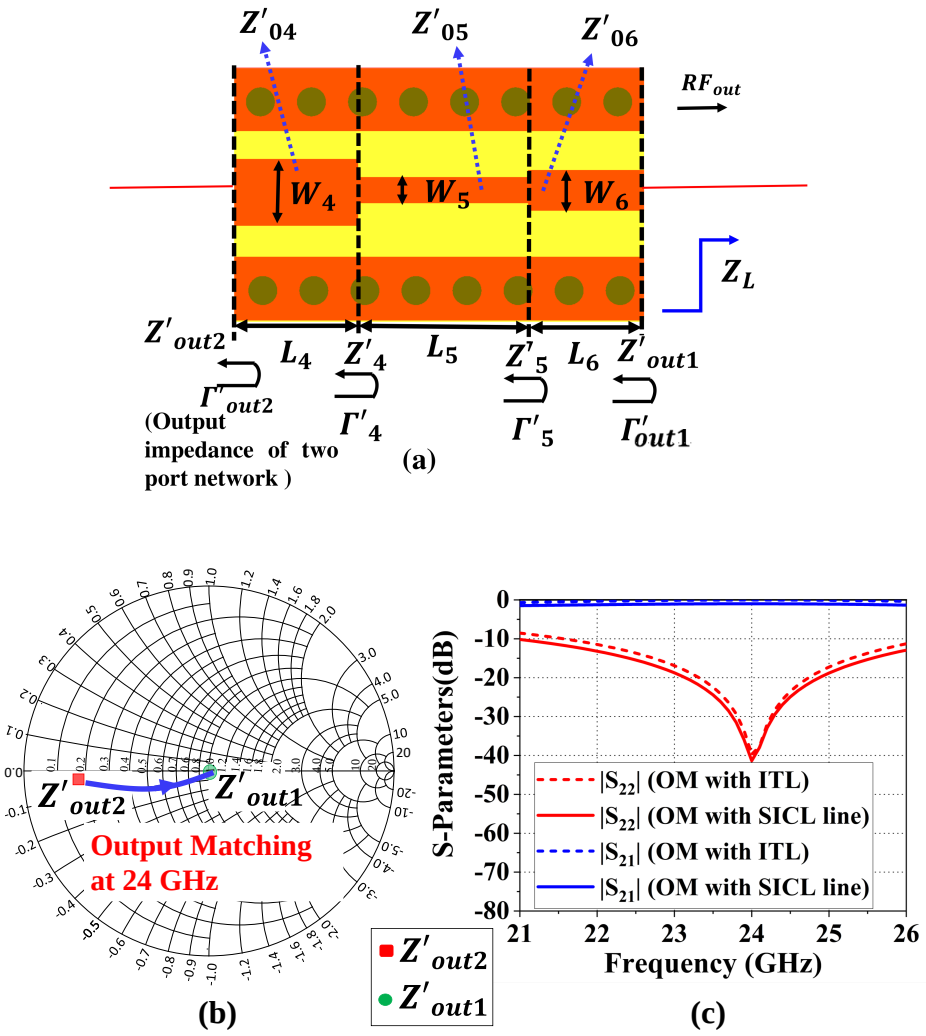


Figure 4.13 : Illustration of output matching network;(a) Physical layout with SICL line dimensions of $W_4 = 0.91$ mm, $W_5 = 0.35$ mm, $W_6 = 0.57$ mm, $L_4 = 1.74$ mm, $L_5 = 2.34$ mm, $L_6 = 1.6$ mm; (c) Impedance transformation with smith chart.

56 Ω and Z'_{06} = 39 Ω by the optimum point P_3. The optimized dimensions of the proposed output matching (OM) network are W_4, W_5, W_6, L_4, L_5, L_6 as shown in Figure 4.13(a). The proposed output network shows the impedance transformation from Z'_{out2} to Z'_{out1} with the help of three stepped impedance in SICL lines as shown in Figure 4.13(b) and its performance with ideal transmission line(ITL) output matching (OM) network as shown in Figure 4.13(c).

4.3 RESULTS AND DISCUSSION

Figure 4.14 (a) and 4.14(b) show the fabricated prototypes of the amplifier circuit. The proposed amplifier circuit has been developed with a SICL -to-GCPW transition, which is applied on both ports for edge mount connector interfaces. Figure 4.15(a) depicts the simulated results of small signal gain ($|S_{21}|$), input and output return losses between RFin and RFout with the operating

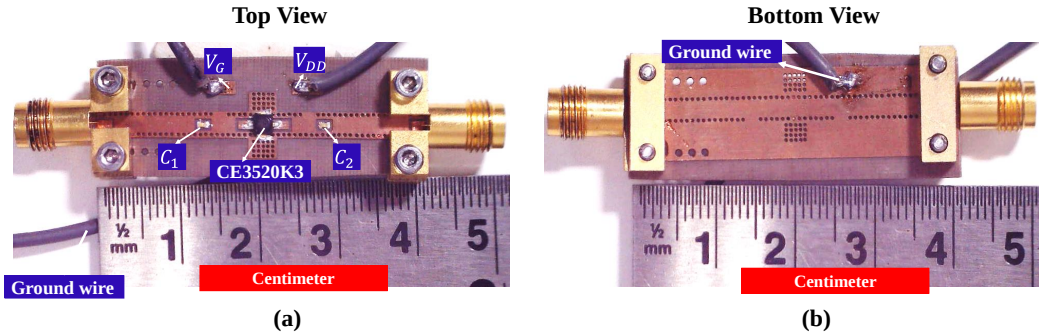


Figure 4.14 : Fabricated prototype of the proposed amplifier circuit;(a) Top View; (b) Bottom View.

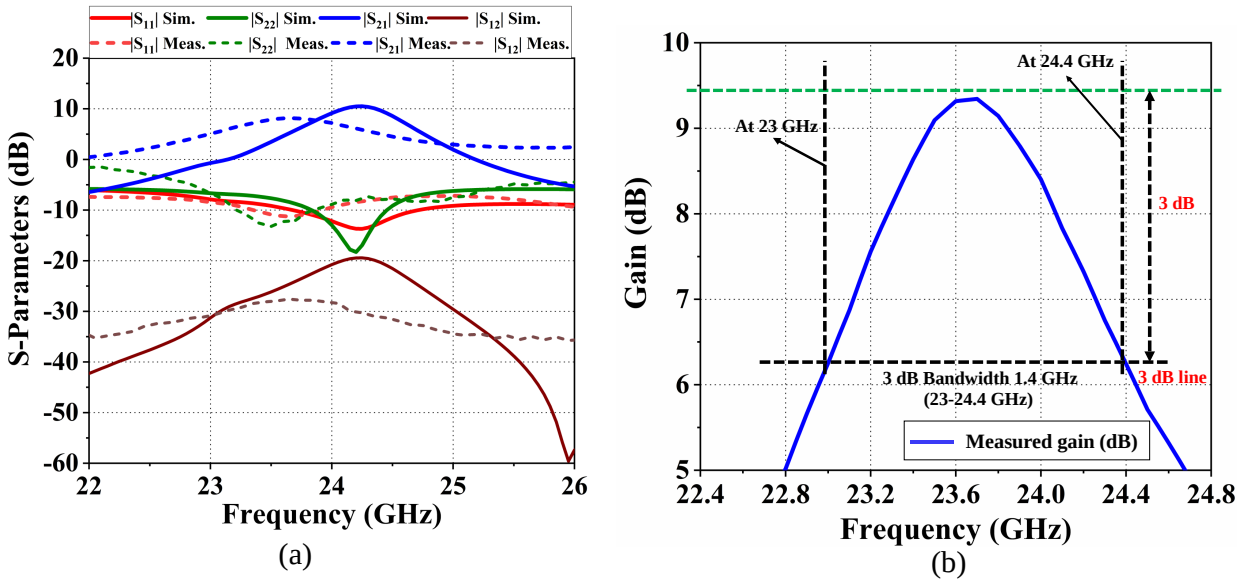


Figure 4.15 : (a) Response of the amplifier circuit; (b) Response of 3-dB bandwidth of the amplifier

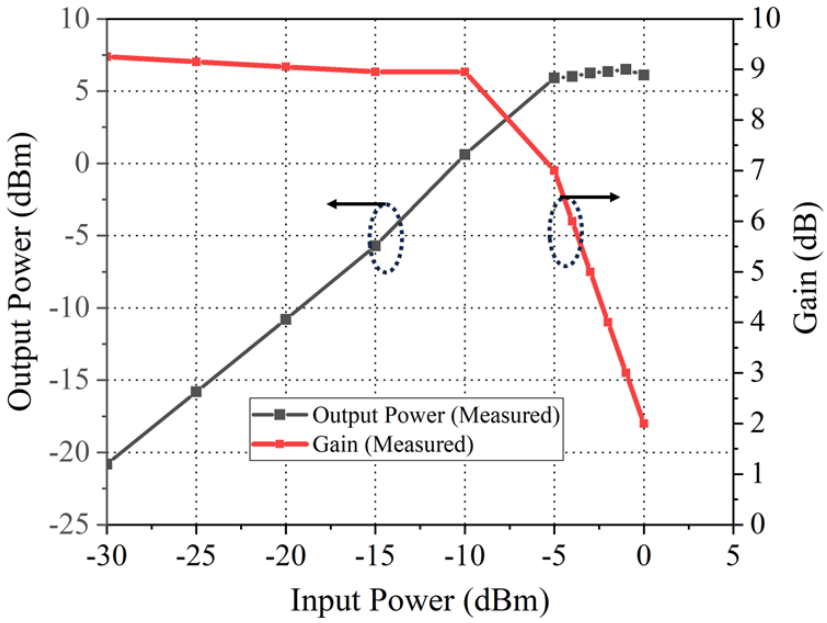


Figure 4.16 : Large Signal Measurement result at 24 GHz

Table 4.2 : Comparisons of the proposed amplifier circuit with the previous reported amplifier's

Ref.	**Technology**	**Frequency (GHz)**	G_{max} **(dB)**	$\lvert S_{11}\rvert/\lvert S_{22}\rvert$ **(dB)**	P_{diss} **(mW)**	**G.R (dB)**
[Eom and Lee, 2017].	HMSIW[a]	4–7.05	15	−10/−11	193.5	N.M.
[Sabzi *et al.*, 2020b].	Microstrip[b]	4–5	7	−14/−18	50	N.M.
[Othman *et al.*, 2007].	Microstrip[a]	5.8	14	−10/−11	120	N.M.
[A and S, 2008].	SIW[a]	8–12	9	−13/−10	N.M.	< 2
TW.	**SICL**[a]	**23.35–24.05**	**9.2**	**−12/−13**	**34**	**< 1**

[a] Single-Stage transistor, [b] Two-Stage transistor, N.M.: Not Mentioned.

voltage of $V_{DD} = 2$ V, $V_{GS} = -0.2$ V and output current $I_{DS} = 17$ mA using DC supply HMP4030. The response of the 3-dB bandwidth of the amplifier is illustrated in Figure 4.15(b). In Figure 4.16, the 1 dB compression point is observed around -5 dBm, indicating enhanced linearity at 24 GHz. The simulated results were validated against measured data within the frequency range of 22-26 GHz using an Agilent N5234A Network Analyzer, where the measured results followed the simulated results with a slight deviation due to fabrication tolerance and connector losses.

Table 4.2 presents a comparative analysis of the proposed amplifier against other reported amplifiers across different technologies. The proposed design achieves a maximum small-signal gain of 9.2 dB with a gain ripple (G.R) of less than 1 dB within the 23.35-24.05 GHz frequency range. Additionally, the amplifier demonstrates input and output return losses exceeding 10 dB while maintaining low power dissipation, highlighting its superior performance in these key metrics.

4.4 CONCLUSION

The contributions of this chapter play a pivotal role in advancing planar amplifier design by leveraging the unique benefits of Substrate Integrated Coaxial Line (SICL) technology. This study introduces an innovative approach that employs a simple, low-profile configuration, utilizing a cost-effective printed circuit board (PCB) fabrication technique. Notably, this work represents the first reported realization of a planar amplifier circuit operating within the 23.35-24.05 GHz frequency range based on SICL technology. The introduction of this amplifier design addresses key limitations encountered in conventional high-frequency circuits, particularly in terms of shielding effectiveness, integration efficiency, and electromagnetic interference (EMI) suppression. One of the most significant advantages of the proposed SICL-based amplifier is the elimination of microstrip line transitions when integrating surface mount device (SMD) components. Traditional microstrip-based amplifier designs often suffer from unwanted radiation losses and spurious coupling effects due to the discontinuities introduced by transition structures. By directly integrating SMD components into the SICL environment, the proposed design overcomes these challenges, leading to an overall improvement in circuit performance. The self-shielded nature of SICL technology inherently suppresses surface wave propagation, which is a common source of performance degradation in planar circuits. This characteristic ensures minimal interference with adjacent components, making the design highly suitable for dense circuit integration. Moreover, the SICL structure offers enhanced isolation and shielding, effectively reducing the impact of parasitic coupling and external interference. The coaxial nature of SICL technology confines the electromagnetic field within its structure, thereby minimizing losses and improving efficiency at millimeter-wave frequencies. This feature is particularly beneficial for high-frequency applications, where maintaining signal integrity is critical. The reduction of radiation losses further contributes to enhanced gain stability and reliability, making the proposed amplifier design well-suited for modern wireless communication and radar systems operating in the 24 GHz band. In addition to the structural advantages, the proposed amplifier configuration is designed with manufacturability and cost-effectiveness in mind. The use of standard PCB-based fabrication techniques enables scalable production while maintaining high performance. Unlike waveguide-based designs, which require complex and expensive machining processes, the SICL-based approach allows for a streamlined manufacturing process without compromising electrical performance. This makes the technology highly attractive for commercial applications in millimeter-wave communication systems, automotive radar, and next-generation wireless networks. In summary, the proposed SICL-based planar amplifier circuit presents a groundbreaking advancement in high-frequency circuit design. By integrating SMD components seamlessly without requiring microstrip transitions, the design significantly enhances shielding, reduces losses, and minimizes spurious coupling effects. These contributions underscore the potential of SICL technology in addressing critical challenges associated with circuit integration and performance optimization at millimeter-wave frequencies. This work paves the way for further exploration of SICL-based active circuits, fostering innovations in compact, high-performance microwave and millimeter-wave systems.