Appendix A
Input-Output Relationship of CMOS Inverter in the Presence of Variability Issues and Power Supply Noise

This appendix presents the required input-output relationships used in Chapter-3. The input-output relationship of the CMOS inverter has been derived by applying KCL at the output node in Figure 3.2.1. The KCL equation can be written as:

$$-(C_L+\boldsymbol{C_M})\frac{dV_{out}}{dt}+\boldsymbol{C_M}\frac{dV_{in}}{dt}+I_p-I_n=0. \tag{1}$$

The falling edge of output is divided into five different regions as shown in Figure 2.2.2, and the output response of each region is derived individually. Then, these individual responses are concatenated in time to get the final output response of CMOS inverter [Arora *et al.*, 2021b]. The output expressions for the respective regions are written in the following subsections.

Region-I:

In this region, the input is rising from 0 to V_{TN}. The nMOS will be in cut-off mode, and the pMOS will be in linear mode. The output expression of this region can be written as:

$$\boldsymbol{V_{out}(t)}=V_{DD}+\sum_{n=1}^{N}A_{s_n}\sin\phi_{s_n}+\sum_{n=1}^{N}\sum_{k=1}^{\infty}(s_{n_k}-\boldsymbol{a_{n_k}})t^k, \tag{2}$$

where $\boldsymbol{a_{n_k}}$ is the coefficient of t^kth term in the series and can be written as:

$$a_{n_1}=s_{n_1}-\boldsymbol{\gamma_1}\frac{V_{DD}}{\tau}, \tag{3}$$

$$\boldsymbol{a_{n_2}}=s_{n_2}-\frac{a_{n_1}\boldsymbol{\gamma_2}}{2}\left(V_{DD}+A_{s_n}\sin\phi_{s_n}-|V_{TP}|\right), \tag{4}$$

$$\boldsymbol{a_{n_k}}=s_{n_k}-\frac{\boldsymbol{\gamma_2}}{k}\left[\left(V_{DD}+A_{s_n}\sin\phi_{s_n}-|V_{TP}|\right)\boldsymbol{a_{n_{k-1}}}-\frac{V_{DD}}{\tau}\boldsymbol{a_{n_{k-2}}}+\sum_{i=1}^{k-2}s_{n_i}\boldsymbol{a_{n_{k-i-1}}}-\frac{(1+\delta_p)}{2}\sum_{i=1}^{k-2}\boldsymbol{a_{n_i}a_{n_{k-i-1}}}\right], \tag{5}$$

where

$$\boldsymbol{\gamma_1}=\frac{\boldsymbol{C_M}}{(C_L+\boldsymbol{C_M})},\quad\text{and}\quad\boldsymbol{\gamma_2}=\frac{\boldsymbol{\beta_p}}{(C_L+\boldsymbol{C_M})}. \tag{6}$$

Region-II:

In this region the input increases from V_{TN} to $(V_{DD}-|V_{TP}|)$. The transistor pMOS will conduct in linear mode, and nMOS will enter into saturation mode. The output expression for this region is written as:

$$\boldsymbol{V_{out}(t)} = V_{DD} + \sum_{n=1}^{N} A_{s_n} \sin\phi_{s_n} + \sum_{n=1}^{N}\sum_{k=1}^{\infty} (s_{n_k} - \boldsymbol{b_{n_k}})(t-T_1)^k + \boldsymbol{V_{12}}, \tag{7}$$

Where $\boldsymbol{V_{12}} = \sum_{n=1}^{N}\sum_{k=1}^{\infty}(s_{n_k} - \boldsymbol{a_{n_k}})T_1^k$, is a constant at time instance $T_1 = \tau V_{TN}/V_{DD}$. The coefficient of t^kth term is denoted by $\boldsymbol{b_{n_k}}$, and can be expressed as:

$$b_{n_1} = s_{n_1} - \boldsymbol{\gamma_1}\frac{V_{DD}}{\tau}, \tag{8}$$

$$\boldsymbol{b_{n_2}} = s_{n_2} - \frac{\boldsymbol{\gamma_2}}{2}\big(V_{DD} + A_s\sin\phi_s - V_{TN} - |V_{TP}|\big)b_{n_1} \tag{9}$$

$$\boldsymbol{b_{n_3}} = s_{n_3} - \frac{\boldsymbol{\gamma_2}}{3}\left[\big(V_{DD} + A_s\sin\phi_s - V_{TN} - |V_{TP}|\big)\boldsymbol{b_{n_2}} + s_{n_1}b_{n_1} - (\frac{V_{DD}}{\tau})b_{n_1} - \frac{1+\delta_p}{2}b_{n_1}^2\right] + \frac{\boldsymbol{\gamma_3}}{6}\left(\frac{V_{DD}}{\tau}\right)^2, \tag{10}$$

$$\boldsymbol{b_{n_k}} = s_{n_k} - \frac{\boldsymbol{\gamma_2}}{k}\left[\big(V_{DD} + A_s\sin\phi_s - V_{TN} - |V_{TP}|\big)\boldsymbol{b_{n_{k-1}}} - \frac{V_{DD}}{\tau}\boldsymbol{b_{n_{k-2}}} + \sum_{i=1}^{k-2} s_{n_i}\boldsymbol{b_{n_{k-i-1}}} - \frac{1+\delta_p}{2}\sum_{i=1}^{k-2}\boldsymbol{b_{n_i}}\boldsymbol{b_{n_{k-i-1}}}\right], \tag{11}$$

where

$$\boldsymbol{\gamma_3} = \frac{\boldsymbol{\beta_n}}{(1+\delta_n)(C_L + \boldsymbol{C_M})}. \tag{12}$$

Region-III:

The input is rising from $(V_{DD}-|V_{TP|})$ to V_{DD} and nMOS is in saturation, and pMOS is in cutoff mode. The output expression for this region is:

$$\boldsymbol{V_{out}(t)} = \frac{\boldsymbol{\gamma_1}V_{DD}}{\tau}t - \frac{\boldsymbol{\gamma_3}\tau}{6V_{DD}}\left(\frac{V_{DD}}{\tau}t - V_{TN}\right)^3 + \boldsymbol{V_{23}}, \tag{13}$$

where,

$$\boldsymbol{V_{23}} = \sum_{n=1}^{N}\left[A_{s_n}\sin\phi_{s_n} + \sum_{k=1}^{\infty}(s_{n_k} - b_{n_k})(T_2 - T_1)^k\right] + \boldsymbol{V_{12}} - \frac{\boldsymbol{\gamma_1}V_{DD}}{\tau} - \frac{\boldsymbol{\gamma_3}V_{TN}^3}{6V_{DD}} + V_{DD}, \tag{14}$$

and

$$T_2 = \tau\frac{(V_{DD} - |V_{TP}|)}{V_{DD}}. \tag{15}$$

Region-IV:

The input voltage reaches V_{DD} and becomes constant, and the transistors nMOS and pMOS conduct in saturation and cutoff mode, respectively. The output expression can be written as:

$$\boldsymbol{V_{out}}(t) = \boldsymbol{V_{34}} - 0.5\boldsymbol{\gamma_3}(V_{DD} - V_{TN})^2(t - T_3), \tag{16}$$

where,

$$\boldsymbol{V_{34}} = \frac{\boldsymbol{\gamma_1} V_{DD}}{\tau}(T_3 - T_2) + \frac{\boldsymbol{\gamma_3}\tau}{3V_{DD}}\left[\frac{V_{DD}}{\tau}(T_3 - T_2) - V_{TN}\right]^3 + \boldsymbol{V_{23}}, \tag{17}$$

and $T_3 = \tau$ is the rise time of the input data signal.

Region-V:

The input voltage remains at V_{DD} and the output voltage starts decreasing from Region Region-I to all successive regions (i.e., the drain to source voltage of nMOS is decreasing continuously, whereas the input is fixed at V_{DD}), as the input falls bellow V_{sat_n} the transistor nMOS starts conducting in linear mode and pMOS remains in cutoff mode only. The output expression can be written as:

$$\boldsymbol{V_{out}(t)} = \frac{2(V_{DD} - V_{TN})}{(1+\delta_n)(1 + e^{\boldsymbol{\gamma_4}(V_{DD}-V_{TN})(t-T4)})}, \tag{18}$$

where $\boldsymbol{\gamma_4} = \boldsymbol{\beta_n}/(C_L + \boldsymbol{C_M})$, $T_4 = T_{sat_n}$, and V_{sat_n} is the saturation voltage of nMOS at T_{sat_n}.

To get the final output response of the CMOS inverter, the output responses of all the regions are concatenated in time.

Publications

Journal Articles

1. V. K. Verma and J. N. Tripathi, "Variability-Aware Modeling of Power Supply Induced Jitter," in *IEEE Transactions on Signal and Power Integrity*, vol. 3, pp. 47-55, 2024.

2. V. K. Verma and J. N. Tripathi, "Analytical Modeling of Deterministic Jitter in CMOS Inverters," in *IEEE Transactions on Signal and Power Integrity*, vol. 2, pp. 64-73, 2023.

3. V. K. Verma and J. N. Tripathi, "Device Parameters Based Analytical Modeling of Ground-Bounce Induced Jitter in CMOS Inverters," in *IEEE Transactions on Electron Devices*, vol. 69, no. 10, pp. 5462-5469, Oct.2022.

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1. V. K. Verma, D. Junjariya and J. N. Tripathi, "Investigating PSN and GBN Induced Jitter at Different Stages of a Chain of CMOS Inverters," 2024 *IEEE Electrical Design of Advanced Packaging and Systems (EDAPS)*, Bangalore, India, 2024, pp. 1-3.

2. V. K. Verma and J. N. Tripathi, "Investigating the Impact of Variability on Deterministic Jitter in VLSI Circuits," 32nd *IFIP/IEEE International Conference on Very Large-Scale Integration* (*VLSI-SoC 2024*), Tangier, Morocco, 2024, pp. 1-2.

3. V. K. Verma, B. S. Challa and J. N. Tripathi, "Modeling of Variability-Aware Supply-Induced Jitter in VMD Circuit Driving Long Transmission Lines," *2024 IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity (EMC+SIPI)*, Phoenix, AZ, USA, 2024, pp. 58-62.

4. V. K. Verma, D. Junjariya and J. N. Tripathi, "Modeling Power Supply and Ground-Bounce Induced Jitter for a Voltage-Mode Driver Circuit driving Long Transmission Lines," *2023 IEEE Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMC+SIPI)*, Aug. 2023, Grand Rapids, MI, USA, 2023, pp. 657-661.

5. V. K. Verma and J. N. Tripathi, "Analytical Modeling of Time Interval Error in CMOS Inverters in presence of Supply and Ground Variations," *2023 Joint Asia-Pacific International Symposium on Electromagnetic Compatibility and International Conference on ElectroMagnetic Interference & Compatibility (APEMC/INCEMIC)*, Bengaluru, India, 2023, pp. 1-4.

6. V. K. Verma and J. N. Tripathi, "Variability-Aware Modeling of Supply Induced Jitter in CMOS Inverters," *2023 IEEE 27th Workshop on Signal and Power Integrity (SPI), Aveiro, Portugal*, 2023, pp. 1-4.

7. V. K. Verma and J. N. Tripathi, "Variability-Aware Modeling of Supply Induced Jitter in CMOS Inverters," *European IBIS Open Forum*, 2023. https://ibis.org/summits/may23/verma.pdf.

8. V. K. Verma and J. Narayan Tripathi, "Analytical Modeling of Ground Noise Induced Jitter in CMOS Inverters," 2022 *IEEE 19th India Council International Conference (INDICON)*, Kochi, India, 2022, pp. 1-4.

9. D. Singh, V. K. Verma and J. N. Tripathi, "Estimating Power Supply Induced Jitter using S-Parameter based Modeling of Transmission Media," *2021 IEEE* 18th *India Council International Conference (INDICON)*, Guwahati, India, 2021, pp. 1-5. **(Best Paper Award)**

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