1
Introduction

In recent years, the rise of the Internet of Things (IoT) and the growing demand for affordable and wearable technologies have driven the advancement of electronic devices that are cost-effective, energy-efficient, mechanically flexible, and biocompatible [Wang et al., 2020, Gao et al., 2019]. These next-generation devices hold significant potential for applications across diverse sectors, including industrial, military, and healthcare domains. As a result, there has been a substantial shift in focus within both the electronics industry and academia, moving away from conventional silicon-based technologies toward the emerging field of flexible electronics. Flexible electronic devices are commonly constructed on light weight, flexible substrates such as plastic or paper sheets[Lee et al., 2024]. Unlike traditional silicon wafer-based devices, which are rigid, costly, lack biocompatibility, and operate at higher voltages, flexible electronic devices offer advantages such as lower costs, mechanical flexibility, lightweight design, biocompatibility, and operation at lower voltages. These devices are always expected to exhibit stable electrical operation under mechanical deformation, making them ideal for next-generation applications, including foldable displays, storage devices, and wearable and flexible sensors [Lee et al., 2024]. The schematic diagram of flexible electronics and their applications are shown in Figure 1.1. To enable these applications, various thin-film devices, such as thin-film transistors (TFTs), solar cells (SCs), light-emitting diodes (LEDs), and emerging non-volatile memory devices are extensively studied in the field of flexible electronics.

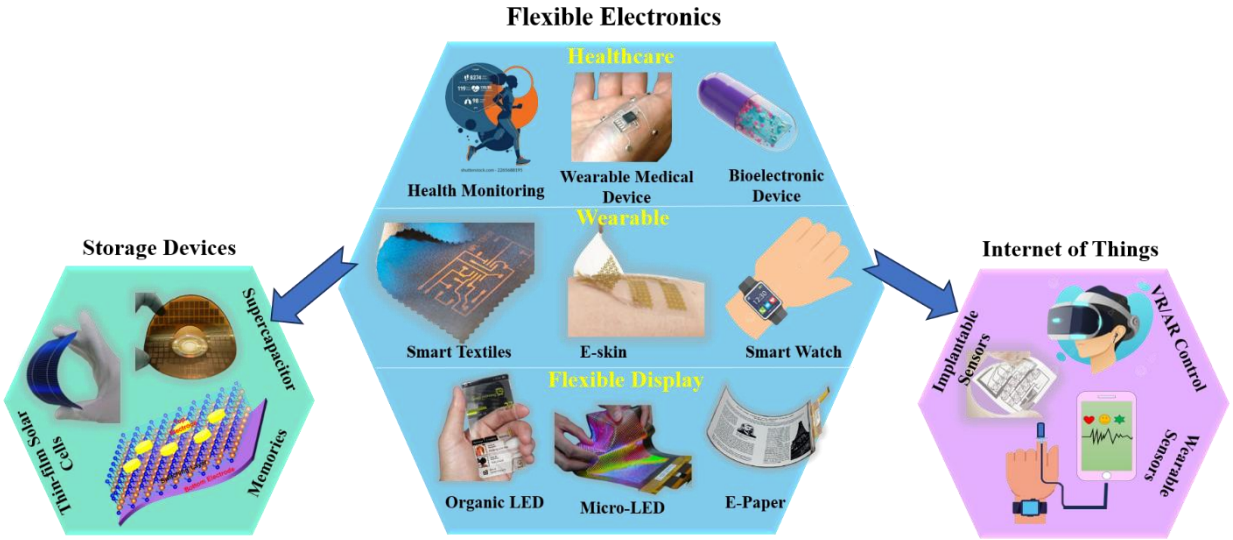


Figure 1.1 Schematic diagram of flexible electronics and its applications.

To realize the potential of flexible electronics, non-volatile memory devices play a crucial role in enabling reliable data storage and retrieval within these systems. Flexible non-volatile memory devices have gained significant attention as a solution for data storage in future electronic applications. These devices offer various advantages, including being thin, lightweight, printable, foldable, and stretchable, making them highly suitable for modern technological needs. There are various flexible non-volatile memory technologies available such as flash memory, resistive random-access memory (RRAM), and ferroelectric-based memories such as ferroelectric random-access memory (FeRAM) and ferroelectric field-effect transistor memory (FeFET). Flexible RRAM stands out among flexible memory technologies due to its simple metal-insulator-metal structure, low power consumption, scalability, and superior mechanical flexibility. Compared to magnetic RAM (MRAM) and spin-transfer torque RAM (STTRAM), RRAM offers easier fabrication, lower switching voltages, reduced heat generation, and higher scalability for nanoscale applications. Additionally, RRAM supports multilevel storage and avoids the complex

magnetic or spin-based switching mechanisms of its counterparts. Unlike phase-change memory (PCM) and ferroelectric RAM (FeRAM), RRAM is faster, more durable, and easier to scale, with fewer issues related to material fatigue or polarization. It also outperforms organic memories in electrical performance while maintaining excellent bending durability. With high I_{ON}/I_{OFF}, non-volatility, and compatibility with various materials, RRAM is ideal for wearable devices, foldable electronics, and IoT applications, making it a versatile, cost-effective, and low power device for next-generation flexible electronics.

1.1 Resistive Random Access Memory (RRAM)

Resistive random access memory (RRAM) represents an emerging class of non-volatile memory devices built with a simple three-layer structure: two conducting electrodes separated by an insulating layer. These devices operate by switching between distinct resistance states - a high resistance state (HRS) and a low resistance state (LRS) which correspond to binary '0' and '1' values respectively. The fundamental operating principle relies on the application of strong electric fields across the dielectric layer, which induces changes in its resistance [Lanza et al., 2019, Wong et al., 2012].

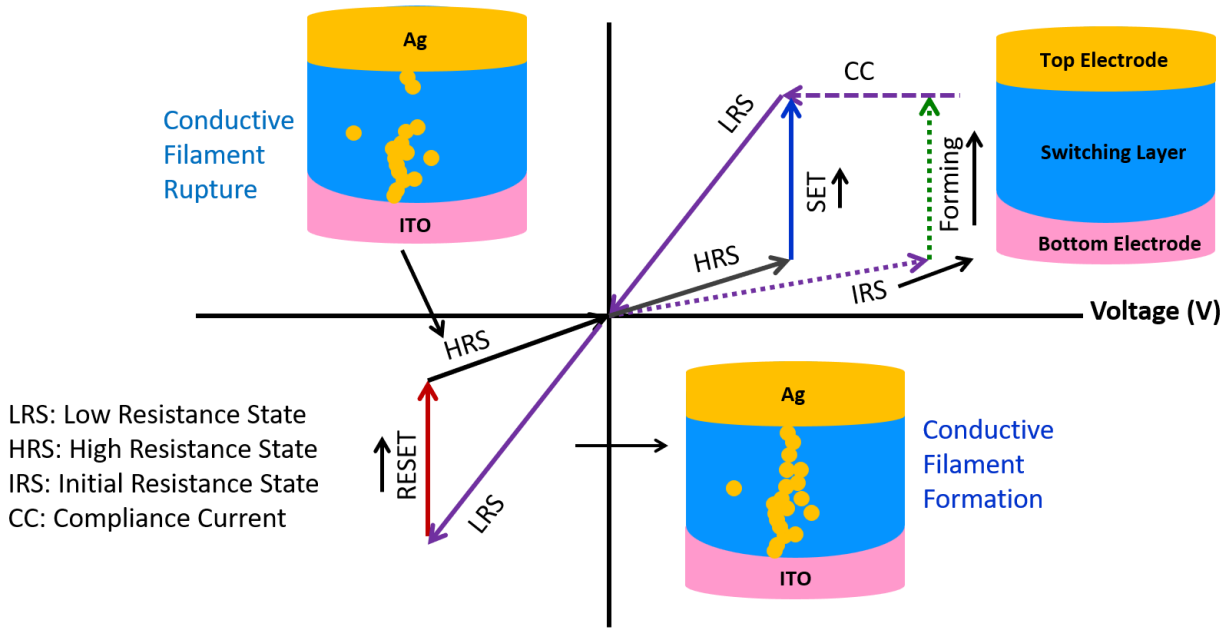


Figure 1.2 Schematic diagram of switching mechanism of bipolar RRAM device.

The switching mechanism involves the formation and disruption of conductive pathways between the electrodes under applied voltage. The schematic diagram of switching mechanism of bipolar RRAM device is shown in Figure 1.2. It illustrates the various steps involved in the switching mechanism of a typical bipolar resistive random-access memory (RRAM) device. Initially, the device behaves as an insulator, remaining in HRS. To initiate the switching process, a forming step is required, which transitions the device to a LRS by creating a conductive filament between the top and BEs. While forming-free RRAM devices are preferred as they simplify operation and avoid the need for high forming voltages, forming remains a critical step in many RRAM devices. This process involves a soft breakdown, where current density and electric field intensity are controlled using an external compliance current, typically imposed through a transistor. This regulation prevents permanent breakdown and improves the device's reliability and lifetime. The forming voltage is generally higher than the SET voltage, and its value is influenced by factors such as switching layer thickness, film quality, electrode materials, and testing environment. Once the filament is formed, a reverse bias voltage is required for the dissolution or partial rupture of the filament which is consider as RESET or "erase" process, representing the storage of a '0' bit. However, the reset process is stochastic, leading to residual

filaments in the switching layer, which can cause reliability issues such as increased leakage current, reduced memory window, and poor variability across cycles and devices. Subsequent operation cycles involve alternating RESET and SET processes to switch between HRS and LRS. The SET process, which rewrites a '1' bit, re-forms the conducting filament through mechanisms such as metal migration or conducting bridge RAM (CBRAM), redox reactions in the oxide layer or valance change RRAM (VCRAM), or charge trapping/detrapping in organic or polymer-based switching layers.

1.1.1 Valance change RAM (VCRAM)

The switching mechanism in VCRAM is governed by the reduction-oxidation (redox) reactions occurring in transition metal oxides under a strong electric field applied across the electrodes. This process drives the migration of ions within the device. Typically, the VCRAM structure employs an easily oxidizable top electrode (TE) such as Al, Ta, Hf, or Ti, along with an inert bottom electrode (BE) made of high work function materials like Pt or Ir. During the electroforming process, the initial soft breakdown of the pristine metal-oxide layer results in the generation of negatively charged oxygen ions (O^{2-}) and positively charged oxygen vacancies ($V_{ö}$). The redistribution of these species within the oxide layer alters the valence state of the transition metal cations (M^{n+}), thereby modifying the electrical conductivity of the switching layer. The generation and movement of oxygen vacancies can be explained with the following equations:

$$O_o \rightleftharpoons \frac{1}{2}O_2 + V_{ö} + 2e^- \quad (1.1)$$

$$me^- + M^{n+} \rightleftharpoons M^{(n-m)+} \quad (1.2)$$

Using Kroger-Vink notation, the oxygen ion located in its lattice site is represented as O^o, while the oxygen vacancy is denoted as $V_{ö}$. Under an electric field, oxygen ions migrate toward the anode-oxide interface, where they can either oxidize to neutral non-lattice oxygen atoms and diffuse into the electrode or react with the oxidizable anode to form a thin interface oxide layer, which may exhibit insulating or conducting properties. Simultaneously, positively charged oxygen vacancies drift toward the cathode, forming an n-type semiconducting region near the interface, referred to as the "virtual cathode." Ultimately, these vacancies create a conductive filament within the oxide layer, establishing a high-conductivity path between the electrodes.

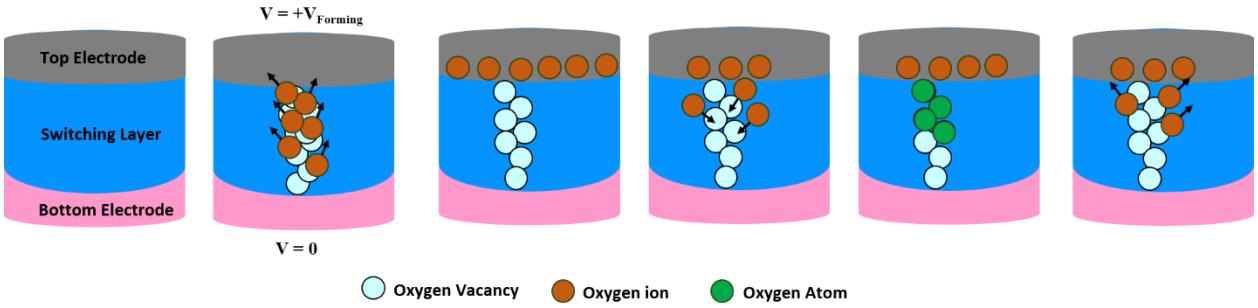


Figure 1.3 Schematic diagram of switching mechanism in VCRAM.

In filamentary VCRAM devices, this conductive filament governs the switching behavior in unipolar and bipolar modes during the forming, set, and reset processes. In contrast, when one electrode forms a Schottky contact and the other forms an Ohmic contact, the device is classified as interface-type VCRAM. The Schottky barrier at the interface causes energy band bending, aligning the energy bands with the Fermi levels. The migration of oxygen vacancies modulates this Schottky barrier, regulating the device's resistance. These devices often exhibit gradual set and reset processes, making them suitable for neuromorphic computing applications. The migration of ions within VCRAM is influenced by electric drift due to potential gradients, Fick diffusion resulting from ion concentration gradients, and thermophoresis caused by temperature gradients. Such complex interactions and processes highlight the high versatility and potential of VCRAM for advanced memory and computing technologies [Wong et al., 2012].

1.1.2 Conducting Bridge RAM (CBRAM)

Unlike VCRAM, the switching mechanism in CBRAM devices is governed by the migration of metal ions from an electrochemically active electrode. When a voltage bias is applied to the active metal electrode, it undergoes oxidation, releasing metal cations that migrate through the insulating dielectric layer and connect to an inert electrode at the opposite terminal of the device. In CBRAM device where Ag active TE was taken the switching process can be divided into four stages as shown in Figure 1.4.

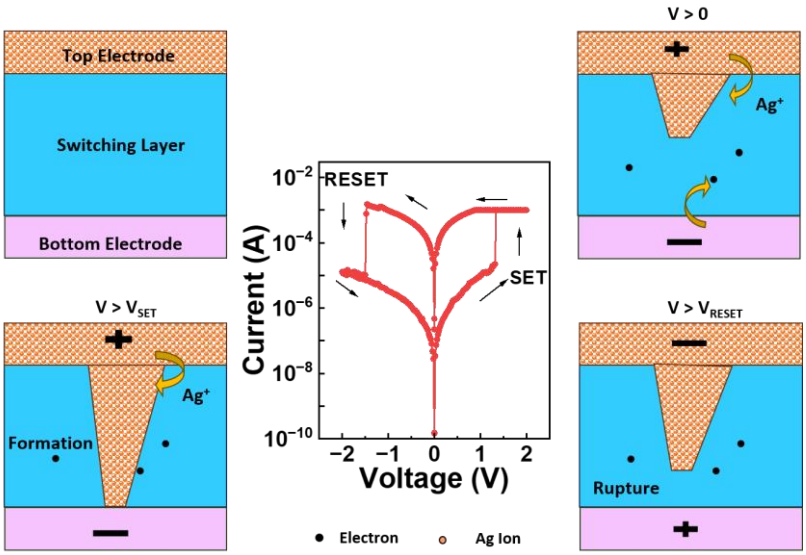


Figure 1.4 Schematic diagram of switching mechanism in CBRAM.

Initially, the pristine device is in a high-resistance state (HRS) and often requires a forming step to activate its functionality. In the absence of a voltage bias, metal ions do not migrate from the TE into the dielectric. However, when a small positive voltage is applied to the Ag electrode, electrochemical dissolution occurs, generating Ag cations ($Ag \rightarrow Ag^+ + e^-$) while electrons are simultaneously injected from the BE. As the applied voltage increases, more Ag ions migrate through the dielectric layer and are reduced to Ag atoms near the dielectric-BE interface ($Ag^+ + e^- \rightarrow Ag$). The accumulation of these Ag atoms leads to the formation of a conductive filament, modulating the device's conductance. With a sufficient voltage at the TE, the Ag atoms eventually create a continuous highly conductive pathway between the two electrodes, completing the forming process and transitioning the device from HRS to LRS. This marks the completion of the SET process, and the device retains its LRS state even after the voltage is removed. During the reset process, reversing the voltage polarity oxidizes the Ag atoms back into ions, which migrate towards the TE, breaking the conductive filament and returning the device to the HRS. The ion migration and conductive filament formation in CBRAM devices are commonly observed through cross-sectional transmission electron microscopy (TEM).

The most commonly used active metal electrodes in CBRAM devices include Ag, Cu, Ni, and Al, as these metals readily dissolve and migrate through the dielectric layer under an applied electric field. Since the switching behavior of CBRAM devices largely depends on the activity of the TE, the switching is typically bipolar, with the voltage bias applied to the TE while the BE remains grounded [Kozicki and Barnaby, 2016].

1.1.3 Structures of RRAM device

The RRAM device typically consists of a metal-insulator-metal (MIM) sandwich structure. Depending on the configuration and spatial relationship between the top and BE, RRAMs can be categorized into three distinct types: common BE, cross-point, and cross-bar, as shown in Figure 1.5. Devices with common BE configurations are advantageous due to their simple fabrication process, making them ideal for studying the fundamental resistive switching properties of

various materials. For materials with small lateral dimensions, the cross-point structure is a highly suitable choice. Meanwhile, the cross-bar structure holds significant promise for three-dimensional high-density stacking and circuit integration, making it the most preferred configuration for advanced applications.

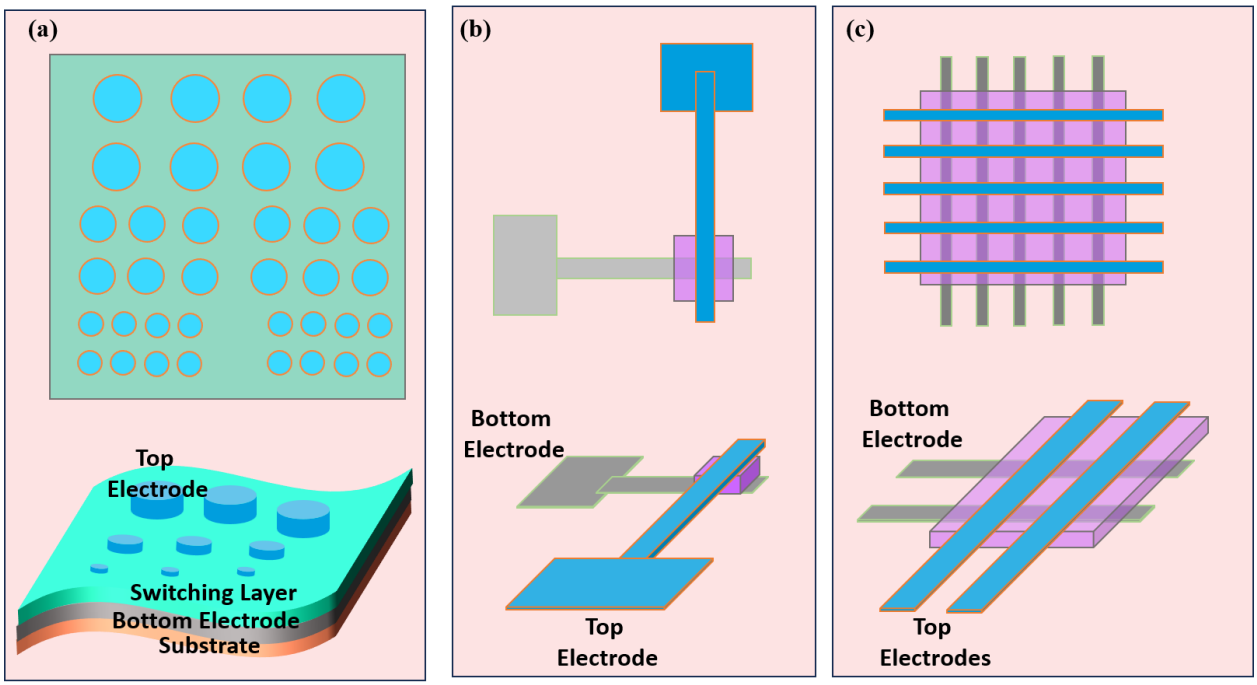


Figure 1.5 Schematic structures of the commonly used RRAM device. (a) BE is common for each cell and the switching layer and TEs were patterned. (b) Cross-point structure. (c) Cross-bar structure forms multiple cross-point cells interconnected to each other.

1.2 Performance Parameters for Resistive Switching Devices

The electrical characteristics of an RRAM device play a crucial role in interpreting its switching performance. However, achieving optimal electrical performance is related with a meticulous fabrication process. Ensuring a uniform and high-quality switching layer with well-defined interfaces to the electrodes is essential for developing high-performance devices. Maintaining a high vacuum environment during the transition between fabrication steps is highly desirable, as it minimizes contamination and preserves interface quality. Unfortunately, this is often challenging to achieve due to the use of different deposition equipment for electrodes and the switching layer. To evaluate the performance of an RRAM device, several key electrical parameters must be analyzed. These parameters provide critical insights into the device's resistive switching behavior, reliability, and potential for practical applications.

1.2.1 Endurance

Endurance refers to the number of cycles a device can switch between HRS and LRS while maintaining a decent I_{ON}/I_{OFF} distinguishable between the two states. This frequent switching can lead to performance degradation and permanent damage of the device. the testing of endurance involves performing continuously repeated *I-V* dual voltage sweeps on a resistive switching RRAM device to measure the resistance or current of HRS and LRS using a minimum read voltage of 0.2 V. While this method ensures accurate detection of switching behavior for each cycle, it can be time-consuming, particularly when dealing with lower current levels. Endurance tests determine the device's ability to maintain reliable performance over multiple SET/RESET *I-V* cycles. Figure 1.6(a) illustrates the endurance plot for approximately 450 consecutive DC cycles of an RRAM device with silver (Ag) as the TE and indium tin oxide (ITO) as the BE. The characterization was performed using a Keithley 4200 system. A DC voltage sweep was applied across the electrodes, and the LRS and HRS currents at 0.2 V were measured and

plotted separately. This endurance plot highlights the clear distinction between LRS and HRS, confirming the device's suitability for RRAM applications. Although the I_{ON}/I_{OFF} is not exceptionally high, the two states are distinguishable, making the device a viable candidate for non-volatile memory applications. The variation in the endurance can be improved by adding composite or metal oxide in the switching layer

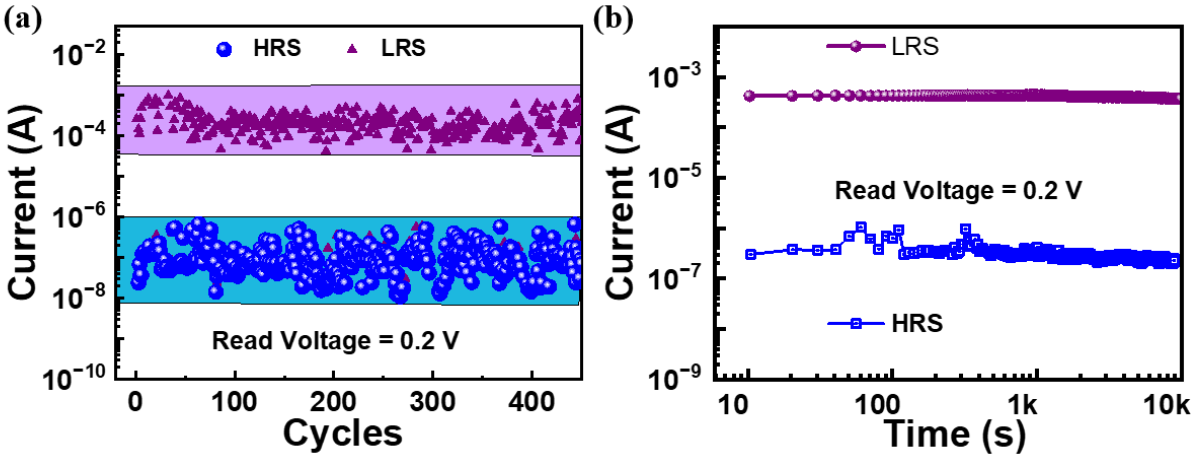


Figure 1.6 Endurance plot of RRAM device at read voltage of 0.2 V for more than 450 consecutive DC cycles with distinguishable LRS and HRS throughout the measurement. **(b)** Retention of RRAM device at read voltage of 0.2 V for around 10000 seconds with distinguishable LRS and HRS throughout the test.

1.2.2 Retention

Data retention in RRAM devices assesses the stability of the LRS and HRS over a long duration of time. This retention period determines how long a RRAM device can reliably maintain its state. By applying a fixed voltage bias of minimum read voltage of ~0.2 V and measuring the current over time (I-t) for both LRS and HRS, retention characteristics can be evaluated. While HRS retention is typically stable as it represents the natural state of the device when no or minimal bias is applied, maintaining a long retention time in LRS is more challenging due to atomic rearrangements caused by the SET voltage. The stability of the LRS largely depends on the compliance current during the SET operation, where a higher compliance current forms stronger conductive filaments, leading to better retention compared to lower compliance currents. The retention plot of flexible RRAM with PVK:MoS_2/TiO_2 hybrid switching layer for around 10000 seconds at read voltage of 0.2 V is shown in Figure 1.6(b).

It can be observed from the results, both LRS and HRS are stable throughout the time period, which is suitable for the reliable non volatile memory application. The standard value of retention time for a practical device should be measured for around 10 years with sample keeping at 85°C, which is too long and not feasible for direct measurement. As a result, the retention value at 85°C is typically extrapolated using the Arrhenius equation based on retention data obtained at different temperatures.

$$Life\ Time = B \times exp(\frac{E_a}{kT}) \tag{1.3}$$

Retention is completely related to filament formation and rupture of the device, thus, since the early 2010s, various switching material optimizations have been tried to improve retention test.

1.2.3 Variability

Scalability and variability are critical challenges in the development of reliable RRAM devices, particularly for flexible electronics. Scalability refers to the ability to maintain device performance and uniformity as memory arrays are scaled down for higher density. Variability, on the other hand, includes two main types: device-to-device variability and cycle-to-cycle

variability. Device-to-device variability arises due to inconsistencies in fabrication, such as non-uniform thicknesses, rough interfaces, or dimensional differences between devices. Improving fabrication processes by ensuring uniform switching layer thickness, smooth interfaces, and precise device dimensions can significantly reduce this variability. The *I-V* characteristics of 15 devices of a sample is shown in Figure 1.7(a), it shows the device to device variability of a hybrid bilayer Ag/MoS_2:PVK/TiO_2/ITO flexible RRAM device.

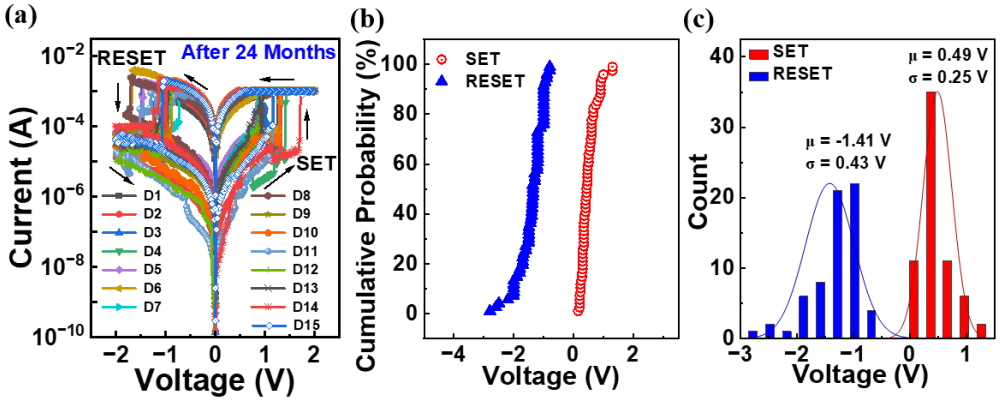


Figure 1.7 Cumulative probability distribution and statistical distribution of SET and RESET voltages respectively of a particular device for cycle-to-cycle variability test. **(c)** I-V characteristics of a particular flexible RRAM device for testing of device-to-device variation.

While cycle-to-cycle variability is primarily caused by the stochastic formation and rupture of conductive filaments, which introduce inconsistencies in electrical characteristics across repeated switching cycles. The unpredictable dimensions and locations of conducting filament formation and rupture aggravate this variability. Although challenging, understanding the exact physical mechanisms behind resistive switching can aid in addressing this issue. To analyze and mitigate variability, recommended methods include plotting electrical parameters such as HRS, LRS, and switching voltages using histograms, cumulative distributions, or Weibull distributions. The cumulative probability distribution and statistical distribution of a particular device is shown in Figure 1.7 (b & c) [Saini and Tiwari, 2024]. The standard deviation and average of SET voltages are 0.25 V and ~0.5 V respectively, while the RESET voltage was distributed with standard deviation and average value of 0.41 V & -1.43 V respectively. This voltage distribution profile indicates the reliable and consistent switching of the device. These statistical analyses also provide insights into the uniformity and reliability of the devices, enabling the determination of threshold values for distinct resistance states. For instance, Weibull distribution analysis can confirm the reliability of switching cycles by evaluating shape factors. The Weibull distribution is most commonly used mathematical equation for the distribution as shown below:

$$\text{Ln-ln}(1\text{-f}(y)) = \beta \ln(x) \tag{1.4}$$

where β is the shape factor, which is the slope of the Weibull distribution curve. Higher β implies higher reliability of the system. The variation coefficient (CV) is a statistical measure used to quantify the relative variability or dispersion of a dataset relative to its mean. A lower value of CV signifies greater consistency in the data, whereas a higher CV indicates increased variability. In flexible RRAM devices, variability can be controlled by improving the fabrication environment, employing advanced material deposition techniques, and optimizing device architectures. Additionally, variability is not always a limitation; it can be leveraged for applications such as true random number generators and physically unclonable functions for hardware security. Future research should focus on balancing variability reduction for memory applications while exploring its advantages in security and neuromorphic computing.

1.3 Conduction Mechanism of Resistive Switching

Understanding of current conduction mechanisms in RRAM devices is essential for their development as reliable resistive memory device. Since RRAM materials are typically semiconductors or insulators, their conduction mechanisms must be thoroughly studied. The charge transport behavior in these devices depends on the underlying principles of conduction mechanisms in such materials. To analyze and optimize the performance of RRAM devices, it is crucial to understand the fundamental conduction mechanisms involved. These mechanisms can be classified into different categories, each describing specific charge transport phenomena that govern the electrical behavior of the device. A detailed understanding of these mechanisms provides insights into resistive switching behavior, enabling improvements in device design and performance.

1.3.1 Direct Tunnelling

Direct tunnelling is a quantum mechanical process where electrons pass through the potential barrier of an insulating layer between two metal electrodes without requiring classical energy to overcome the barrier. This phenomenon arises from the wave-like nature of electrons, which enables them to penetrate regions that are classically inaccessible. The tunneling probability is described using the Wentzel-Kramers-Brillouin (WKB) approximation, which accounts for the barrier height, width, and the effective mass of the electrons. The net tunneling current is determined by the tunneling probability and the difference in electron distribution between the two electrodes, which depends on the applied voltage. This process becomes significant in nanoscale electronic devices, where ultra-thin insulating layers allow measurable tunneling currents. Direct tunneling is a critical mechanism in applications such as tunneling diodes, flash memory, and resistive switching memory devices, influencing their performance and reliability as shown in below in equation (1).

$$I = V \frac{q^2\sqrt{2mq\emptyset_B}}{4\pi h^2 d} e^{\frac{-2d\sqrt{2mq\emptyset_B}}{\hbar}} \tag{1.5}$$

V q, m, $\emptyset$, ħ, d are the applied voltage, charge, electron mass, barrier height, Planck's constant and barrier width, respectively. Direct tunnelling in M-I-M band diagram structure is shown in Figure 1.8(a).

1.3.2 Fowler-Nordheim Tunneling

Fowler-Nordheim (F-N) tunnelling is a high-voltage quantum mechanical phenomenon where charge carriers tunnel through a triangular potential barrier formed by a strong electric field. At low voltages, the system exhibits a band diagram similar to direct tunnelling. However, with increasing voltage, band bending reduces the effective barrier height, allowing charge conduction. The process is described mathematically using the time-dependent Schrödinger equation and WKB approximation, with current density depending on the electric field strength and material properties.

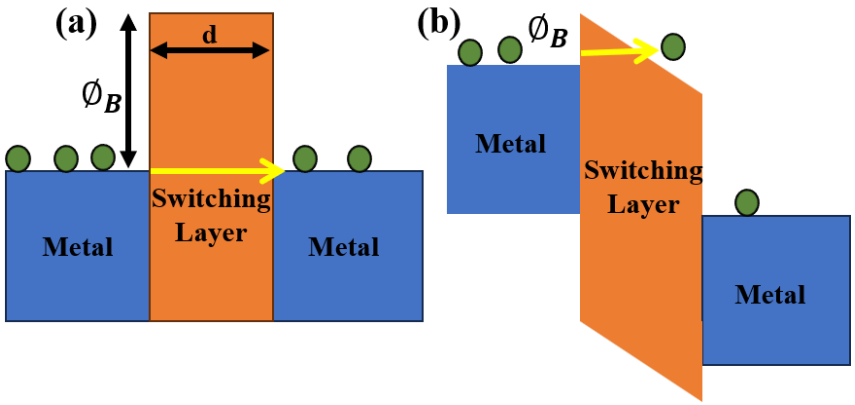


Figure 1.8 Band Diagram of M-I-M structure **(a)** Direct tunneling and **(b)** F-N tunneling**.**

F-N tunnelling is a key conduction mechanism in devices with ultra-thin insulating layers, such as flash memory and resistive switching memory cells, where high electric fields facilitate charge transport. F-N tunnelling in M-I-M band diagram structure is shown in Figure 1.8(b).

1.3.3 Thermionic Emission

Thermionic emission is a thermal excitation process where electrons gain sufficient energy to overcome the potential barrier between a metal and an insulator. The emission is governed by the material's work function and the Richardson-Dushman equation, where current density depends on temperature and material properties. In devices like metal-insulator-metal structures, thermionic emission contributes to current flow, particularly under high-temperature conditions. This mechanism is crucial for understanding charge transport in various electronic and memory devices. Here the current is propotional to square root of voltage

$$(I\alpha\sqrt{V}) \tag{1.6}$$

1.3.4 Poole-Frenkel Emission

In Poole-Frenkel emission, electrons gain sufficient energy from thermal excitation to traverse the insulating material. These thermally energized electrons transition from trap sites within the insulator to the metal contact. The resulting positively charged trap sites, left behind by the electrons, lead to a reduction in the effective barrier height.

$$ln\frac{I}{V}\alpha\sqrt{V} \tag{1.7}$$

1.3.5 Space Charge Limited Conduction

Space charge limited conduction (SCLC) is a mechanism observed in RRAM with low carrier mobility, where the transport of charge is dominated by the density of injected carriers rather than the material's intrinsic carriers. This conduction mechanism becomes significant when the density of carriers injected from the electrodes exceeds the intrinsic carrier density of the semiconductor. Under such conditions, the accumulation of these carriers creates a space-charge effect, altering the internal electric field and influencing current flow. In cases where trap sites are minimal or absent, the *I-V* characteristics simplifies and can be described by a quadratic dependence on voltage. The current density in this trap-free regime follows the expression,

$$J = \frac{9\epsilon_o\epsilon_r\mu}{8d^3}V^2 \tag{1.8}$$

where ϵ is the dielectric permittivity, μ is the carrier mobility, V is the applied voltage, and d is the thickness of the material. Here the current is proportional to square of voltage

1.4 Current Status of Flexible RRAM

In recent years, significant progress has been made in the research and development of flexible RRAM devices and their applications. Decades of extensive investigation have laid a strong foundation for RRAM technology, enabling its potential deployment in futuristic applications such as neuromorphic computing, logic implementation, in-memory computing, random number generation, and memory storage. Table 1.1 highlights the comparison of performance parameters such as SET/RESET voltage, I_{ON}/I_{OFF}, endurance, retention time, and bending radius of flexible RRAM devices on various flexible substrates.

Table1.1 Comparison of flexible RRAM devices performance

Device Structure	*Substrate*	V_{SET} *(V)*	V_{RESET} *(V)*	I_{ON}/I_{OFF}	*Endur.*	*Ret. (s)*	*Radii (mm)*	*Ref*
Cu/ZnO:Mg/ITO	PET	1	-1.5	30	100	14×10^3	20	[Shi et al., 2010]
Al/GO/AL	PES	2.5	-2.5	100	100	1×10^5	9	[Jeong et al., 2010]

Al/GO/ITO	PET	-1.6	2	10^3	100	1×10^7	4	[Hong et al., 2010]
Al/Mn:ZnO/HfO_2/Ti/Pt	Kapton	5	-5	70	50	-	11	[Zhou et al., 2011]
Al/PMMA:PCBM/ITO	PET	5	-5	10^3	-	-	10	[Ho Lee et al., 2011]
Al/GO/ITO	PET	2.2	-3.5	100	100	1×10^4	-	[Wang et al., 2012]
Al/AlOx/CdTe:Sb/Au	PET	10	-10	10^5	15	1.2×10^3	-	[Xie et al., 2013]
Al/PS:PCBM/ITO	PET	-1.5	1.3	10^4	43	1×10^3	4	[Jo et al., 2013]
Al/PMMA:P_3HT/GO/ITO	PET	3.6	-2.6	10^5	80	8×10^3	10	[Lai et al., 2014]
Ag/Al_2O_3/RGO/PMMA/Pentacene/Au	PET	-	-	10^4	800	1×10^5	20	[Han et al., 2014]
Al/ZnO/GO/ITO	PET	2.1	-2	100	1000	1×10^4	4	[Khurana et al., 2014]
Al/GO/Cu	PES	3.5	-0.5	10^3	90	1×10^4	-	[Lin et al., 2014]
ITO/Au NPs-RGO-PVA/Al	PET	0.44	-2.45	10^3	50	1×10^3	-	[Midya et al., 2015]
Ag/ZnO/ITO	PET	3.2	-4.9	10	100	1×10^4	8	[Wu et al., 2015]
Ag/MoS_2/MoO_x/Ag	PEN	0.1	-0.2	2.38×10^5	-	1×10^4	10	[Bessonov et al., 2015]
Mg/Ag-doped Chitosan/ITO	PET	1.6	-0.83	10^2	60	1×10^4	5	[Hosseini and Lee, 2015]
Cu/pEGDMA/ITO	PET	1	-1	10^2	500	1×10^6	4	[Lee et al., 2015]
Al/PI:PCBM/Al	PEN	4	-4	10^4	200	1×10^4	10	[Jang et al., 2015]
Ag/G-QDs/PVP/Ag	PET	1.6	1.7	14	500	30 Days	8	[Ali et al., 2015]
ITO/GO/ITO	PES	1	-1	10	-	1×10^5	10	[Wu et al., 2015]
W/Polyparaxylene/Al	Parylene	2.2	-0.6	10^4	500	2×10^5	10	[Cai et al., 2016]
Al/pV3D3/Cu	PES	5	2	10^7	10^5	1×10^5	3.8	[Jang et al., 2016]
Au/starch/ITO	PET	3	-4	10^3	100	1×10^4	5	[Raeis-Hosseini and Lee, 2016]
Ag/hBN/Cu	PET	0.72	-0.37	~100	550	3×10^3	7	[Qian et al., 2016]
Au/Lignin/ITO	PET	-0.81	0.76	10^3	100	1×10^3	15	[Park and Lee, 2017]
ITO/hBN-PVOH/Ag	PET	0.78	-1	4.8×10^2	1000	-	4	[Siddiqui et al., 2017]
Pt/GO/Ti/Pt	PEN	3.3	-3.2	100	200	1×10^3	9	[Nagareddy et al., 2017]
Cu/GO-MoS_2/Ag	Paper	3.3	-3.3	10^4	500	1×10^4	-	[Yalagala et al., 2019]
ITO/MoS_2-RGO/Ti	PET	0.6	-0.6	~10	200	1×10^4	10	[Wu et al., 2019]
Al/Au/Nitrocellulose/Au	PI	2.65	-1.67	10^3	100	1×10^4	10	[Lee et al., 2020]

Ag/P3HT:OD/Ag	PET	1.5	-1.5	5×10^2	50	1×10^4	5	[Sherazi et al., 2020]
Ag/TiO_2/ITO	PET	1.5	-1	10	100	2×10^3	9	[Zou, 2021]
Al/HfO_x/Al:HfO_x/HfO_x/ITO	PET	1.45	-2.32	10^3	200	1×10^4	2.5	[Paul et al., 2022]
Au/CPR1/Au/ITO	PET	-2	2.5	10^8	1000	3×10^7	3	[Zhou et al., 2022]
ITO/PAA:PEI/ITO	PET	-2	2	50	-	1×10^4	2	[Ren et al., 2022]

1.5 Performance Requirements and Challenges of Flexible RRAM

Flexible RRAM represents a key technology for future electronics, particularly in wearable devices, foldable displays, and flexible sensors. To achieve practical applications, several performance requirements must be met. First, flexible RRAM must exhibit high endurance, maintaining its write/erase functionality over extensive cycling without failure. It should also demonstrate excellent data retention, ensuring information remains stable over long periods despite mechanical deformations such as bending or stretching. Low operating voltage and power consumption are critical to support energy-efficient operations in portable and wearable devices, while fast switching speeds are necessary for real-time data processing. Additionally, scalability is essential to enable high-density memory integration, and devices must deliver consistent switching behavior across arrays and over multiple cycles. The mechanical robustness of flexible RRAM is another vital requirement, as it must maintain performance under repeated physical stress, such as folding or twisting, while being compatible with flexible substrates and existing fabrication processes. Despite its promise, flexible RRAM faces significant challenges. Material selection is a critical hurdle, as the switching materials must combine mechanical flexibility with reliable electrical performance. Interfaces between layers are prone to instability, which can lead to issues like diffusion, delamination, or uneven switching behavior. Managing thermal effects, especially in wearable applications, is crucial to ensure stable device operation under varying temperatures. Furthermore, the mechanical fatigue resulting from repetitive bending can degrade materials and interfaces over time. Electrical variability remains another challenge, as resistive switching properties can vary due to defects or stress-induced nonuniformities. Fabrication processes for flexible substrates and layers need to be scalable, cost-effective, and precise to meet commercial demands. Flexible RRAM must also be environmentally stable, resisting the detrimental effects of moisture, oxygen, and other external factors. Lastly, the integration of flexible RRAM with complementary metal-oxide-semiconductor (CMOS) technology presents a challenge, as traditional processes need adaptation for flexible platforms. To address these challenges, innovations in materials and device structures are essential. The use of advanced materials such as two-dimensional semiconductors and polymer composites offers a promising path forward, combining flexibility with high-performance resistive switching. Encapsulation layers can protect devices from environmental factors, while the development of flexible conductive interconnects ensures reliable electrical connections. Printing technologies, such as inkjet and screen printing, provide scalable and low-cost manufacturing solutions, enabling large-area fabrication of flexible RRAM arrays. By overcoming these challenges, flexible RRAM can unlock new possibilities for next-generation electronics, driving progress in areas such as healthcare monitoring, smart textiles, and foldable computing devices.

1.5.1 Flexibility and Stretchability

To meet the requirements of various practical applications, flexible RRAM devices need to exhibit not only excellent electrical properties but also additional features such as mechanical robustness, stability upon bending, transparency, self-healing capabilities, biocompatibility, biodegradability, and user comfort. Achieving these desired characteristics requires a holistic approach involving material innovation, careful selection, and meticulous device design and fabrication. Among these features of flexible RRAM, flexibility is a crucial aspect of a material's mechanical properties, reflecting its ability to withstand bending and stretching without

incurring damage or failure. The bending radius (r) and strain ratio are commonly used to assess these properties. Figures 1.9(a) & (b) illustrate the concepts of bending radius and strain ratio, respectively. The ultimate flexibility of a material is typically characterized by the minimum bending radius (r_{min}), which depends on the elastic modulus and film thickness of the material, as expressed by the equation:

$$r_{min} = \frac{Eh}{2\sigma_y} \tag{1.9}$$

Here, E represents the Young's modulus, h is the film thickness, and σ_y is the yield strength of the material. The mechanical properties of a material can be enhanced by selecting suitable materials, such as 2 D materials composite with polymer, designing innovative device structures like 3D geometries, or incorporating encapsulation layers.

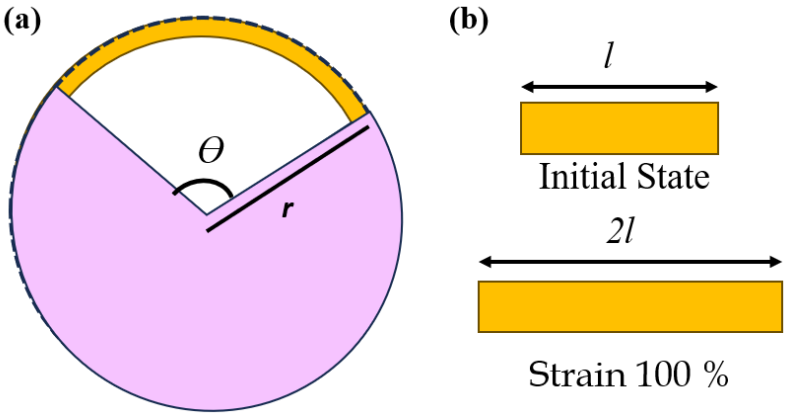


Figure 1.9 Schematic structure of bending radius **(a),** where Θ is bending angle, r is the bending radius and *l* is the length of the device and strain ratio **(b)** of flexible RRAM.

1.5.2 Substrate Selection

The selection of a suitable substrate is also the crucial initial step in fabricating flexible RRAM devices. There are some commonly used substrates available such as polyethylene terephthalate (PET), polyethylene naphthalate (PEN), Polyimide (PI), Polyurethane (PU), and styrene ethylene butylene styrene (SEBS) offer desirable properties like low surface roughness, low modulus, and excellent mechanical stability. The chemical structure of PET, PEN and PI are shown in Figure 1.10. A comparison of key parameters for these materials is summarized in Table 1.2, highlighting their unique characteristics. PET is known for its high cost-effectiveness and excellent transparency, while PEN offers superior thermal and chemical stability compared to PET. However, both PET and PEN have relatively lower film smoothness compared to thermally polymerized polyimide (PI).

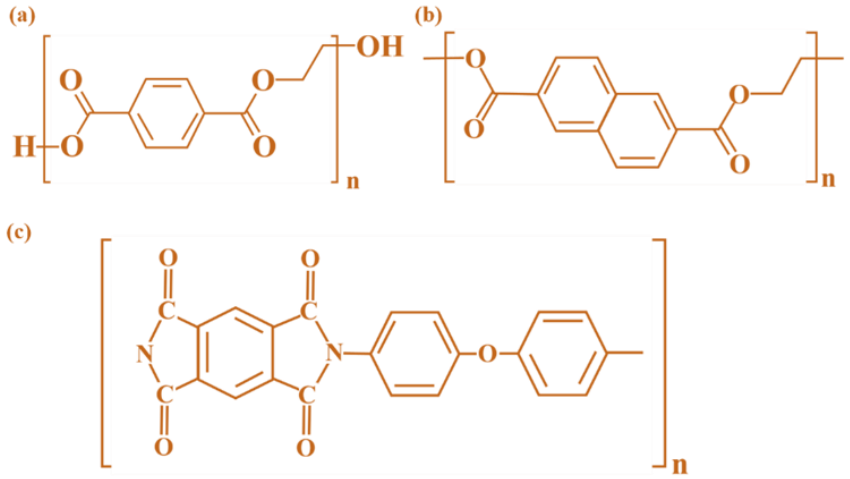


Figure 1.10 Chemical structure of common flexible substrates **(a)** PET, **(b)**PEN, **(c)** PI.

Table1.2 Comparison of properties of flexible substrates

Substrate	Tensile Strength (MPa)	*Young Modulus (MPa)*	T_{Glass} (°C)	T_{melt} (°C)	T_{deg} (°C)	Transparency (%)	Dielectric const	Ref
PET	79-115	3300	78	255	300	>80	3.1	[Yang et al., 2014]
PEN	105	3260	120	263	522	>75	4.2	[Macdonald, 2015]
PI	144	2.5	320	590	-	-	-	[Choi et al., 2019]
PU	7.32	19.4	<-50	>180	>250	>80	>4	[Dai et al., 2020]
SEBS	7.06	0.43	-50	140	377	55	>1.8	[Murthe et al., 2022]

T_{Glass} =Glass transition temperature, $T_{Melt.}$ =Melting temperature, $T_{Deg.}$ = Degradation temperature

1.5.3 Failure Mechanism of RRAM device

Flexible RRAM devices are often subjected to repeated bending during use, which makes them subject to issues like cracks, delamination, and thermal stress accumulation. These challenges can lead to a loss of bistable characteristics, resulting in device failure. [Shang et al., 2017] observed that cracks in the electrode and dielectric layers during bending significantly impact carrier transport, which is a primary reason for device malfunction. These cracks hinder the formation of conductive filaments and may also cause existing filaments to break, as shown in Figure 1.6. Furthermore, the density of cracks tends to increase with repeated bending, disrupting the formation and stability of conductive filaments and compromising the overall device performance. [Ahmad et al., 2021] reported that when the operating current is high, the conductive filaments become thicker, generating significant Joule heating. Over time, with repeated bending and cyclic scanning, the accumulated Joule heat can dissolve portions of the conductive filaments, ultimately leading to device failure. Additionally, if the device remains in the same state for an extended period, electrode material may migrate and deposit on the opposite electrode. This deposition can cause delamination, further contributing to device failure. The schematic structure of cracks in flexible RRAM devices is shown in Figure 1.11

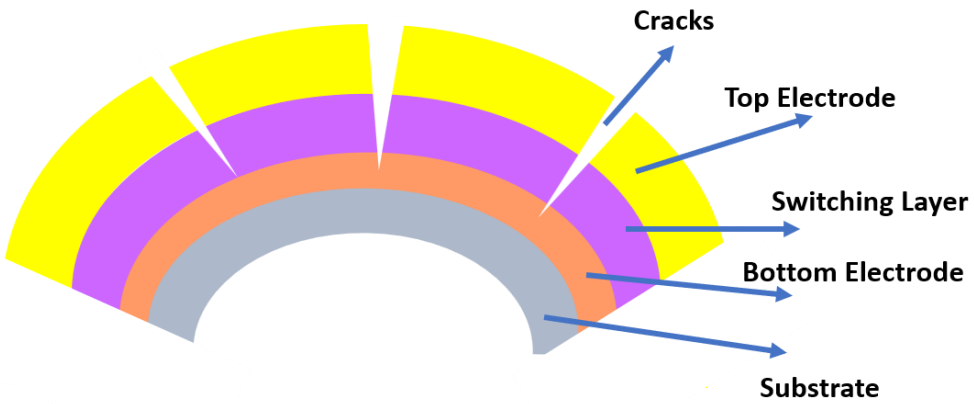


Figure 1.11 Cracks in flexible RRAM devices which is the main reason of failure of device.

1.6 Research Focus and Thesis Organization

The growing demand for efficient, flexible, and high-performance resistive memory devices has driven significant research in the field of flexible RRAMs devices. Flexible RRAMs are at the forefront of next-generation memory technologies due to their potential for use in wearable and foldable electronics. This research focuses on developing solution-processed

composites of polymers and 2D materials as switching layers to achieve enhanced performance in flexible RRAM devices. The work is centred on addressing key challenges such as low switching power, high cyclic endurance, stable multilevel switching, and environmental durability under flexible conditions. To achieve these objectives, various aspects of material synthesis, device fabrication, and performance characterization have been explored. Polymers and 2D materials, known for their unique electrical and mechanical properties, have been utilized to develop hybrid composite layers that combine the advantages of both materials. The integration of these composites enables reliable resistive switching with improved performance metrics such as retention, endurance, and resistance variability, while maintaining excellent mechanical flexibility. The impact of fabrication techniques, environmental stability, and multilevel resistive switching on device performance has also been systematically studied. The objectives of my thesis work are as mentioned below

I. Fabrication of flexible RRAM devices using composition of solution processed polymer and 2D material
II. Exploration of enhanced resistive switching performance, including low voltage, high endurance, excellent data retention, high banding stability
III. Investigation of shelf life, and environmental stability of flexible RRAM devices under varying conditions of humidity and temperature
IV. Forming free, multi-level resistive switching, lowest cycle to cycle and device to device variation with high bending stability

This thesis is organized into seven chapters, each addressing a specific aspect of the research:

Chapter 1: This chapter provides an overview of flexible electronics, emphasizing the role of RRAMs in emerging applications. It explores the structural and functional aspects of RRAMs, focusing on performance parameters such as endurance, retention, variability, and bending stability. The conduction mechanism and current status of flexible RRAM with performance parameters and challenges is extensively discussed.

Chapter 2: The fabrication techniques used in this research, including solution deposition methods and physical deposition processes like atomic layer deposition (ALD), are detailed in this chapter. It also covers the characterization tools employed for analyzing material properties and device performance, including electrical, morphological, and thermal analyses.

Chapter 3: This chapter focuses on the investigation of resistive switching behavior in the selected materials and their combinations, including poly(4-vinylphenol) (PVP), poly(N-vinylcarbazole) (PVK), molybdenum disulfide (MoS_2), molybdenum diselenide ($MoSe_2$), titanium dioxide (TiO_2), and their composites. These materials are explored for their potential as active switching layers in RRAM devices, emphasizing their distinct contributions to switching mechanisms, operating voltages, and reliability.

Chapter 4: This chapter presents the optimization of RRAM devices using a hybrid bilayer structure comprising high-k TiO_2 and poly(4-vinylphenol) (PVP) nanocomposites integrated with molybdenum disulfide (MoS_2). The primary goal is to demonstrate reliable and efficient resistive switching behavior in both rigid and flexible RRAM devices. This work focuses on achieving low operating voltages, high I_{ON}/I_{OFF}, excellent retention, and mechanical stability, which are critical for the next generation of non-volatile memory devices.

Chapter 5: This chapter focuses on the development and comprehensive evaluation of flexible RRAM devices utilizing a hybrid bilayer structure of PVK:MoS_2, and TiO_2. The primary objectives are to enhance switching performance, environmental stability, and shelf life. The

integration of solution-processed PVK:MoS_2 nanocomposites with ALD-deposited TiO_2 aims to achieve reliable resistive switching, low operating voltages, and excellent endurance. A particular emphasis is placed on the device's stability under varying environmental conditions such as humidity and temperature, ensuring their feasibility for long-term use in flexible electronics.

Chapter 6: This chapter investigates composite of a rarely explored 2D material ($MoSe_2$) with PVP as a potential resistive switching layer for flexible RRAM devices. a composite material made from polymer and a 2D material, specifically PVP:$MoSe_2$, for use as a resistive switching layer in flexible RRAM devices. The devices demonstrate impressive resistive switching characteristics, such as low voltage operation, high endurance, and retention time, alongside stability under bending conditions. The PVP layer functions as a charge blocking layer, while $MoSe_2$ serves as a charge trapping medium. The results indicate low cycle-to-cycle variation, confirming device reliability, and highlight the potential of PVP:$MoSe_2$ composites for multi-bit storage in flexible electronics. Overall, the findings suggest promising applications for this composite in the development of high-performance flexible RRAM devices.

Chapter 7: The final chapter summarizes the key findings and contributions of this research. It outlines the conclusions drawn from the studies conducted and provides insights into the future scope of work in the development of flexible RRAM devices for advanced applications.

…