2
Device Fabrication and Characterization Techniques

This chapter will give an overview of used techniques to fabricate organic transistors. In order to achieve the intended outcomes, an appropriate selection of processing methods, as well as deposition and characterization techniques, is essential for every device fabrication. To make the devices more cost-effective, various solution-processed methods at low-temperature processing are used in device fabrication. Moreover, different material characterization techniques are also being utilized to perform the detailed study of thin film properties. In addition, it is crucial to understand the science and mechanism of each characterizing tool. This chapter, first demonstrates the complete process flow for fabricating OFETs, followed by discussing the mechanisms of different deposition and characterization techniques. Moreover, electrical characterization and processes to extract and calculate the crucial electrical parameters are discussed in the last section.

2.1 SUMMARY OF FABRICATION STEPS

To start the fabrication of any organic devices, one always needs to consider the cleanliness of the surroundings as organic materials are highly prone to contamination. A stable environmental condition is tried to maintain throughout the fabrication and characterization processes to obtain accurate data without getting affected by changes in humidity, temperature, etc. In this thesis, OFETs were fabricated on different rigid and flexible substrates including indium tin oxide (ITO) coated glass, ITO-coated polyethylene terephthalate (PET), and biodegradable paper substrates. Firstly, substrates were thoroughly cleaned using organic solvents before starting the fabrication process. ITO-coated glass and pieces of PET substates with size 3 cm × 4 cm were immersed in 2-propanol (IPA) and ultrasonicated for 30 minutes followed by heated on hot plate for 10 minutes at 60 °C and washed with de-ionized (DI) water. Further, the samples were immersed in Acetone and followed the same steps as described earlier. In similar way, in the final stage the samples were immersed in methanol followed by ultrasonicating and heating on hot plate and then dried by heavy nitrogen (N2) blow to remove all dust and contaminant particles. On the other hand, paper substrates were directly cleaned by heavy N2 blow. Both flexible PET and paper substrates were pasted on bare glass as a holder to make the fabrication process more convenient and easier. Herein this work, devices with bottom gate top contact structure were fabricated. After completion of the cleaning process, bottom gate electrodes were deposited through thermal evaporation process. For ITO coated substrates, ITO acts as the bottom electrode, thus a separate deposition is not required for patterning the bottom electrode. In case of paper substrates, Silver (Ag) was deposited with thickness ~100 nm to act as bottom gate electrode by thermal evaporation at high vacuum of 10^{-6} torr. Further the inorganic oxide and natural polymer dielectrics were deposited by their corresponding processes. For HfO_2 oxide gate dielectric, atomic layer deposition (ALD) technique was used to form high quality thin film layer. For the other polymers like gelatin, chitosan, and cellulose, spin coating technique was used after preparing the solutions in suitable solvents. Further for the deposition of active layer, either neat solution of TIPS-Pentacene or blend of Polystyrene (PS): TIPS-Pentacene was utilized and deposited over gate dielectric according to the devices' functionality and requirements. Both TIPS-Pentacene and PS were prepared in toluene with

certain concentration for continuously stirring at 65 °C for 2.5 hours. Further, the blend solution was prepared with equal volume and again stirred for another 1 hour at same temperature to prepare a homogeneous solution. The prepared neat and blend solutions were drop casted over dielectric layer and immediately covered by a glass petridish to provide a suitable environment for controlling the solvent evaporation, which eventually help in forming a proper crystal of semiconductor. Top source/drain gold (Au) contacts were patterned through a shadow mask containing 72 no. of transistors and it was attached on the active layer perpendicular to the crystal direction. Finally, Au was deposited using thermal evaporation process at high vacuum of 10^{-6} torr. In a single substrate, the width (W) of the transistors is varied from 500 to 4000 µm with a constant length (L) of 150 µm. However, W of the transistors with TIPS-Pentacene and their blend are determined from the area covered by crystals and L is from their corresponding direction. In addition, to measure the gate capacitance density (C_i) and leakage current density (J), similar processing techniques were used to fabricate metal-insulator-metal (MIM) and metal-insulator-metal-semiconductor (MISM) structures on the same substrate, which are also important to study the suitability of dielectric properties in transistors. Figure 2.1 shows the device schematic; various substrates used in fabrication along with the shadow mask used for patterning source and drain top contact.

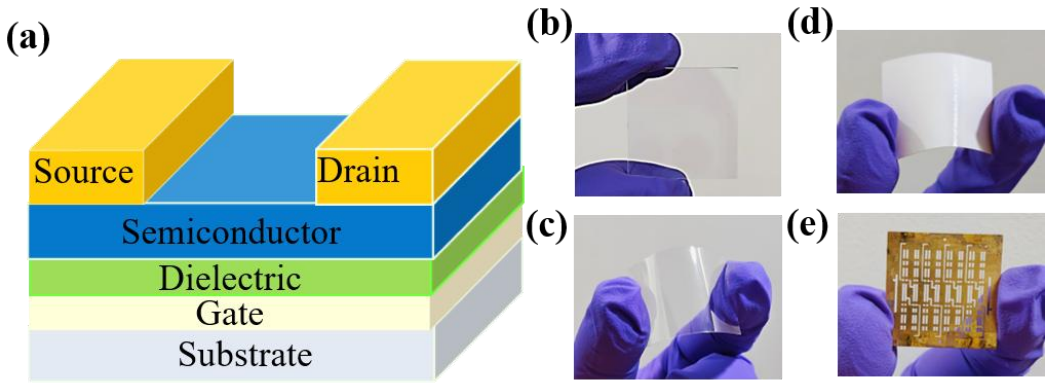


Figure 2.1 : (a) Device schematic with top gate bottom contact structure. Digital image for various substrates ITO-coated glass (b), ITO-coated PET (c), paper (d); and shadow mask containing 72 transistors for top contact patterning (e).

Various electrical and material characterization techniques were utilized during and after the fabrication process to optimize various thin film and device parameters. During the fabrication process, atomic force microscopy (AFM) technique using SPM XE-70 instrument from Park Systems, was used to determine the surface roughness of gate dielectrics along with observing the surface structure of crystals. The D8 advanced system manufactured by Bruker was utilized to perform the X-Ray Diffraction (XRD) measurements of active layers. In addition, Fourier Transform infrared spectroscopy (FTIR) and thermogravimetric analysis (TGA) were employed to analyse the chemical bonding in a thin film and weight loss of polymers with respect to temperature, respectively. The Keithley 4200 SCS analyzer in combination with the probe station was used to perform the electrical characterizations. The following sections discuss the basic working principle of deposition tools and analytical techniques.

2.2 VAPOR DEPOSITION TECHNIQUES

In this dissertation, various metal electrodes and dielectric layers are deposited through thermal and chemical vapor deposition techniques to fabricate the OFET devices. the deposition of these layers is performed in a controlled manner to obtain the smooth surface morphology. Thermal evaporation, a physical vapor deposition technique is typically employed for the deposition of metal electrodes Au and Ag. On the other hand, a chemical vapor deposition method named atomic layer deposition (ALD) was employed for the deposition of thin, pinhole-free high-k inorganic oxide gate dielectric (HfO_2). The working mechanisms of both deposition techniques are discussed thoroughly as follows.

2.2.1 THERMAL EVAPORATION

The thermal evaporation technique is regarded as a traditional physical vapor deposition method for thin film or metal deposition. Figure 2.2 illustrates the operational principle of a vacuum thermal evaporator along with the digital photograph of the instrument from Semicore employed for the deposition of metal contacts. In this process, the source material undergoes resistive heating and transforms to a gaseous phase once it has crossed the melting point. The gaseous atoms then traverse towards the cool substrate and condense on it to form the thin film for respective metals. This process is generally conducted in a high vacuum environment (1.5×10^{-6} torr), thus high vacuum condition is achieved by pump before starting the deposition process. The high vacuum helps in achieving a long mean-free path for source materials which can travel to the target substrate without colliding with any unwanted particles, facilitating high purity in metal deposition. In this method, a sufficient quantity of metal is placed on the tungsten boat, which is then heated by a strong electric current generated by the power source. The tungsten boat associated with a power supply is positioned at the bottom, while the targeted samples for film deposition are fixed on top of the chamber and directed toward the source material. Both Ag and Au electrodes were deposited using this system as bottom and top electrode respectively. In general, the Ag thickness was around 100nm while the source/drain electrode thickness was considered to be ~150-200 nm. The thickness is confirmed by the stylus-based profilometer.

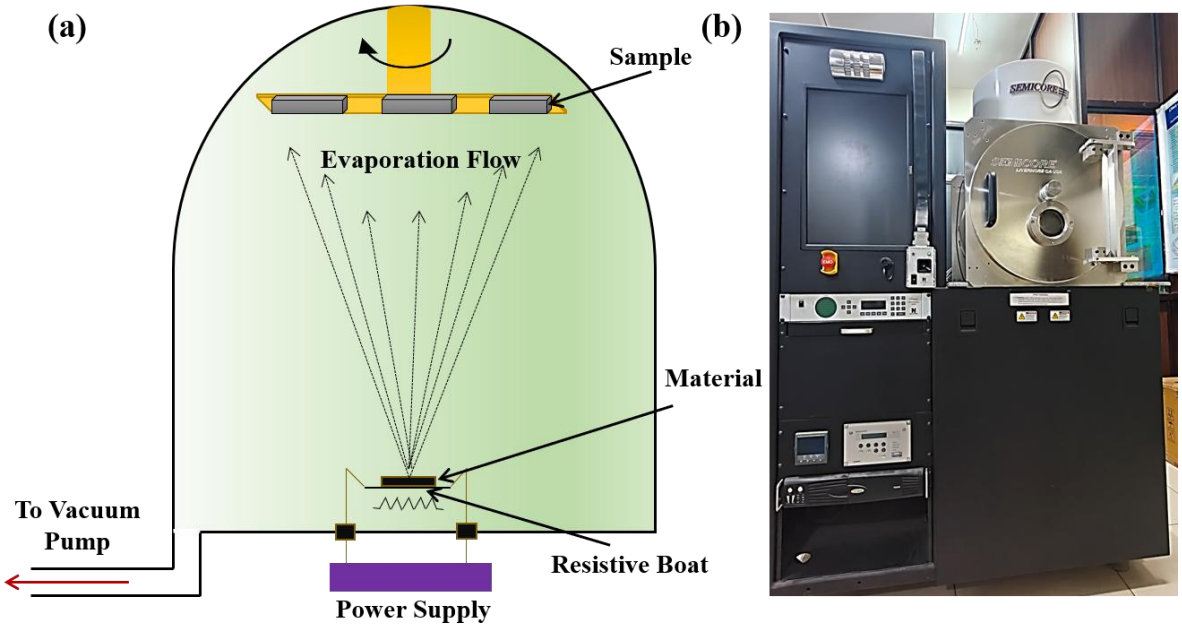


Figure 2.2 : Thermal Evaporation System: graphical illustration of the working principle (a), and image of the used Semicore thermal evaporation system (b).

2.2.2 ATOMIC LAYER DEPOSITION

Another chemical vapor deposition technique, atomic layer deposition (ALD) is employed to deposit thin film using gas phase chemical reaction. It is a surface-controlled layer-by-layer process where at a time one atomic layer is deposited. Different metals such as oxides, nitrides, and metals can be deposited by ALD with precise thickness. This deposition technique contains two types of precursors, and the reaction happens between the chosen material and the reactant to form the desired film. Samples are kept in an inert chamber and heated by the connecting heater according to the deposition requirements. Both the precursor valves open alternatively for a certain amount of time and allow them to reach the chamber with the help of inert carrier gas. The layers are created during reaction cycles by sequentially pulsing precursors and reactants, followed by purging with inert gas between

each pulse. The by-products produced during the reaction are pumped out from the chamber, making the system completely ready for the next iteration. The target film thickness is attained by reiterating this cycle. The self-limiting nature of the ALD process yields films with exact thickness and uniformity, regardless of surface topography variations. This process provides excellent control on thickness, yielding thin, pinhole-free, and homogeneous film over large area. This technology allows for scaling down the devices to smaller dimensions, supporting the reduction of power consumption of transistors. Figure 2.3 demonstrates the film-forming mechanism of ALD with the actual image of the used thermal ALD system in this experiment from. In this work, inorganic oxide layer HfO_2 was deposited for 40 nm thickness using two precursors named tetrakis-dimethyl-amidohafnium (TDMAH) and water at 100 °C. The thickness of 40 nm was attained by conducting the ALD system for ~370 cycles.

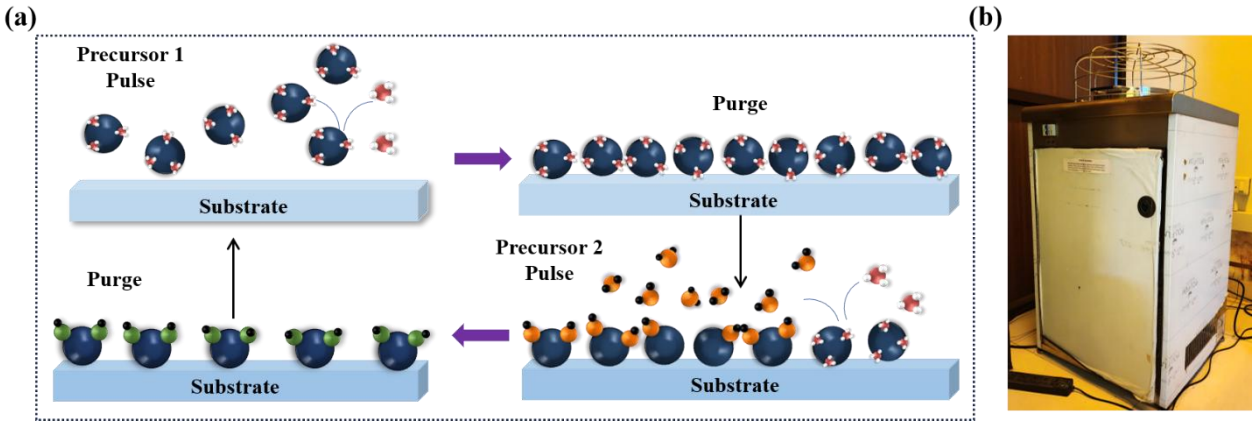


Figure 2.3 : (a) Complete process flow in the ALD system for film formation and (b) image of used thermal ALD system with model no: savannah S-200 from Cambridge nanotech.

2.3 SOLUTION PROCESSING METHODS

Solution processing methods are the most promising deposition strategy for the production of low-cost organic electronics. In this process, materials are dissolved in a suitable solvent to form the solution and then deposited using appropriate technique for thin film formation. Nowadays, number of solution processing methods such as spin coating, drop casting, dip coating, blade/bar coating, printing, etc. are being employed to fabricate cost-effective organic transistors. In this study, spin coating method was used for dielectric coating. On the other hand, drop casting technique was used for active layer deposition.

2.3.1 SPIN COATING

Spin-coating is an easy and cost-efficient method for the deposition of thin films on a planar substrate. Organic dielectrics and semiconductors can be deposited through this process with uniform thickness ranging from few nanometers to micrometers. This method involves four steps: dispensing of the solution over the substrate, spin-up, spin-off, and evaporation of residual solvent. Firstly, material is dissolved in a suitable solvent to prepare the solution and then dispensed over the substrate with an adequate amount. The substrate is then rotated at a particular speed, time, and acceleration to distribute the solution thoroughly using the centrifugal force, which covers the complete area. Further, the coated sample is annealed to remove the residual solvents, and finally a uniform thin film is formed with desired thickness. The quality of deposited film is dependent on various factors including surface property of the substrate, viscosity of the solution, material concentration, boiling point, etc. Moreover, the thickness can be controlled by adjusting the process parameters such as rotation speed, acceleration, and duration. Film deposited at higher rotating speed resulting in lowering the thickness due to higher centrifugal force and fast evaporation of solvent. On the other hand, a thicker film is obtained or the solution with higher concentration due to high its viscosity. In our study, most dielectrics were deposited using this process with different rotation speeds. The deposition of TIPS-Pentacene is generally avoided to deposit through this process as the

whole material flies off very quickly and does not get enough time to form the crystals. Polymer dielectrics such as gelatin, chitosan, and cellulose were deposited by spin coating method on various substrates like glass, plastic, and paper. Different rotation speeds varying from 1000-300 rpm for 30/60s were used in this study. Moreover, the polyvinyl alcohol (PVA) planarization layer on a paper substrate is also deposited by spin coater. Figure 2.4 (a) shows the graphical illustration of all four stages of spin-coating process. The digital image of the used model for spin-coating is shown in Figure 2.4 (b) (Model No: HO-TH-OSC from HOLMARC).

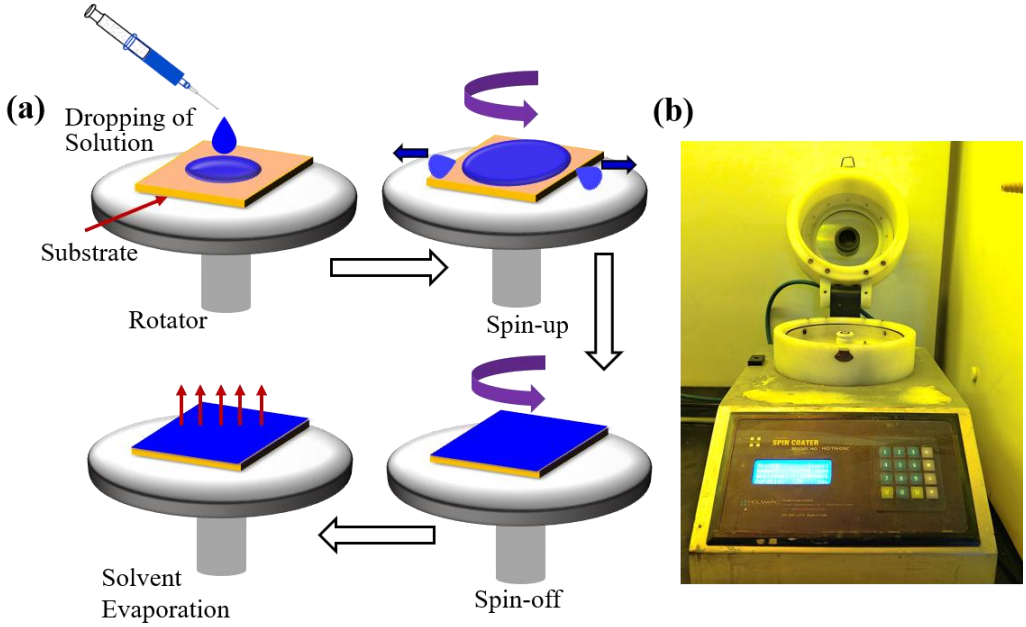


Figure 2.4 : (a) Schematic illustration of the spin coating technique to form the thin films, and (b) digital depiction of the HO-TH-OSC spin coating apparatus from HOLMARC.

2.3.2 DROP CASTING

Another simple and easy solution-processed method drop casting is employed for thin film depositing. This method involves simply dispensing the solution over the substrate which subsequently self-spreads to form film without the need of any deposition apparatus. The desired film is formed after evaporation of excess solvent. The main advantages of this process are easy processing and no requirement of any instrument to deposit. However, this process has less control over the film's uniformity, thickness, and reproducibility. Though this technique has some serious demerits, this process is quite suitable where slow evaporation of solvent is needed. Here, the solvent is slowly evaporated and gets enough time for molecular arrangement, leading to a highly crystalline film for semiconductors. In addition, the thickness and quality of the film depend upon the concentration of solution, boiling point, and evaporation rate. In some cases, external temperature is provided to enhance the rate of evaporation to form the desired film.

In our work, drop drop-casting method is utilized to deposit the active layers. Both the pristine and blend of semiconductor: polymer solutions were deposited using this process. The solution was poured over the flat substrate and immediately covered by a glass pteridish to provide a closed environment to slow down the drying process for high-quality film deposition. Further, the solvent is gradually evaporated resulting in a high crystalline semiconductor film with a thickness around 1-2 micrometers. Difficulty in controlling the orientation of crystals is one of the major concerns in this process. Hence, the crystal direction is carefully observed during the pattering of top source/drain contacts. Generally, the pattern shadow mask is pasted perpendicular to the crystal to make a direct connection between source and drain contacts. Figure 2.5 (a-c) shows the drop-casting technique. The optical microscope image of the obtained semiconductor crystals is shown in Figure 2.5 (d). TIPS-

pentacene films deposited by drop casting show superior crystallinity to alternative deposition methods, including spin-coating and spray coating (Raghuwanshi, Bharti, & Tiwari, 2016), (Deepak Bharti et al., 2017), (Park et al., 2007).

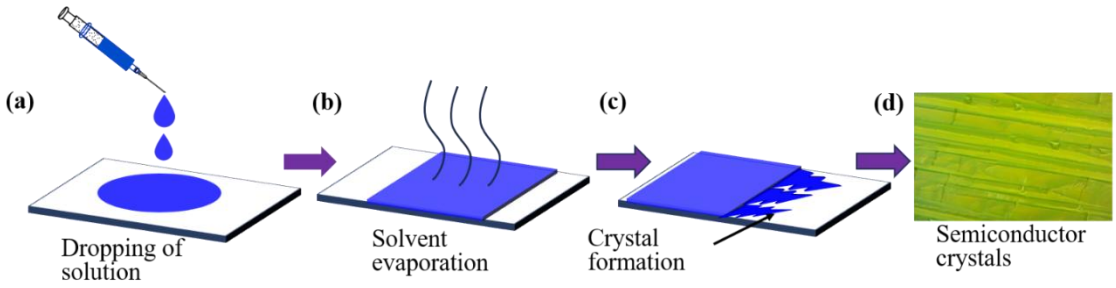


Figure 2.5 : Illustration of drop-casting method for semiconductor layer, dropping of solution (a), self-spreading and solvent evaporation (b), crystal formation (c), and digital image of the deposited semiconductor crystals (d).

2.4 MATERIAL AND SURFACE CHARACTERIZATION TECHNIQUES

The detailed analysis of surface and material properties of deposited thin films is crucial in understanding their suitability in OFET performance. This section will give a brief overview of the working mechanism of used characterization techniques in this dissertation.

2.4.1 SURFACE PROFILING

For thin film devices, it is crucial to determine the thickness for optimum performance in transistors. In this regard, surface profiling is used to identify the thickness of deposited film on different substrates. Linear surface profiling is the easiest method for assessing the surface profile of thin films. The surface profilometer is equipped with a crucial component called a stylus or shar tip, which continuously exerts a constant force on the film's surface during the investigation. A computerized feedback system is interconnected with the profilometer, which records and monitors the constant force. The stylus first moves downward direction and comes closer to the surface then it scans the surface from one location to another. As the stylus navigates, it encounters hills and valleys in the film surface which exerts a force depending on the surface and sent to the profiler. The applied constant force varies with its movement, and this deviation is captured by the closed feedback loop.

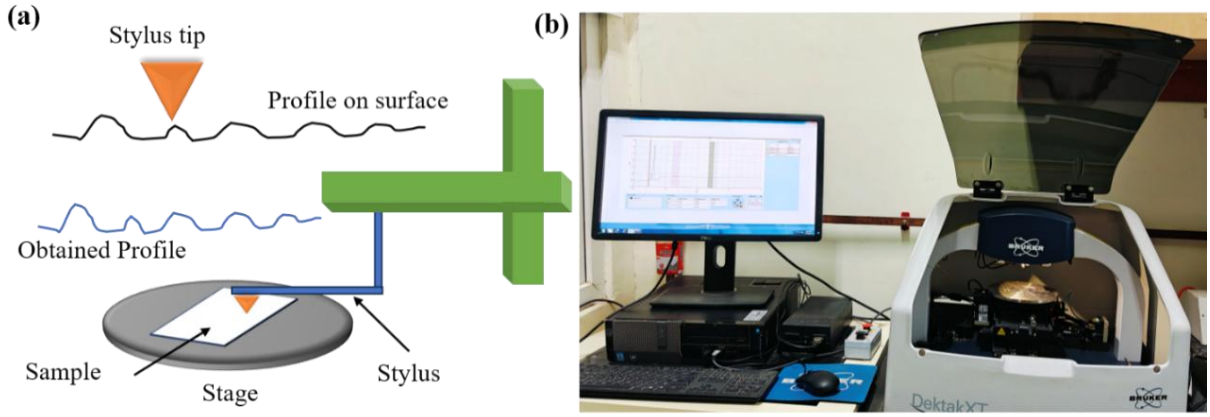


Figure 2.6 : (a) Illustration of the working process for stylus profilometer, and (b) digital picture of complete setup for surface profiler system.

Figure 2.6 (a) shows the basic mechanism of linear profilometer. This type of surface profiling technique is commonly referred to as contact-type method. Despite the benefits, the contact profiling has some limitations, including the risk of stylus damage while evaluating rough films and restricted scanning speed due to direct touch to the films. In contrast, non-contact surface profiling is also available where light is illuminated to determine the surface profiles without requiring any physical contact, facilitating quicker measurements and minimizing the

chance for equipment damage. In this study, the DekTak-XT surface profiler from Bruker was used to measure film thickness. The digital picture of the surface profiler with feedback system is shown in Figure 2.6 (b). During this study, system employs the stylus radius of 2 µm with scan times ranging from 20 to 30 seconds and ranges from 1000 to 3000 µm. To get a high accuracy, film thickness was measured for a minimum 3-4 locations and their average value was estimated as thickness of the deposited films.

2.4.2 X-RAY DIFFRACTION

X-ray diffraction is one of the most widely used analytical techniques to determine the crystallinity and composition of any material. It helps to study the crystal structures, recognize unknown substances, the determination of unit cell diameters, the analysis of desired orientations in polycrystalline materials, and calculate the stress and defects of the material. The structure of atoms can be identified in larger crystals, whereas the composition, crystallinity, and phase purity of samples are determined from the small-size crystals. XRD mainly consists of three key components: X-ray source, the sample holder, and the detector. X-rays are produced in a cathode ray tube where high voltage is applied to heat the filament. The heated filament emits electrons and accelerates on applying the high voltage to them. These accelerated electrons collide with the target material (commonly copper) and dislodged electrons from the inner shells, producing characteristic X-rays, such as CuKα (wavelength 1.5418 Å), which are commonly used for diffraction studies. The sample holder holds the specimen and maintains a specific orientation to obtain correct analysis. A constructive interference results in a peak in the collected intensity, when the X-ray incident on the material satisfies Bragg's Equation ($n\lambda = 2d\sin\theta$). The rotating detector measures the intensity of the reflected X-rays. Further, it was processed and converted to the count rate, which is eventually the output of the system. In general, a thick film is needed for accurate X-ray analysis. The non-destructive nature and simple sample preparation make this approach superior to the alternative approaches. Figure 2.7 (a) presents a schematic representation of a fundamental X-ray diffractometer. In this study, X-ray diffraction experiments were conducted using the Bruker D8 Advanced.

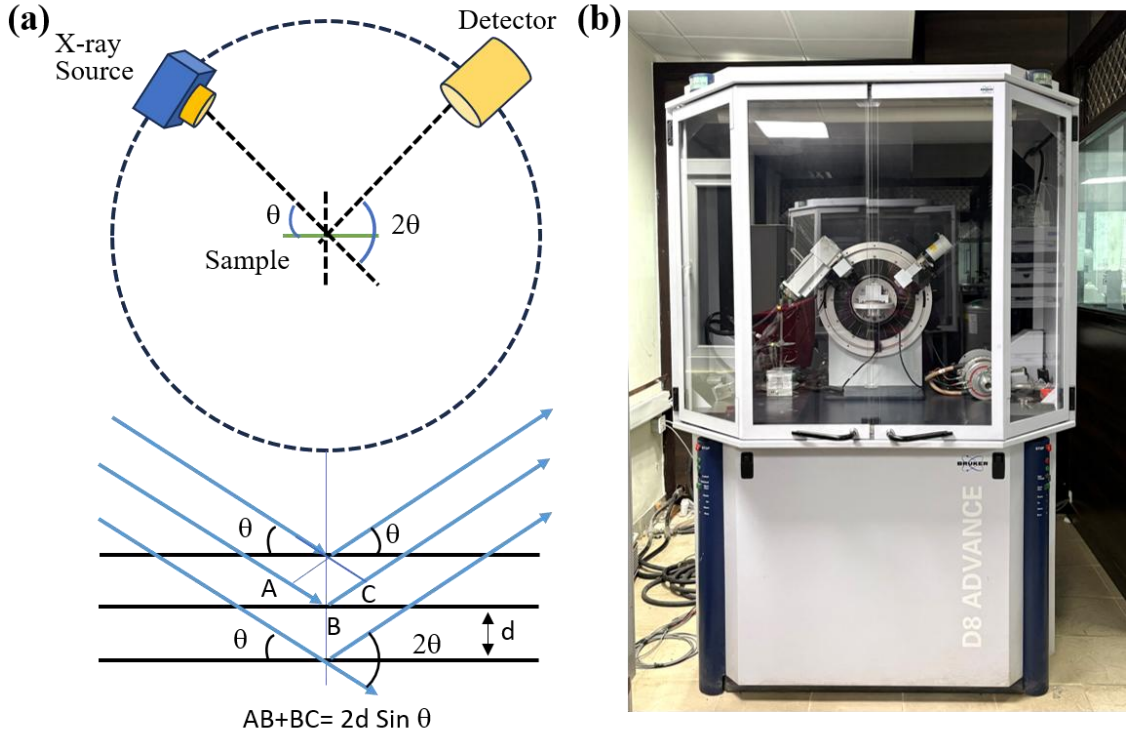


Figure 2.7 : (a) Schematic representation of the functional concept of XRD measurement system, and (b) a digital picture of the XRD system used in this investigation.

2.4.3 ATOMIC FORCE MICROSCOPY

Atomic force microscopy (AFM) is a sophisticated advanced imaging technique for analyzing the surface morphologies of deposited thin films in nanoscale range. Along with the three-dimensional morphology of films, AFM also offers a wide range of surface measurements based on users' requirements. Additionally, images were produced at atomic or nanoscale resolution, incorporating height information at angstrom scale with minimal sample preparation. The fundamental idea of AFM involves the deflection of a cantilever over the sample surface. AFM consists of a cantilever with a sharp tip and the surface of the sample was scanned for a particular area. When the tip moves toward the sample, it encounters an attractive force that draws the cantilever closer to the surface. However, as the tip approaches the sample surface sufficiently, a repulsive force is encountered between the sample and the tip, resulting in a deflection of the cantilever away from the surface. A continuous laser beam is incident for monitoring and recording the deflection. Whenever there is a deflection in the cantilever, the trajectory of an incident laser beam is altered, and corresponding changes are captured by position-sensitive photodiode (PSPD). During the measurement, the tip oscillates within the selected area and traverses through hills and valleys, resulting in vertical up-down motion of the cantilever. The deflection of the cantilever fluctuates based on the surface characteristics of the sample, leading to alterations in the direction of the reflected beams, which are observed by the PSPD. In addition, a reference point is established by maintaining a constant distance between the sample and the tip, which is continuously monitored and regulated via a closed feedback loop. The AFM system displayed a precise image of the surface, representing the surface shape and numerous surface properties. The graphical representation of AFM working principle is shown in Figure 2.8 (a). This work utilized the SPM XE-70 from Park Systems to record the surface morphology of the deposited thin films, which is shown in Figure 2.8 (b). In this dissertation, mainly surface roughness of gate dielectric layers was measured through AFM to study their suitability for semiconductor deposition and good dielectric: semiconductor interfacing.

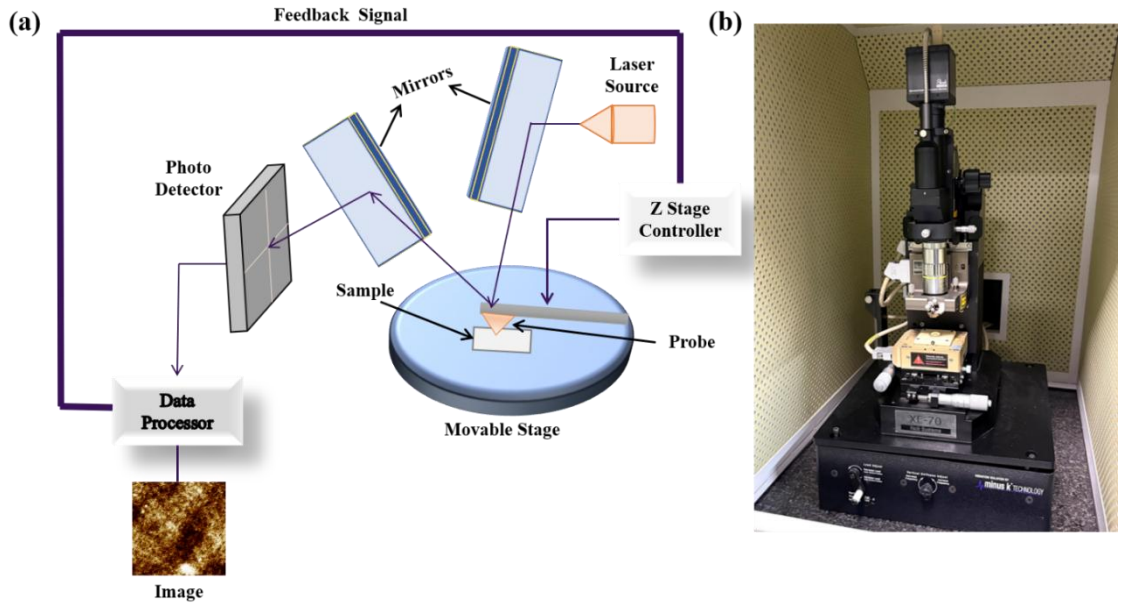


Figure 2.8 : (a) Graphical illustration of the operating mechanism of AFM system, and (b) picture of the used AFM system from Park Systems with model no. of SPM XE-70.

2.4.4 FOURIER TRANSFORM INFRARED SPECTROSCOPY

The Fourier Transform Infrared (FTIR) spectroscopy is a powerful analytical technique that is mainly used to identify molecular structures and study chemical bonding by measuring the infrared absorption of materials. It also provides information about intermolecular and intramolecular chemical bonding between two molecules, and functional groups present in any organic materials [Reis et al., 2006, Tsai et al., 2013]. Depending upon the excitation wavelength and molecular transitions, infrared spectroscopy is different than UV-Vis spectroscopy.

Vibrational transitions occur in the infrared area, whereas UV-Vis spectroscopy exhibits electronic transitions in the ultraviolet-visible range. The key components of a typical FTIR instrument are a sample holder, source and detector unit, beam splitter, and movable and fixed mirrors. Figure 2. 9 (a) shows the operating mechanism of FTIR. During the operation, the source unit generates an infrared light which is firstly passed through a beam-splitter to split into two portions. Half of the beam reaches the fixed mirror, while the other half is directed to a movable mirror at a constant velocity. These split beams are reflected back and recombined to produce an interference pattern. This pattern is subsequently directed to the sample, and the corresponding transmitted portion is passed to the detector. The transmitted portion is compared with the reference sample beam spectrum at the detector, ultimately yielding the FTIR spectrum of the sample as a function of wavenumber. This analysis technique is versatile, non-destructive, and applicable to both thin films and powders, which can identify the polymer compositions and material purity. In this study, FTIR spectroscopy of thin film was conducted using the VERTEX 70v from Bruker. The image of the FTIR spectroscopy apparatus is shown in Figure 2.9 (b).

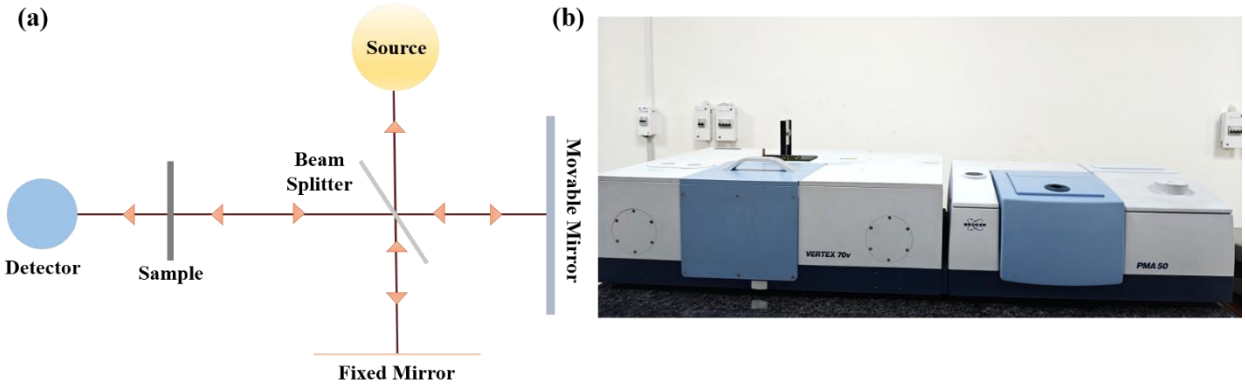


Figure 2.9 : (a) Schematic representation of operating mechanism of FTIR, and (b) image of the FTIR setup.

2.4.5 THERMOGRAVIMETRIC ANALYSIS

The investigation of thermal stability is crucial for any organic material to study its suitability in fabrication. In this regard, thermogravimetric analysis (TGA) is employed to quantify the variations in the mass of a material with respect to temperature or time inside a controlled environment. This measuring phenomenon gives information regarding physical processes including phase transitions of a material alongwith absorption, and desorption of temperatures. In addition, chemical informations like chemisorption, breakdown with temperature, and solid-gas reactions (e.g., oxidation or reduction) are also provided by TGA. The key components of a TGA are a precision balance, a furnace, and a temperature control device.

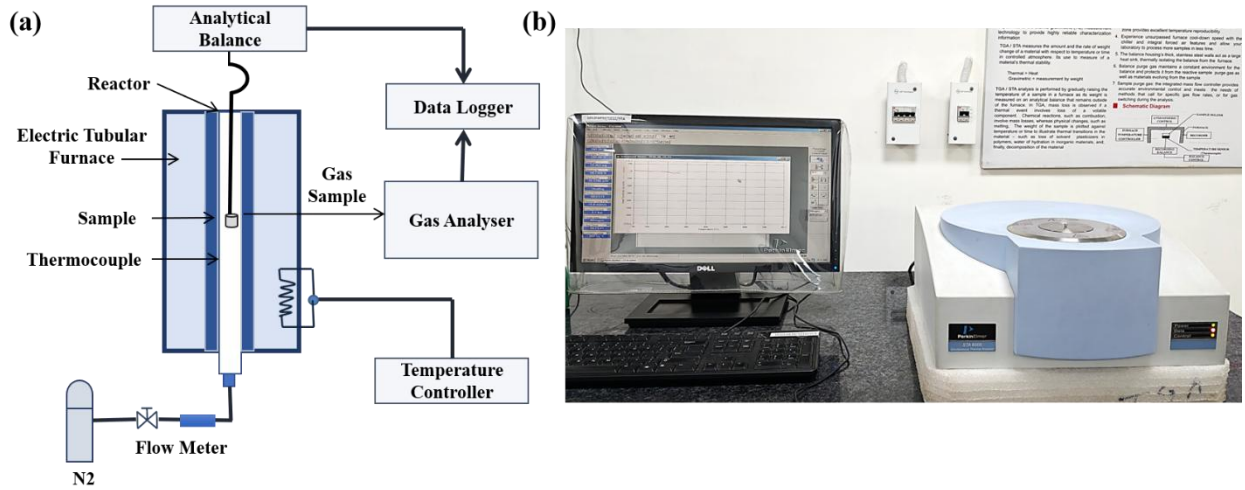


Figure 2.10 : (a) Schematic of the operating mechanism of TGA, and (b) digital image of complete setup for TGA (STA6000) used in this study.

A sample is positioned on a microbalance inside the furnace, and the system is configured to heat the sample at a specified rate in an inert atmosphere. With increasing the temperatures at a constant rate for a known initial weight, the material experiences physical or chemical transformations, leading to variations in mass which are recorded as a function of temperature. The microbalance is highly sensitive which consistently measures mass variations throughout the measurements. TGA offers insights into the thermal stability, composition, and degradation mechanisms of materials. It is widely used in polymer analysis, material characterization, and investigation of composites, providing information about moisture content, decomposition temperatures, and remaining quantity. In this study, the TGA was performed using a simultaneous thermal analyzer (STA) from Perkin Elmer company with model ID STA6000, which is shown in Figure 2.10 (b). STA has the capability to perform both TGA and differential scanning calorimetry (DSC) measurements.

2.5 ELECTRICAL CHARACTERIZATION

After successful fabrication of devices, electrical characteristics of transistors were observed to study their performance. For organic devices, environment has a huge influence on their performance. In our study, all the devices were characterized in ambient conditions through Keithley 4200 parameter analyzer. The accurate measurement of electrical characteristics is desirable to estimate the important device parameters. The parameter analyzer is capable of providing current-voltage (*I-V*), capacitance-voltage (*C-V*), and capacitance-frequency (*C-f*) measurements in the Keithley Interactive Test Environment (KITE). Devices were positioned and probed at the Cascade Microtech PM5 probe station and it was connected to the measuring unit through a coaxial cable. The experimental setup for electrical characterization is shown below.

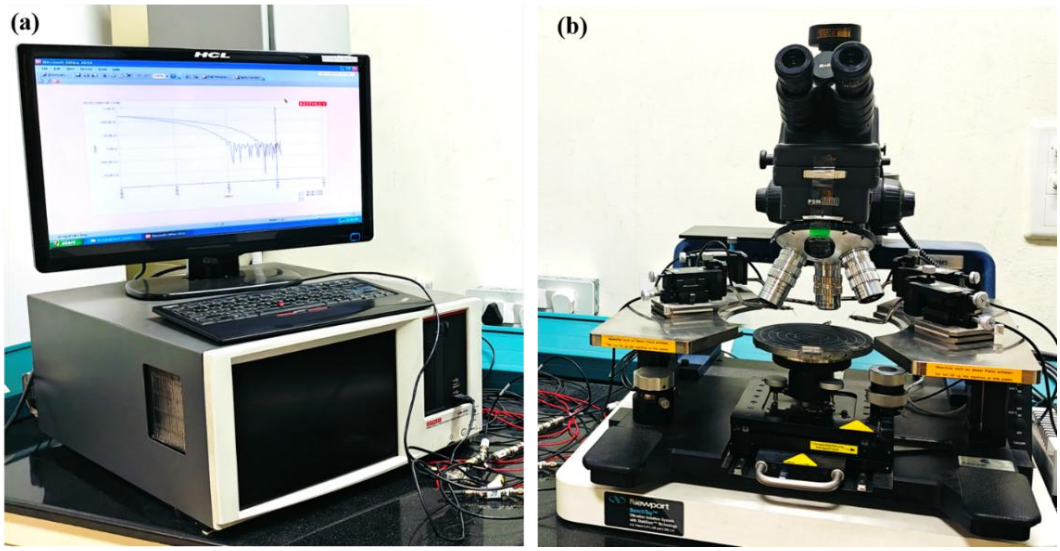


Figure 2.11 : Experimental setup for electrical characterization: (a) Keithley 4200-semiconductor parameter analyzer, and (b) probe station from Cascade Microtech PM5.

2.5.1 Extraction of Electrical Parameters

The effectiveness of an electronic device is investigated through its electrical characteristics. Each device has essential unique electrical properties that signify its quality, and depending on them it can be evaluated whether a device is performing well or not. These parameters are influenced by several factors such as material selection and manufacturing techniques. To compare the OFETs fabricated with different materials and processes, it is crucial to determine some parameters or figures of merits. The key electrical parameters that evaluated the performance of OFETs are field-effect mobility (μ), threshold voltage (V_{TH}), sub-threshold slope (SS), current on-off ratio (I_{on}/I_{off}), and interface trap density (D_{it}). All these parameters are influenced by numerous factors starting from material properties, film properties, device

structure, processing techniques, and interface qualities. The selection of suitable material results in high performance in transistors. Moreover, the environment has a huge impact on transistor performance since organic materials are very sensitive to humidity and other external stimuli. Thus, environmental condition is also considered while extracting the parameters. These parameters are extracted from the electrical characteristics of the transistors. Transfer and output characteristics are the two basic characteristics of a transistor. For transfer plot, changes in drain current (I_{DS}) is measured with respect to gate voltage sweep (V_{GS}) for a constant drain voltage (V_{DS}). On the other hand, the output plot refers to the variation in I_{DS} as a function of V_{DS} for different step values of V_{GS}, which is important to investigate the saturation regime of a transistor. Figure 2.12 (a) and (b) show the typical transfer (I_{DS} vs V_{GS}) and output (I_{DS} vs V_{DS}) plots of a p-channel OFET. The linear and saturation regime of OFET is represented in the output plot. Most of the electrical parameters are extracted from the transfer plot. For an OFET, μ is one of the most crucial parameters to define the performance efficiency of any organic transistors. It measures the average charge carrier drift velocity per unit of electrical field. This can be extracted in both linear and saturation regimes from their respective I_{DS} equations. However, this thesis mainly focuses on the extraction of μ values in the saturation regime as given below:

$$\mu_{\mathrm{Sat}} = \frac{2L}{WC_{\mathrm{i}}}\left(\frac{\partial\sqrt{I_{\mathrm{DS,Sat}}}}{\partial V_{\mathrm{DS}}}\right)^2 \qquad (2.1)$$

where C_i is gate-capacitance density, width and length of the semiconductor channel are termed as W and L, V_{GS} refers to the voltage applied between gate and source, V_{DS} refers to the voltage between drain and source, and the threshold voltage is referred as V_{TH}. The linear fit in the saturation regime is shown in Figure 2.12 (a). This method is used to evaluate the mobility for all the studies included in this dissertation. Despite its simplicity, this methodology experienced two major drawbacks. One is the contact resistance parameters are not considered during the extraction and other one is device geometry highly influenced these values. Moreover, it can be seen the μ values are dependent on C_i extracted for a particular frequency. The incorrect extraction of C_i might result in overestimation and underestimation of obtained values. To avoid the frequency dependency, process transconductance ($k_p = \mu \times C_i$) was determined for the accurate comparison among devices as shown in the below equation:

$$k_{\mathrm{p}} = \frac{2L}{W}\left(\frac{\partial\sqrt{I_{\mathrm{DS,Sat}}}}{\partial V_{\mathrm{DS}}}\right)^2 \qquad (2.2)$$

In addition, average mobility values are highlighted in these studies. Instead of claiming high mobility, our work mainly focuses on the investigation of the suitability of natural polymers in OFETs and their stability in harsh environments. Another crucial parameter for OFET is threshold voltage (V_{TH}), which is important for operating voltage. Low V_{TH} values are preferred for low voltage operation of the device. It defines the minimum value of V_{GS} required to accumulate sufficient charge at the semiconductor: dielectric interface to turn on the device. This value is generally extracted from the maximum slope of $\sqrt{I_{DS}}$ vs. V_{GS} plot of the transfer characteristics in saturation regime along with the extraction of μ. The X-intercept of this plot is referred to as V_{TH}. To achieve lower V_{TH} and lower voltage operation, a higher C_i value. Various dielectrics like high-k inorganic or inorganic/organic bilayer hybrid gate dielectric combinations were used to achieve this high C_i value (Sachin Rahi et al., 2022). I_{on}/I_{off} is another important factor which is defined as the I_{DS} ratio between 'on' and 'off' states of the transistor. I_{on} is determined from the I_{DS} at $V_{DS}= V_{GS}= V_{DD}$, whereas the I_{off} at $V_{GS}= 0$ V and $V_{DS}= V_{DD}$. For high-performance devices, it should be high so that both 'on' and 'off' states are distinguishable, confirming the transistor capability for high current modulation. I_{on} is primarily influenced by mobility of the semiconductor, contact resistance at the gate and drain electrodes, and the capacitance of the gate dielectric, and consequently it increases as these factors are enhanced. On the other hand, I_{off} is primarily determined by the bulk conductivity of the semiconductor and the gate leakage current.

Therefore, it is feasible to decrease the off-currents through the proper choice of gate material, optimization of the film thickness, parasitic leakage suppression, interface engineering, and patterning of gate electrodes.

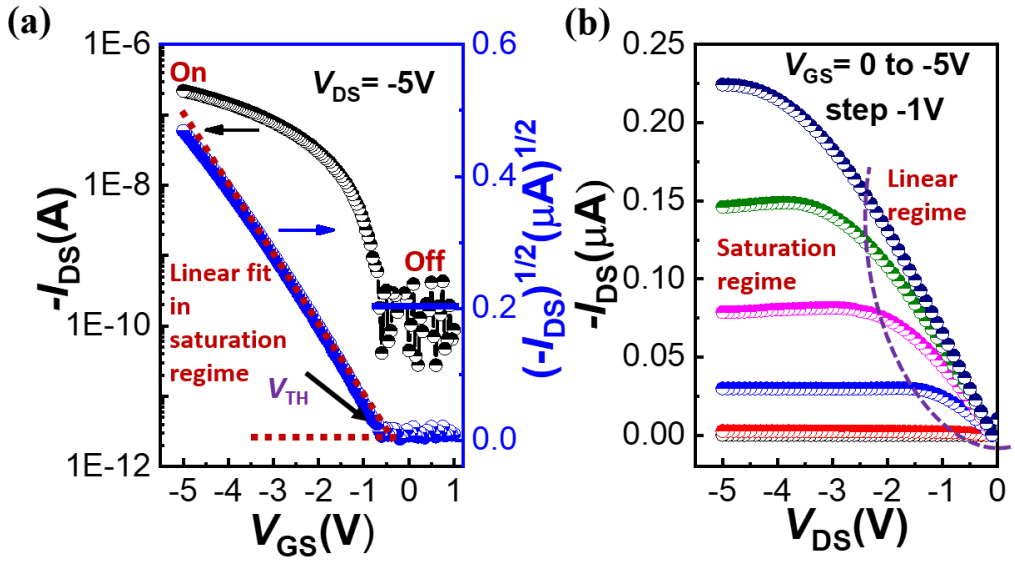


Figure 2.12 : Typical (a) transfer and (b) output characteristics of a p-type OFET for analyzing the device parameters.

SS is useful to determine the switching speed of any transistor. It defines how sharply the devices are turned on from the off state and is described as the requirement of minimum V_{DS} to enhance one decade of I_{DS}. Transfer plot having a sharper slope indicates faster device operation and lower *SS* value, which can be defined by the following formula:

$$SS = \frac{\partial V_{GS}}{\partial(log_{10}(I_{DS}))} \qquad (2.3)$$

The minimum theoretical *SS* value for any transistors is 60 mV/dec. In general, a lower value of *SS* is preferable to turning on the device at a smaller V_{GS} value. Moreover, interface trap D_{it} is another crucial parameter to define the number of trapping densities at the dielectric semiconductor interfaces. In general, lower trapping sites are advantageous to operate the device at high charge carrier conductions. D_{it} is calculated by following the formula (Held et al., 2015)

$$D_{it} = \frac{C_i}{q}\left[SS\frac{log(e)}{kT/q} - 1\right] \qquad (2.4)$$

where q is electronic charge, k is Boltzmann's constant, and T is temperature at kelvin. A bad interface leads to slower devices whereas a high-quality interface helps towards performance and speed of the devices. An appropriate selection of semiconductor: dielectric interface is needed to achieve high performance.

2.5.2 Electrical Stability

Apart from electrical parameters, stability in transistor performance is crucial for utilizing these organic transistors in real-world applications. It is broadly classified into two types: operational and environmental stability. One of the primary concerns in OFETs is operational stability for their use in circuit and sensing applications. Throughout the operation, devices are exposed to a variety of external stimuli, such as electrical, thermal, mechanical, and humidity or environment. Stability is dependent upon a variety of factors, including the type of semiconductor material used, the processing techniques employed, and the structure of the device. This can be evaluated by performing various experiments such as investigating hysteresis, multiple scanning of transfer characteristics, bias-stress, cyclic, mechanical, and shelf-life stability. OFETs exhibit a current hysteresis during the forward and backward sweep of the transfer plot, causing instability

in device performance. This might occur due to trapping of charge carriers and is useful for non-volatile memory characteristics. However, minimum or negligible hysteresis is desirable for circuit applicability. During the multiple scanning, transfer characteristics is continuously recorded for 100 scans, and their variations in terms of 'on' current, V_{TH}, μ, and SS were observed. For the most reported bias-stress studies, constant V_{GS} and V_{DS} are applied for a long duration. The drain current is shifted for applying the gate bias for such a long duration. The normalized I_{DS} (I_{DS}(t)/ I_{DS} (0)/) with time is observed, showing a decrement in current due to trapping of charge carriers in the bulk of the semiconductor, at the grain boundaries, at various interfaces like dielectric: semiconductor or the electrode: semiconductor interface. Mathematically it is given as:

$$\frac{I_{DS}(t)}{I_{DS}(0)} = exp\left[-2\left(\frac{t}{\tau}\right)^{\beta}\right] \qquad (2.5)$$

where, τ is relaxation time, which defines the charge carrier trapping time and β is stretched exponential factor indicating the involved trap distribution width (Raghuwanshi, Bharti, & Tiwari, 2016). These values were extracted by exponentially fitting the normalized drain current, further used to extract the shift in V_{TH} during the stress period from the following equation:

$$|\Delta V_{TH}(t)| = |V_{GS} - V_{TH0}|[1 - exp\left(\frac{t}{\tau}\right)^{\beta}] \qquad (2.6)$$

Where V_{TH0} refers to the initial value and ΔV_{TH} (t) determines the value at a particular time instance. In addition, cyclic stability was investigated by applying continuous voltage sweep (V_{GS}) within the operating voltage range, and the corresponding changes in I_{DS} were recorded to study how perfectly the device can switch between 'on' and 'off' states. In addition, both tensile and compressive strains are subjected to the devices for different bending radius and their effect on transistor performance was recorded. In our study, devices were subjected to a maximum of up to 200 repeated bending cycles.

2.5.3 Photo Transistor Parameters

To analyse the light sensing capability in OFETs, LEDs were used as light sources to emit blue (λ~460 nm) and UV (λ~365 nm) lights on the photosensitive TIPS-Pentacene layer. The light source was adjusted on top of the device to provide optimal illumination with maximum intensity. Transfer characteristics was measured under dark and light illumination conditions to analyse the light sensing capability of fabricated devices. Two most important parameters are extracted directly from the transfer curves, which are important to investigate the suitability of these transistors in real applications.

First important figure of merit is current modulation (P), which defines the ratio of photogenerated drain current to field-generated drain current as given below:

$$P = \frac{I_{DS,light} - I_{DS,dark}}{I_{DS,light}} \qquad (2.7)$$

Photo-responsivity (R) is another crucial parameter, that indicates the photogenerated current to the incident light density to the effective area. This parameter signifies how effectively an input light can convert to the electrical signal in the form of current or voltage and the unit is A/W.

$$R = \frac{I_{DS,light} - I_{DS,dark}}{A \times P_i} \qquad (2.8)$$

Where, $I_{DS,\,light,}$ and $I_{DS,\,dark}$ are transfer characteristics under light and dark conditions respectively, A is the effective area of the OFET, and P_i is the light intensity. In our cases, the light intensities for blue and UV lights were 2.5 mW/cm^2 and 0.6 mW/cm^2, respectively.

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