2
Literature Review

In the previous Chapter, the introduction of $2\omega-$ripple problem in the single-phase inverters have been presented. This Chapter further extends the study on $2\omega-$ripple problem in the single-phase inverters and presents a comprehensive review of the aforesaid problem. Several control techniques to mitigate the second-order ripple problem and associated challenges are discussed throughout the Chapter. The control techniques are broadly divided in the three parts, namely, passive power-decoupling techniques, active power-decoupling techniques, and a subcategory of the active power-decoupling technique nominated here as "control-oriented compensation techniques for the single-phase inverters with the front-end control capability". These techniques are thoroughly reviewed with the supporting figures of circuits and control-techniques. The mathematical analysis is presented wherever needed and the merits and challenges of the different control techniques are listed in tabular form. The Chapter is organized as follow. In Section 2.1, the calculation of minimum size of capacitance required at the DC-link to absorb the $2\omega-$ripple and the impact of $2\omega-$ripple on the system are discussed. Section 2.2 discusses about the single-phase inverters used for the renewable or alternative energy applications and the effect of $2\omega-$ripple on the systems having inverter loads. Several techniques for the $2\omega-$ripple mitigation are classified and discussed under the Section 2.3. The Section 2.4 presents a conclusive discussion and challenges based on the reviewed $2\omega-$ripple control techniques.

The second-order harmonic ripple poses several adverse effects on the system components, sources and control algorithm which lead to various challenges related to reliability, stability, durability, efficiency, cost, size and weight of the system. The impact of $2\omega-$ripple on the system and safety constraints and measures are discussed in the following section.

2.1 MINIMUM SIZE OF CAPACITANCE REQUIRED AT THE DC-LINK TO ABSORB $2\omega-$RIPPLE AND CONSEQUENCES OF $2\omega-$ RIPPLE ON SYSTEM

For an ideal inverter, the instantaneous values of input power and output power must be equal. However, in actual scenario, there is the power mismatch between the instantaneous values of DC power and AC power; the pulsating nature of AC power causes the pulsation in input power.

2.1.1 Minimum Size of Capacitance Required at the DC-link to Absorb $2\omega-$Ripple

Suppose an inverter supplies an AC load at ω rad/s. The mathematical representation of such systems is as follows [Ge *et al.*, 2018],

$$v_{ac} = V_m cos(\omega t),\ \ i_{ac} = I_m cos(\omega t - \theta) \tag{2.1a}$$

$$v_{ac} i_{ac} = 0.5 V_m I_m cos\theta + \underline{0.5 V_m I_m cos(2\omega t - \theta)} \tag{2.1b}$$

$$p_{ac} = P_o + \underline{p_r} \tag{2.1c}$$

Here v_{ac} and i_{ac} are the instantaneous output AC voltage and output AC current of the inverter. θ is the displacement angle. The subscript m stands for the maximum value of v_{ac}/i_{ac}. The underline part of (2.1) is 2ω-power ripple pulsating over the average DC offset. Therefore, the rectification

or inversion in a DC-AC power converter causes a reflection of 2ω-ripple at the DC-terminal. In the Fig. 2.1(a), this phenomenon is depicted.

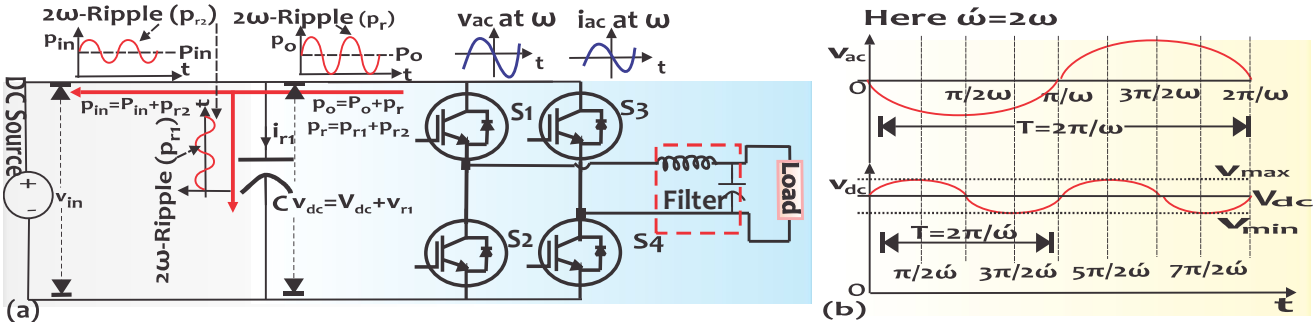

Figure 2.1 : (a) Background of 2ω-ripple in single-phase inverter (b) Waveform of AC output voltage and DC-link voltage

In Fig. 2.1(a), suppose v_{dc} is the instantaneous voltage at DC-link and i_r is the current through DC-link capacitor (C) and assume 2ω-ripple passes through the capacitor only i.e. $p_r = p_{r1}$ and therefore no ripple propagates to the input i.e. $p_{r2} = 0$ then the instantaneous power of capacitor is,

$$p_r = v_{dc} i_r \tag{2.2a}$$

$$p_r = (V_{dc} + v_r) i_r = V_{dc} i_r + v_r i_r \tag{2.2b}$$

Here V_{dc} is the average voltage of DC-link and v_r is 2ω-ripple voltage. For large value of C, the value of v_r in (2.2) is negligible, this implies that $v_r i_r << V_{dc} i_r$. This gives,

$$p_r = V_{dc} i_r \tag{2.3}$$

Using the value of p_r from (2.1) in (2.3) gives,

$$i_r = \frac{0.5 V_m I_m cos(2\omega t - \theta)}{V_{dc}} = \frac{P_{rms} cos(2\omega t - \theta)}{V_{dc}} \tag{2.4}$$

Here *rms* stands for root-mean-square. Also,

$$i_r = C \frac{dv_r}{dt} \tag{2.5}$$

Using (2.4) and (2.5) gives,

$$dv_r = \frac{P_{rms}}{C V_{dc}} cos(2\omega t - \theta) dt \tag{2.6}$$

Integrating (2.6) from both sides and using upper and lower limits in it from Fig. 2.1(b) gives,

$$\int_{v_l}^{v_u} dv_r = \int_{\frac{\pi}{4\omega}}^{\frac{3\pi}{4\omega}} \frac{P_{rms}}{C V_{dc}} cos(2\omega t - \theta) dt \tag{2.7a}$$

$$\Delta v = v_u - v_l = \frac{P_{rms}}{2\omega C V_{dc}} [sin(2\omega t - \theta)]_{\frac{\pi}{4\omega}}^{\frac{3\pi}{4\omega}} \tag{2.7b}$$

$$\Delta v = \frac{P_{rms}}{\omega C V_{dc}} cos\theta \tag{2.7c}$$

Here Δv is the peak to peak voltage ripple and subscripts u and subscript l stand for upper limit and lower limit respectively. For the given value of Δv, P_{rms}, θ and V_{dc}, the size of capacitor required at the DC-link is,

$$C \geq \frac{P_{rms}}{\omega \Delta v V_{dc}} cos\theta = \frac{P_{rms}}{\omega \Delta v V_{dc}} p.f. \tag{2.8}$$

Here $p.f.$ stands for power-factor.

2.1.2 Consequences of 2ω-Ripple on System

The low-frequency 2ω-ripple poses several problems subjected to cost, size, efficiency, reliability and stability on the system [Khajehoddin *et al.*, 2013; ZhengWei *et al.*, 2012]. This ripple forces an over-rated design of the system components and the pulsation of this ripple about DC average values further increases the peak-rating of system. Consequently, i^2r or conduction loss in the system increases. The i^2r-loss inside the E-cap causes heating of electrolyte (a complex liquid chemical) [Almeida *et al.*, 2015; Parker, able]. To restrict the DC-link voltage ripple to $\pm 1\%$, an electrolytic capacitor of $\approx 6\ mF$ is required for a 100 W-inverter operating at 60 Hz with 48 V-DC-link voltage [Krein *et al.*, 2012]. The Fig. 2.2(a) depicts that a large size capacitor among the capacitors of same voltage rating is required to decouple more 2ω-ripple. The power-density of the inductors are comparatively lesser than the capacitors [Wang *et al.*, 2011]. Therefore, 2ω-ripple affects the sizing of the inductor more in the comparison to the capacitor. Furthermore, an injection of the SHC ripple into the DC sources such as fuel-cell, MPPT based solar-PV system and battery causes detrimental effect on the performance of sources [Wang *et al.*, 2013]. An injection of SHC ripple into the fuel cell causes fuel-starvation, reduction in efficiency, heating inside and stress on the proton exchange membrane. The low frequency ripples (less than 400 Hz) should be kept small for the long life expectancy [Mazumder *et al.*, 2007] and for this SHC ripple should not exceed 10% [RS, 2003]. For the good efficiency and life-expectancy of the fuel-cell, the SHC ripple of 100 Hz/120 Hz should be limited to 15% of output power [EG and Inc, 2016]. In [Mazumder *et al.*, 2007], it is established that for a solid-oxide fuel-cell, a 17%-reduction in the peak-value of current ripple (from 22% to 5%) improves the efficiency of the fuel-cell by 5%. This efficiency can go upto 9% for the ripple compensation by 31% (i.e. from $36\% - 5\%$). The AC-DC power conversion used in the PFC to supply power to LEDs leads to low-frequency $2\omega-$ripple at the DC link. Unlike the incandescent lamps, the no-time delay operation of the LED at the low frequency causes the flickering effect [Arias *et al.*, 2013; Krein *et al.*, 2012; Veitch and McColl, 1995]. In the North America, the flicker i.e at two times of 60 Hz or at 120 Hz should be limited within 10% of the averaged lighting output [Fang *et al.*, 2015]. In the MPPT operation of the solar-PV or fuel cell, a pulsation of the SHC ripple about the maximum power points (MPPs) of the power/current/voltage may shift the actual MPPs. This causes an improper MPPT operation and results in the reduced efficiency of the power conversion. According to [Sullivan *et al.*, 2013], a decrease of 5% in the efficiency and power of the solar-PV with MPPT operation is observed for an 8% ripple in the rms value of MPPs. In the Fig. 2.2(b), the effect of the SHC ripple on the MPPs is shown using P-V diagram. Table 2.1 summarizes the Section 2.1.2.

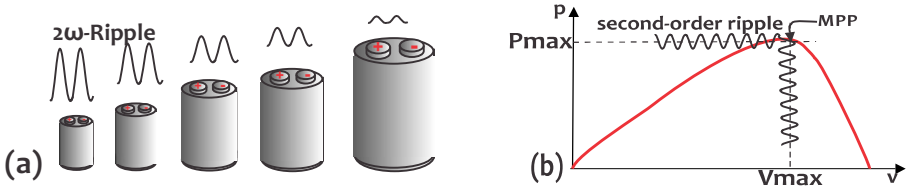

Figure 2.2 : (a) For the same voltage rating, a large size E-cap decouples more 2ω-ripple (b) Effect of 2ω-ripple on MPPT operation [Shi *et al.*, 2016a]

The injection of 2ω-ripple into the battery causes heating effect. According to [He *et al.*, 2014], a current ripple more than 8% may badly affect the electrodes and electrolyte of the battery and reduces the performance and efficiency of the system. Moreover, ripple increases the voltage/current stress on the system components [Kwon *et al.*, 2009; Zhang *et al.*, 2013].

Before proceeding for $2\omega-$ripple mitigation methods, a brief discussion of $2\omega-$ripple problem for the different topologies of single-phase inverter is presented in the next Section.

Table 2.1 : Summary of cause, effect and design constraint of SHC ripple

Affected system/algorithm	Effect on system	Cause and constraint	Reference
Capacitor at DC-link	Heating effect; Reduction in life of aluminum capacitor by $10\% - 90\%$ a year at $105^o\ C$	Large ESR causes i^2r-losses and high temperature;$10^o\ C$ rise reduces life of E-cap by half; To limit voltage pulsation within $\pm 1\%$, a $\approx 6\ mF$ E-cap required for $100\ W, 60\ Hz-$inverter	[Krein *et al.*, 2012] [gui, Epdf; He *et al.*, 2014]
Fuel cell stack	Poor efficiency and affect life	SHC ripple $> 10\% - 15\%$	[EG and Inc, 2016; RS, 2003] [Mazumder *et al.*, 2007]
Fuel cell MPPT	Excessive use of H_2/O_2 or reactant	SHC ripple $> 8\%$	[He *et al.*, 2014]
Solar PV MPPT	Poor efficiency; Nuisance tripping	SHC ripple $> 10\%$; Oscillation about MPP	[Sullivan *et al.*, 2013]
Battery	Affect the electrodes and electrolyte,	SHC ripple $> 8\%$; Heating due to hysteresis	[He *et al.*, 2014]
LED lights	Flickering effect; Visual fatigue	No time delay or latency effect in LED lights against SHC ripple flicker should be restricted within 10%	[Veitch and McColl, 1995] [Krein *et al.*, 2012; Wilkins *et al.*, 2010] [Arias *et al.*, 2013; Fang *et al.*, 2015]
System components	Over-rated design; High stress	low frequency and increase in peak values	[Zhang *et al.*, 2015]

2.2 SINGLE-PHASE INVERTER TOPOLOGIES AND ASSOCIATES $2\omega-$RIPPLE PROBLEM

The reflection and injection of the second-order ripple at the input of the DC-AC power converters may directly affect the DC source. However, the topologies with the front-end converter(s) or front-end control circuitry such as Z-source network in the ZSI or quasi-ZSI are capable to restrict the prapogation of the SHC ripple to the DC source when the components of the Z-source network are chosen accordingly; an optimum design of the inductors of Z-source network can restrict the low-frequency current ripple and an optimum design of the capacitors of the Z-source network can restrict the low-frequency voltage ripple Liang *et al.* [2018]. In such systems, the front-end converter or network is affected by the $2\omega-$ripple. A good engineering is required to design an optimum design of the components of the front-end network and a suitable compensator for the front-end converter to restrict the flow of the ripple to source. In this Section, a classification of the single-phase power converters is carried-out on the basis of (a) number of power conversion stages for the power processing, (b) location of the power decoupling components, (c) isolation and (d) grid-integration (grid-tied or off-grid operation) Franquelo *et al.* [2008]; Kjaer *et al.* [2005]; Lai and Ellis [2017]; Li and Wolfs [2008a]; Siwakoti *et al.* [2015]. Fig. 2.3 shows a classification of topologies of the single-phase inverter based on the different applications. In the single-stage topologies, the H-bridge is used to convert the DC power into AC power. In such topologies, the passive and active power decoupling techniques are used. The single-stage topologies can be the voltage source inverters or the current source inverters. Generally, the large size capacitor at the input of the voltage source inverter decouples $2\omega-$ripple. Similarly, in the current source inverter, the large size input inductor may help in the reduction of the $2\omega-$ripple at the source. The multi-stage toplogies have multiple front-end converter with back-end inverter. Generally, two stage converters are used in several RE applications. The front-end converter of two-stage converter is the DC-DC converter for the DC input. The front-end converter facilitates the system in several ways such as $2\omega-$ripple control, voltage transformation, MPPT operation, voltage regulation. In such topologies, besides active and passive ripple compensation techniques, the control-oriented compensation techniques can also be used. These topologies can also be classified based on the location of the E-cap at the DC-link. An E-cap can be placed at the input of the inverter or at the input of the front-end converter in the two-stage converter or at both locations. A large size E-cap at the DC terminal ensures a better $2\omega-$ripple compensation. Furthermore, the classification can be done on the basis of the isolation and the grid-interaction. The isolation can be achieved using the line frequency transformer or using a high frequency DC-DC converter at the front-end of inverter such as dual-active bridge. Island or remote power systems are standalone power networks. In such systems, storage is an important requirement. The loads are supplied through renewable energy sources directly while storage supplies power at the non-availability of the renewable energy sources or at the energy deficit in the system. The sources and storage (battery energy storage system) may be affected by the $2\omega-$ripple when they supplies AC loads. The grid-tied system exchanges power with the main grid through the AC-DC converter at the point of common coupling. The AC-DC power converter may injects the $2\omega-$ ripple into DC power system.

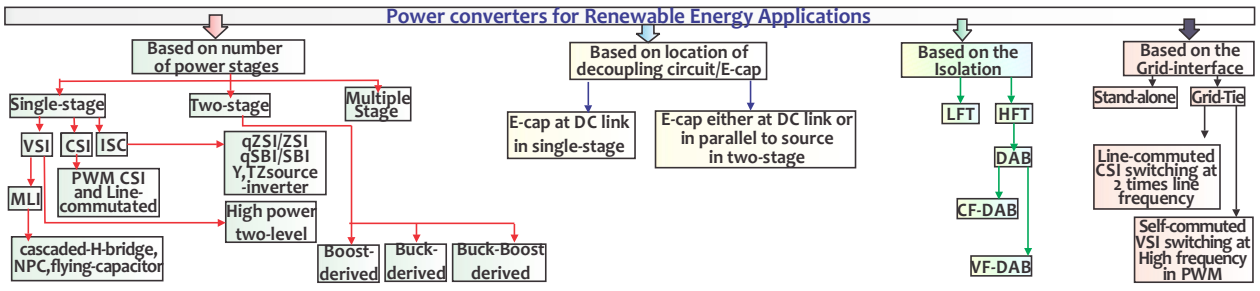

Figure 2.3 : Topologies of single-phase inverter for the renewable energy applications

2.3 CLASSIFICATION OF RIPPLE MITIGATION METHODS

There are several techniques to decouple the 2ω-ripple at the DC-link itself and/or to resist 2ω-ripple propagation to the DC source. The propagation of 2ω-ripple towards the DC source can be avoided by storing the 2ω-power ripple in a large E-cap at the DC-link or forcing the voltage to swing at 2ω directly at the DC-link itself or allowing indirect voltage-swing across the film capacitor through an auxiliary circuit or active filter, and hence 2ω-swing effect in the DC-link voltage can be avoided. The indirect power decoupling is a better choice in terms of the reliability of the film capacitor and ripple-free DC-link voltage. Besides this, the control-oriented compensation techniques can directly be used in the two-stage DC-DC-AC converters and single-stage inverters with the front-end control-capability; no additional active filter is necessary in such power converters to achieve ripple free or reduced ripple operation of source. These techniques utilize the one or more control-strategy(s) such as output-impedance shaping, loop-bandwidth shaping, generation of the ripple-free reference of the input current and forcing the ripple flow through the DC-link capacitor. Based on the above mentioned techniques, the 2ω-ripple control techniques can further be classified in the three broad categories (i) passive power-decoupling techniques (PPTs) (ii) active power-decoupling techniques (APTs) and its sub-category (iii) control-oriented compensation techniques (CCTs) for inverter with front-end converter or in-built front-end control circuit. To implement these techniques, different topographical arrangements (based on the location) can be made for the different power-decoupling circuits and control strategies. These topographical arrangements are made (a) at DC-link or DC side of the inverter and (b) at AC side of the inverter or mixed-type. In the Fig. 2.4, the basic methodology of the different techniques are depicted. The classification of the $2\omega-$ripple mitigation techniques is depicted in the Fig. 2.5. These techniques are reviewed in the next subsections.

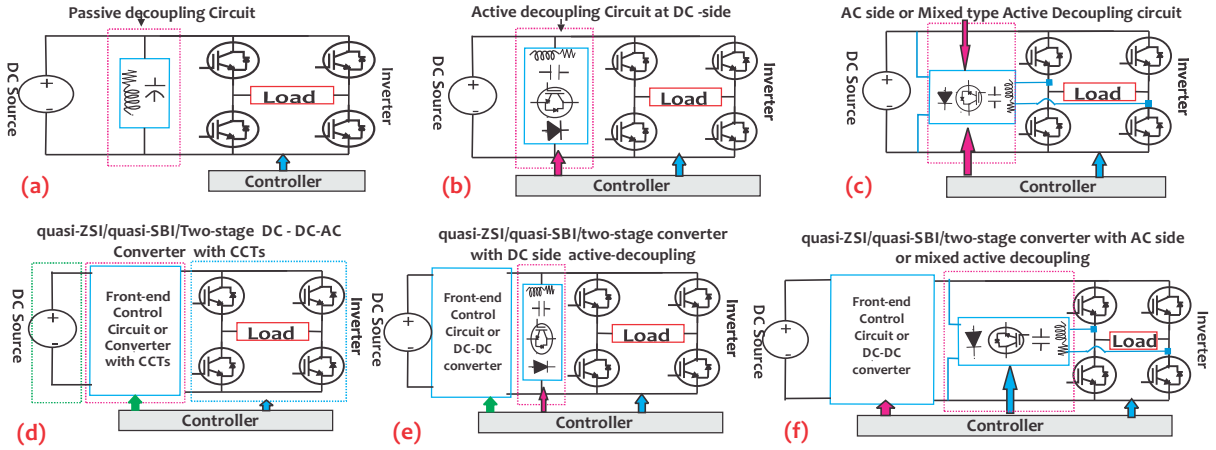

Figure 2.4 : Topographical Arrangements: (a) PPTs at DC link (b) APTs at DC link (c) APTs at AC side or mixed type APTs (d) ZSI, quasi-SBI or two-stage DC-DC-AC converter with CCT only (e) ZSI, quasi-SBI or two-stage DC-DC-AC converter with active power decoupling circuit at DC side (f) ZSI, quasi-SBI or two-stage DC-DC-AC converter with mixed type active power decoupling circuit

2.3.1 Passive power-Decoupling Techniques

PPTs are conventional and easy to implement without using control schemes. There are several topologies of the inverter which use the PPTs. The topologies shown in the Fig. 2.6(a-b) are the conventional stand-alone voltage source inverter [Nguyen and Choi, 2018; Rodriguez *et al.*, 2002; Wenyi and Chen, 2009] and grid-connected voltage source converter [Araujo *et al.*, 2010; Liserre *et al.*, 2006; Rahim and Selvaraj, 2010] respectively. These topologies require a large size of DC-link capacitor [Blaabjerg *et al.*, 2006; Kjaer *et al.*, 2005; Xue *et al.*, 2004]. Moreover, in such topolo-

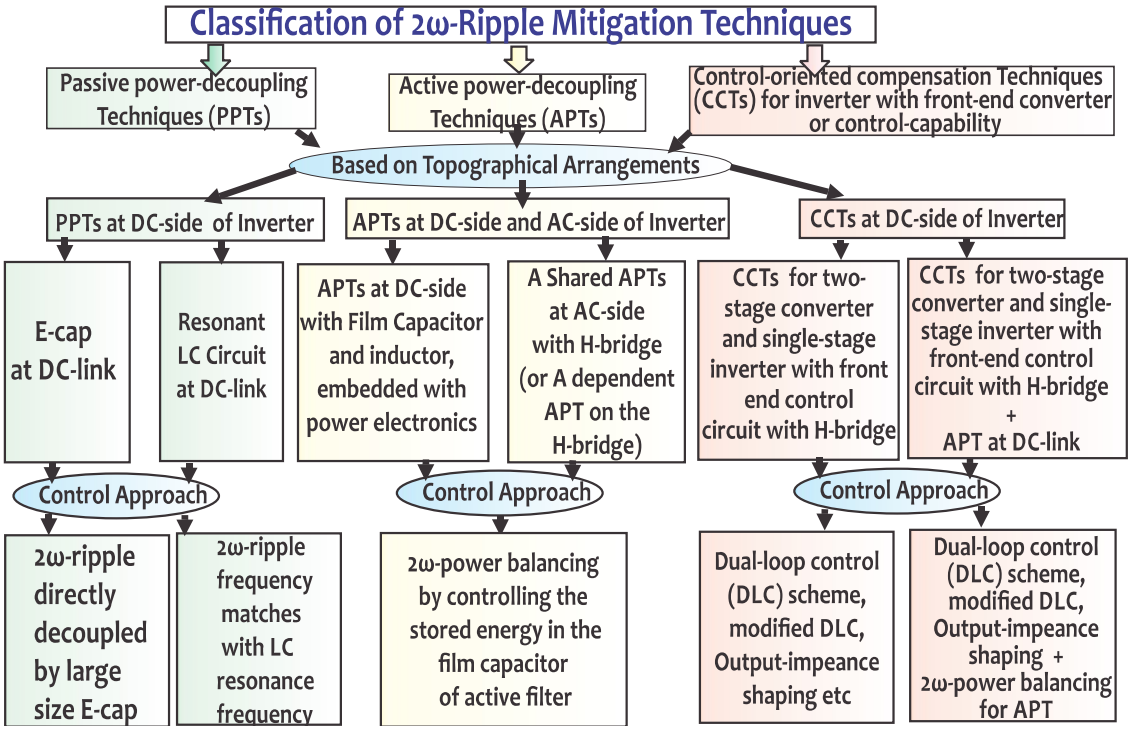

Figure 2.5 : Flow chart of classification of $2\omega-$ripple mitigation techniques

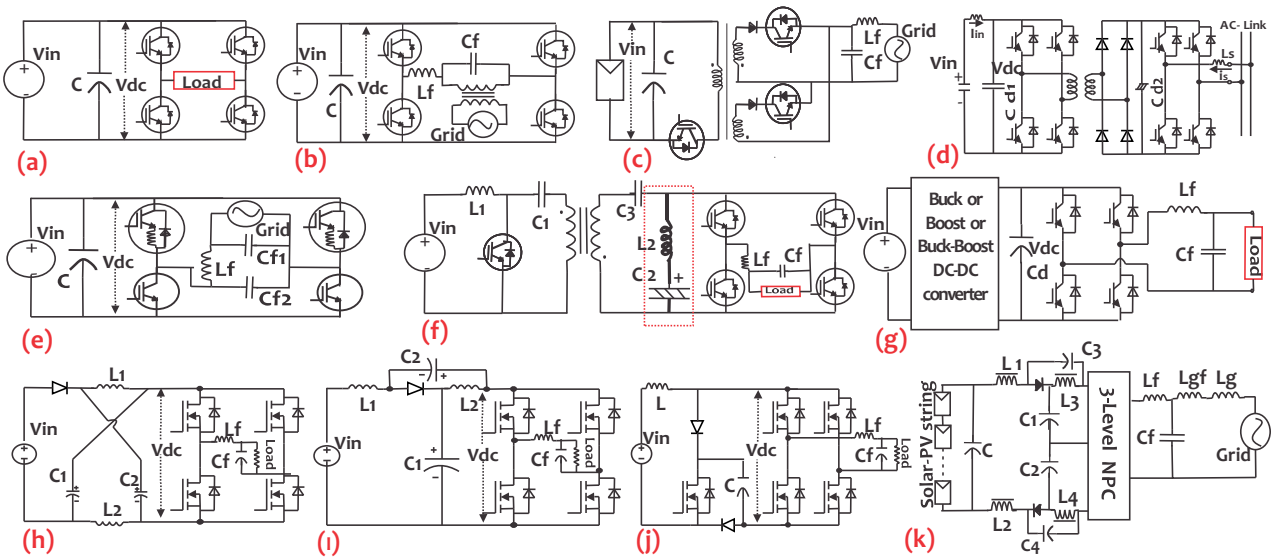

Figure 2.6 : Passive power decoupling techniques (a) Isolated Voltage source inverter (b) Grid-tied-Voltage source converter (c) Flyback-type center-tapped inverter (d) Inverter with front-end dual-bridge converter with high-frequency DC-link (e) Transformer-less buck and boost inverter topology (f) Pulse-link DC-AC converter (g) two-stage DC-DC-AC converter (having a front-end buck or boost or buck-boost DC-DC converter) (h) Z-source inverter (i) quasi-Z source inverter (j) quasi-switched boost inverter (k) Three-level single-phase impedance source inverter

gies, a front-end DC-DC buck or boost converter or a line-frequency transformer at the output-end of the inverter is used to step-down or step-up the voltage. Some of the isolated topologies are shown in the Fig. 2.6(c)-(d)-(f). A flyback-type center-tapped inverter (see Fig. 2.6(c)) is proposed in [Kyritsis *et al.*, 2005] for the isolated operation. However, this topology is suitable for the residential low power applications. Recently, some isolated two-stage DC-DC-AC power converter with high frequency AC link (see Fig. 2.6(d)) such as dual-half bridge converter and dual-active bridge (DAB) are proposed for the high power applications [Hu and Li, 2017; Shen *et al.*, 2018; Steigerwald, 2001; Zhao *et al.*, 2014]. In [Wang, 2004], a novel topology is proposed for the voltage buck and boost operation without using a front-end DC-DC converter or a transformer (see Fig. 2.6(e)). However, in all these topologies, a power decoupling electrolytic capacitor is used at the DC link. The large size inductors used in the current-fed inverter can minimize the ripple at the input [Jang *et al.*, 2007], and also by employing a tuned-resonant filter at the DC-link, the SHC ripple can be decoupled [Iyer and John, 2015]. An optimal design of the resonant filters allows to replace the E-cap(s) with the film capacitor(s). In [Fukushima *et al.*, 2009], authors have proposed a pulse-link DC-AC converter (see Fig. 2.6(f)). In this topology L_2C_2 makes the resonating tank. This resonant-filter is tuned at 2ω such that the most of SHC ripple passes through the low impedance L_2C_2-branch when the resonance frequency (ω_o) matches with 2ω. However, this method has a drawback, even though the C_2 is small enough to replace with the film capacitor, the size of the inductor (L_2) required is quite large. The non-isolated two-stage DC-DC-AC converter are popular in the RE/alternative energy applications [Li and Wolfs, 2008b]. The intermediate DC-DC power stage can be a buck-type, boost-type or buck-boost-type depending on the voltage/power requirements [Ahmad *et al.*, 2012; Jamatia *et al.*, 2016b; Zhu *et al.*, 2015] (see Fig.2.6(g)). Conventionally, a large size E-cap is used at the DC link in these topologies. These topologies still have a challenge of accidental short-circuiting of the switches in the same leg(s) of the inverter [Peng, 2003]. This may damage the system as the inverter in such topologies is a voltage source converter. The impedance-source inverters (ISIs) [Chub *et al.*, 2016; Ellabban and Abu-Rub, 2016] are the good choice in such limitations and operating conditions. However, these topologies require large size impedance-source network to filter low-frequency SHC ripple [Ge *et al.*, 2016a,b; Zhou *et al.*, 2016]. In Fig.2.6(h-k), Z-source inverter, quasi-Z source inverter and quasi-switched boost inverter are shown. In [Makovenko *et al.*, 2017], a resonant-cum-PID controller based PPT is presented for the three-level single-phase impedance-source inverter. The main idea of this method is to restrict the voltage fluctuation about the capacitors in impedance source network (see Fig.2.6(k)) by varying the shoot-through duty accordingly such that the SHC ripple confines at the quasi-ZSI network and does not affect the input. The resonant controller suppresses the SHC ripple at the input. However, in this technique, the closed-loop zeros and poles of the system come very close to imaginary-axis, therefore, a PID controller is added for the desired pole-zero cancellation. According to [Makovenko *et al.*, 2017], this method still suffers the input power ripple fluctuation (i.e. about 30%) at the rated power operation.

2.3.2 Active Power-Decoupling Techniques

Active power-decoupling techniques have been evolved from the PPTs to fulfill the need of a suitable and reliable substitute of E-cap. Generally, APTs use additional power electronic devices and energy buffer especially a thin film capacitor and inductor. The wide applicability and substantial reduction in the size of E-cap using engineering techniques make the APTs popular. The active filter contains a small size film capacitor to buffer $2\omega-$ripple. An inductor is also required to transfer 2ω-power ripple between the coupling point of active filter at the DC or AC side of the main circuit and the buffer capacitor connection point. The control scheme of active decoupling circuit is generally associated with the main control. In general, the control aims to balance the required 2ω-ripple power in the system by exchanging the reserved power of buffer capacitor in the active filter. Nevertheless, a proper selection of the film capacitor is a priori to keep the design optimum, physically as well as economically. According to [Zhang *et al.*, 2017], the voltage across

buffer capacitor can have three general form of the voltage considering all types of the APTs: a sinusoidal waveform at ω, a sinusoidal waveform at 2ω with DC-offset and rectified waveform at 2ω (see Fig. 2.7). Suppose $v_c(t)$ and $i_c(t)$ are the voltage across and current through the buffer

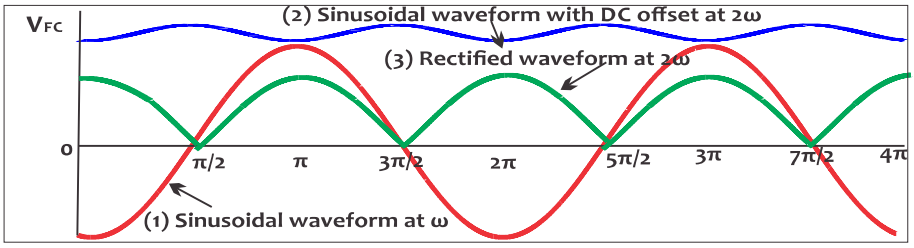

Figure 2.7 : Three type of voltage waveform buffered by film capacitor [Zhang *et al.*, 2017]

capacitor (C_{FC}) respectively then 2ω-ripple power decoupled is given by,

$$p_r = v_c(t)i_c(t) \tag{2.9a}$$
$$p_r = 0.5C_{FC}\dot{v}_c^2(t) \tag{2.9b}$$

By solving the differential equation (2.9b) for the given $v_c(t)$ and p_r, the minimum size of the ripple-port capacitor for the three different waveforms can be calculated [Zhang *et al.*, 2017]. The minimum size of the ripple-port capacitors required in the different APTs is tabulated in the Table 2.2. In what follows several APTs are discussed using the two different topographical arrangements of the active power-decoupling circuits. Firstly, the DC-side APTs are discussed here.

Topographical Arrangement#1: APTs at DC side/link

This arrangement is made at the DC-link or DC-side of inverter. Generally, the active power decoupling circuit is directly shunted at the DC-link by replacing the large size E-cap (see Fig. 2.8(a) to Fig.2.8(g). These topologies are independent of the H-Bridge of the DC-AC power converter. The circuits in the Fig. 2.8(h) and Fig. 2.8(i) are the dependent decoupling circuits and utilize a part of the H-Bridge. Recently, some series power decoupling technique as shown in Fig. 2.8(j) are proposed [Liu *et al.*, 2015; Lyu *et al.*, 2015, 2016; Wang *et al.*, 2014a]. This type of decoupling techniques add a series active decoupling circuit between the source and H-Bridge. The buck, boost or buck-boost type active filters are addressed in [Cai *et al.*, 2014; Christidis *et al.*, 2016; Fan *et al.*, 2012; Hu *et al.*, 2010; i. Itoh *et al.*, 2016; Krein *et al.*, 2012; Kyritsis *et al.*, 2007; Wang *et al.*, 2011; Watanabe *et al.*, 2018].

The basic principle of ripple decoupling in the APTs using active filter at the DC-side is as follows [Krein *et al.*, 2012]. Suppose C_{FC} is the film capacitor for power decoupling in active filter. The voltage across the film capacitor is v_c is given by,

$$v_c = V_{c_m}cos(\omega t + \varphi) \tag{2.10}$$

Here V_{c_m} is maximum value of the capacitor voltage and φ is an arbitrary phase-angle. The current through the capacitor is,

$$i_c = C_{FC}\frac{d}{dt}V_{c_m}cos(\omega t + \varphi) \tag{2.11}$$

The decoupling power ripple is given by,

$$p_{FC} = v_c(t)i_c(t) \tag{2.12a}$$
$$= v_c(t)C_{FC}\frac{d}{dt}V_{c_m}cos(\omega t + \varphi) \tag{2.12b}$$
$$= -0.5C_{FC}V_{c_m}^2\,\omega sin(2\omega t + 2\varphi) \tag{2.12c}$$

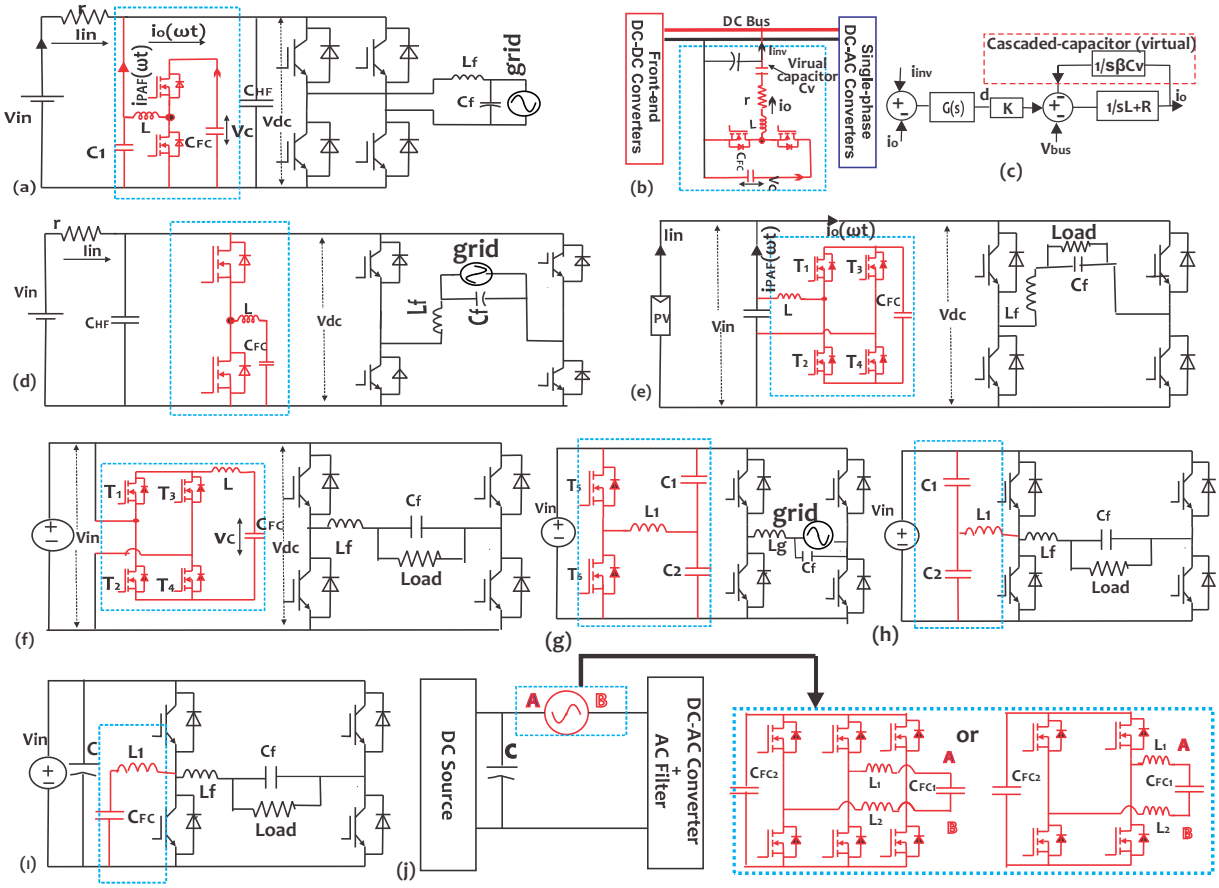

Figure 2.8 : Active power-decoupling circuits at DC-link: (a) CPS-PAF-Boost type [Kyritsis *et al.*, 2007] (b) ALFRCD with cascaded capacitor [Cai *et al.*, 2014] (c) Current control loop of ALFRCD with virtual cascaded capacitor [Cai *et al.*, 2014] (d) Bidirectional-buck type APT [Wang *et al.*, 2011] (e) FB-RCR circuit [Christidis *et al.*, 2016] (f) Ripple-port circuit [Krein *et al.*, 2012] (g) Dual-voltage control decoupling strategy using a symmetric half-bridge circuit with H-bridge [Huang *et al.*, 2018; Tang *et al.*, 2015b] (h) Dependent power decoupling with two-phase legs [Qi *et al.*, 2014; Serban, 2015; Zhang *et al.*, 2017] and (i) [Tang *et al.*, 2015a; Zhang *et al.*, 2017] (j) Series power decoupling technique with two legs [Wang *et al.*, 2014a] and three legs [Lyu *et al.*, 2015, 2016]

The 2ω-power ripple at DC-link is equal to p_{FC}. Applying power ripple balance at the DC-link and using (2.1c) and (2.12),

$$0.5V_mI_mcos(2\omega t-\theta) = -0.5C_{FC}V_{c_m}^2\,\omega sin(2\omega t+2\varphi) \tag{2.13a}$$

$$P_ocos(2\omega t-\theta) = -0.5C_{FC}V_{c_m}^2\,\omega sin(2\omega t+2\varphi) \tag{2.13b}$$

In (2.13), the amplitude of V_{c_m} is adjusted by control such that $P_o = 0.5C_{FC}V_{c_m}^2\,\omega$ which follows,

$$sin(2\omega t+2\varphi) = cos(2\omega t-\theta) \tag{2.14}$$

Solving (2.14) gives,

$$\varphi = -\frac{\pi}{4}-\frac{\theta}{2} \tag{2.15}$$

The active filter decouples 2ω power ripple if (2.15) holds and $P_o = 0.5C_{FC}V_{c_m}^2\,\omega$ is satisfied by some value of V_{c_m}. Therefore, the control adjusts φ and V_{c_m} to buffer 2ω-power ripple.

Several APTs based on the above control design and some other control schemes reviewed here for the DC-side power decoupling arrangement. In [Kyritsis *et al.*, 2007], a current pulsation smoothing-parallel active filter (CPS-PAF) is proposed. The CPS-PAF consists of a small film capacitor and a conventional non-isolated buck/boost circuit (see Fig. 2.8(a)). This circuit behaves like a current-source. The working principle of power decoupling is shown in the Fig. 2.9(a) [Christidis *et al.*, 2016; Kyritsis *et al.*, 2007]. In Fig. 2.8(a), the controller continuously compares the input

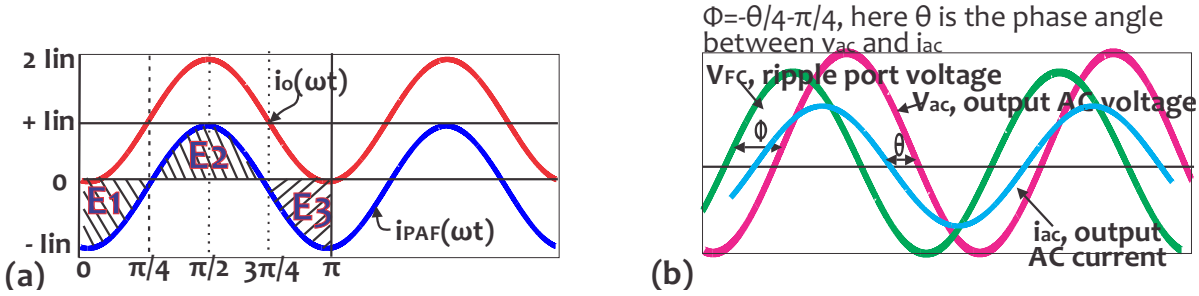

Figure 2.9 : Working principle of (a) CPS-PAF [Christidis *et al.*, 2016; Kyritsis *et al.*, 2007] (b) Ripple-port [Krein *et al.*, 2012]

current (I_{in}) with instantaneous value of the DC-link current ($i_o(\omega t)$). For $I_{in} > i_o(\omega t)$ in interval $0-\pi/4$ and $3\pi/4-\pi$, C_{FC} stores energy (boost-mode) and for $I_{in} < i_o(\omega t)$ in interval $\pi/4-3\pi/4$ releases the energy (buck-mode). For energy stored (say E_1+E_3) equals to energy released (say E_2) by C_{FC}, the low frequency pulsation at the DC-link is zero. C_{HF} takes care of high frequency ripples. The implementation of this active filter is simple. However, the active power imbalance between input and output of PAF and the power loss of PAF cause a decrease in the voltage of C_{FC} resulting in a lower value of V_c than the DC-link voltage. In such case the PAF gets short-circuit the input and output and ripple elimination is affected [Christidis *et al.*, 2016]. To resolve this problem, a mixed type APT version of CPS-PAF is proposed in [Kyritsis *et al.*, 2007] (see Fig. 2.11(f)). The grid feeds the rectified power to C_{FC} through the line transformer to compensate the losses. However, the system becomes bulky and complex. In Fig. 2.8(b), a buck-boost type active low-frequency ripple control device (ALFRCD) is shown that is proposed in [Cai *et al.*, 2014] for the building-integrated photovoltaic (BIPV) systems. The concept of ripple mitigation using ALFRCD is same as presented in [Kyritsis *et al.*, 2007]. However, in [Cai *et al.*, 2014], a virtual capacitor is added in series with the inductor of the active filter through the control (see Fig. 2.8(b)). The virtual capacitor is realized by adding an integrator in the current control-loop (see Fig. 2.8(c)). The

control scheme forces the output current of the active filter (i_o) to track the DC-link current (i_{inv}). The important requirement of this scheme is to keep the voltage of the film capacitor (C_{FC}) higher than the bus voltage. Wang *et al*. proposed a similar bidirectional buck type-APT (see Fig. 2.8(d)) in [Wang *et al*., 2011]. The working principle of the power ripple decoupling control scheme is same as in [Kyritsis *et al*., 2007] (see Fig. 2.9(a)). In [Wang *et al*., 2011], a DCM control scheme is used such that the C_{FC} stores all the SHC ripple while L functions like a power transfer element. Therefore, L does not store decoupling power that is good in terms of the power-density. Also, unlike CPS-PAF, the voltage of C_{FC} is less than the DC bus or DC-link voltage or any other voltage in the system. It is to be noted that the discontinuous current mode (DCM) operation of the front-end DC-DC converter of two-stage converter minimizes the input 2ω-ripple inherently [Lu, 2017]. The main cause of the ripple-reduction at the input of the two-stage converter is the less interaction of DC source and DC-link due to discontinuity. The buck-derived and boost-derived two-stage converter has minimum SHC ripple at the input in the DCM operation. The input and output of the buck-boost-derived two-stage converter do not interact directly during switching in the DCM operation. Therefore, the input of buck-boost-derived two-stage converter are ripple-free. A four-switch based bidirectional full-bridge-ripple current reduction (FB-RCR) circuit is shown in the Fig. 2.8(e) [Christidis *et al*., 2016; Wang *et al*., 2014a]. The working principle of the FB-RCR is same as of CPS-PAF of [Kyritsis *et al*., 2007]. However, unlike [Kyritsis *et al*., 2007], there is no requirement of the line-frequency transformer with the rectifier. The internal energy losses which are the cause of constant voltage decrease of C_{FC} in the FB-RCR circuit are compensated by sourcing power from the input source itself. However, the FB-RCR circuit contains four switches which operate at the high frequency. Therefore, the system becomes bulky and the switching loss increases. A similar APT based on the ripple-port concept is presented in [Krein *et al*., 2012]. In this circuit, the inductor (L) is placed in series and adjacent to C_{FC}, this makes a ripple-port (see Fig. 2.8(f)). The control design is based on (2.10)-(2.15). The working principle of this technique is depicted in the Fig. 2.9(b). In the Fig. 2.8(f) and Fig. 2.9(b), ϕ is the phase difference between the instantaneous voltage of the film capacitor (v_{FC}) across C_{FC} and output voltage of inverter (v_{ac}), and θ is the displacement angle between instantaneous value of v_{ac} and i_{ac}. In (2.15), for the unity power factor, $\theta = 0$, the phase-shift between v_{ac} and v_{FC} is $\pi/4$. In [Tang *et al*., 2015b], Tang *et al*. have proposed a dual voltage control strategy for the symmetric half-bridge circuit with H-bridge. The circuit diagram is shown in the Fig. 2.8(g). The two capacitors (C_1, C_2) are used to decouple the power ripple. The control scheme aims to modulate the switches of half bridge such that the voltages across the two capacitors are equal and 2ω-pulsating voltage component over the offsets of voltages are out of phase by 180°. Following the power balancing condition, the required power decoupling condition for the voltage and phase are as follows,

$$\varphi = 0.5tan^{-1}\left(\frac{-V_{rms}}{\omega L_f I_{rms}}\right) \tag{2.16a}$$

$$V_c = \sqrt{\frac{\sqrt{(V_{rms}I_{rms})^2 + (\omega L_f I^2 m)^2}}{\omega(2C_f - L_f(2\omega C_f)^2)}} \tag{2.16b}$$

Here I_{rms} and V_{rms} are *rms* values of AC current and voltage. I_m is maximum current of AC current. $C_f = C_1 = C_2$. V_c is rms offset-voltage of capacitors. φ is phase difference between the grid voltage and pulsing voltage in the capacitor.

The APTs as shown in the Fig. 2.8(h) and Fig. 2.8(i) share at least one of phase of the H-bridge and active filter circuit. Therefore, these APTs are dependent on the H-bridge. This affects the modulation signal of the inverter. In the two-phase legs topologies (see Fig. 2.8(h-i)), the DC voltage utilization is kept always less than or equal to 0.5 to avoid over-modulation and to keep the value of film capacitor minimum. In such topologies, the third type of voltage waveform across the film capacitor shown in Fig. 2.7 ensures that the size of capacitor required in the circuit is minimum [Zhang *et al*., 2017].

In the Z-source inverters and quasi-Z source inverters, the large number of components and their bigger size pose challenges. The 2ω-ripple further forces over-sized design of these components especially a large size E-cap requirement. Adding active decoupling circuit at the DC-link resolves this problem. The thin film capacitor can be used with the active filter. However, this adds extra components to the circuit. Recently, some buck-boost type active filters are presented for the quasi-Z source inverter [Singh *et al.*, 2016]. In [Singh *et al.*, 2016], a hysteresis current controlled active power filter is proposed to confine the 2ω-ripple within the active filter ripple-port (see Fig. 2.10(a)). The control logic is same as shown in the Fig. 2.9(a). However, the control design of active filter for the quasi-ZSI is somewhat more challenging than the H-bridge converter. A bidirectional buck-boost type active filter connected at the DC-link of the quasi-ZSI is shown in the Fig. 2.10(b) [Liu *et al.*, 2017]. The design of the active filter is similar as shown in the Fig. 2.8(d). In [Liang *et al.*, 2018], a comprehensive design of asymmetric ZS-network in the perspective of high frequency and low frequency ripple minimization is discussed the first time. The design is presented for a battery energy-stored quasi-Z source based PV generation system (see Fig. 2.10(c)). The optimum size of the inductors for the $2\omega-$ current ripple suppression and the size of the capacitors for the $2\omega-$ voltage ripple suppression can be calculated using the quasi-ZS network design presented in [Liang *et al.*, 2018].

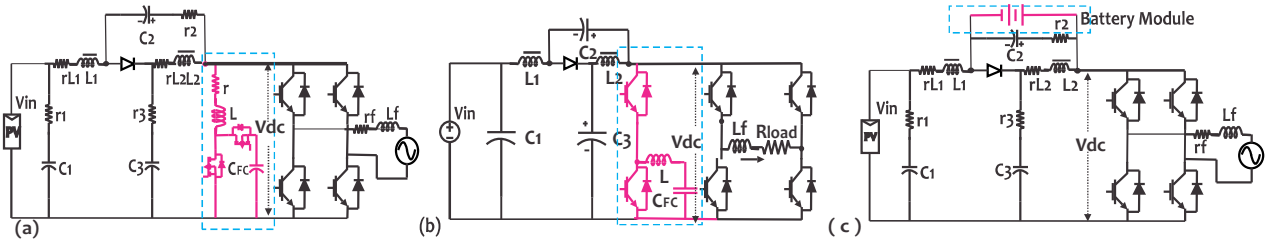

Figure 2.10 : quasi-ZSI with DC-side (a) boost-type active filter [Singh *et al.*, 2016] (b) bidirectional buck-boost type active filter [Liu *et al.*, 2017] (c) battery module [Liang *et al.*, 2018]

The AC-side APTs are discussed here.

Topographical arrangement#2: APTs at AC side or mixed

In this arrangement, the APT utilizes a part of DC side and a part of AC side of the main circuit, hence a mixed type arrangement. Generally, the power decoupling circuit in such techniques shares atleast one leg of the inverter and main circuit. The AC-side power decoupling techniques improve the power conversion efficiency in comparison to the DC-side power decoupling as the low frequency power pulsations are forced to confine at the AC-side [r. Zhu *et al.*, 2016; Zhu *et al.*, 2013]. Some of the recent AC side APTs are shown in the Fig. 2.11.

In [Serban, 2015], Serban has proposed an active power decoupling technique using two decoupling capacitors at the AC-side (see Fig 2.11(a)). The control technique reshapes the voltage across the legs of the inverter such that the SHC ripple is forced to propagate towards the two decoupling capacitors. The technique does not add extra power electronics to the main circuit. However, the DC-link voltage and current loading of the inverter set a trade-off for the values of decoupling capacitors. Consequently, the efficiency of the system is affected. This technique implements a complex control using multiple controllers. The utilization factor of storage elements is less than 50%. The circuits shown in the Fig. 2.11(b-g) add extra switches to the system. The inclusion of the third leg with the H-Bridge reduces the stress on the switches by 57% in comparison to the conventional topologies or H-Bridge [Bhowmick and Umanand, 2018; Shimizu *et al.*, 2000]. Zhu *et al*. in [r. Zhu *et al.*, 2016] proposed a ripple confinement control technique for the circuit shown in Fig. 2.11(b). This technique implements a voltage waveform control [Zhu *et al.*, 2013]

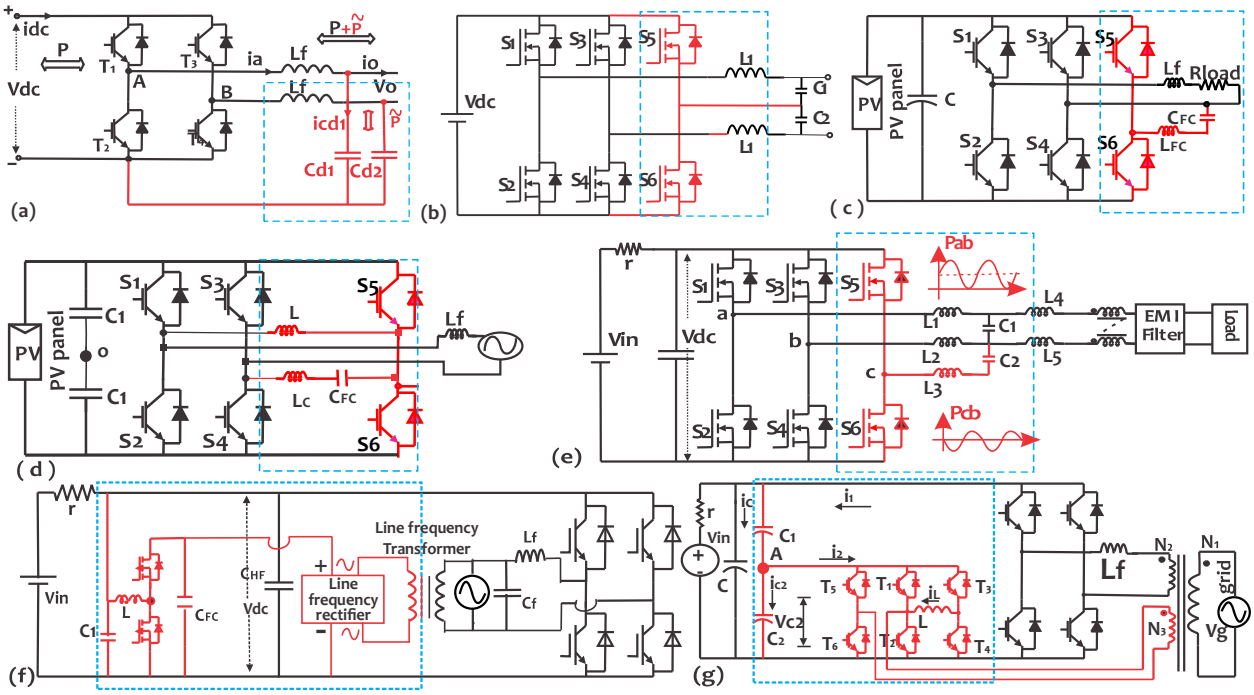

Figure 2.11 : Mixed type of APTs without adding extra power electronics (a) proposed in [Serban, 2015] and adding extra pair of switches (b) proposed in [r. Zhu *et al.*, 2016] (c) proposed in [Chen *et al.*, 2015] (d) proposed in [Bhowmick and Umanand, 2018] (e) proposed in [Morsy and Enjeti, 2016] (f) Modified version of CPS-PAF scheme based circuit in Fig. 2.8(a) [Kyritsis *et al.*, 2007] (g) Hybrid filter [Iyer and John, 2015]

to confine the pulsating power within the capacitors at the AC-side. A brief explanation of the waveform control is presented in the Section 2.3.4. A 100% utilization of the storage elements can be achieved using this method. However, this technique adds an extra pair of switches (see Fig. 2.11(b)) and also increases the voltage-stress on the capacitors. In [Chen *et al.*, 2015], Chen *et al.* have proposed a 2ω-power pulsation mitigation at the DC-link using the SVPWM method for the circuit proposed in [Li *et al.*, 2013] (see Fig. 2.11(c)). This technique eliminates DC capacitance and minimizes voltage and current stress on the switches for a range of the power factor. However, two extra switches are required and the total device power rating is increased by 50%. An APT for grid connected AC-DC power converter as shown in the Fig. 2.11(d) is proposed in [Bhowmick and Umanand, 2018]. This active decoupling technique significantly reduces the size of the DC-link capacitor. The stress on the switches is reduced up to 70% for all the power factor. However, this technique again adds a pair of switches and L-C components to the system. The study analyzes the effect of the grid-side inductance as well and provides design guidelines for different system parameter for the practical implementation. Another APT is proposed in [Morsy and Enjeti, 2016] for the microinverter applications; a problem from the Google little box challenge. The proposed technique is implemented on the GaN-based three-phase inverter topology as shown in the Fig. 2.11(e). In the circuit of Fig. 2.11(e), the load is fed between the phase a and b and the decoupling circuit is placed between phase b and c. The basic principle of the ripple cancellation is that the control keeps the sum of instantaneous powers p_{a-b} and p_{b-c} a constant value. Therefore, the ripple is confined within the AC side decoupling circuit and hence the ripple at the DC-link eliminates. Extra switches with the H-Bridge topology have been used in this topology. However, GaN switches are used in the considered topology which have comparatively better figure of merits such as low on-state conduction loss, wide-band gap, higher electron-mobility, switching frequency, efficiency

and power densities. A similar topology is presented in [Li *et al.*, 2013]. In [Iyer and John, 2015], a hybrid filter is proposed as shown in the Fig. 2.11(g). In the hybrid filter, there are three legs (six switches). The ripple energy is stored in both, capacitor C_1 and inductor, L. Using Kirchhoff's current Law at A in Fig. 2.11(g),

$$i_C = i_1 - (i_2 + i_{C2}) \tag{2.17}$$

In Fig. 2.11(g), for $C_2 << C_1$ the i_{C2} can be neglected in (2.16),

$$i_C \approx i_1 - i_2 \tag{2.18}$$

The hybrid filter generates i_2 such that $i_1 = i_2$. For this the inductor current should be controlled to keep the voltage across C_2 constant. However, the voltage v_{c2} keeps on decreasing due to internal loss of the filter. The hybrid filter (with 2 legs) alone is not sufficient. Therefore, an additional leg (switches T_5, T_6) is added to import the energy from the grid as shown in Fig. 2.11(g). This is a mixed type APT. Nevertheless, a small capacitor can be used for the power decoupling. However, the extra switches in third leg make the circuit bulky.

An AC side active filter is proposed for the quasi-ZSI in [Ge *et al.*, 2016b]. The control confines the decoupling power within the LC component of the filter using a third leg besides the H-bridge. The proposed topology of [Ge *et al.*, 2016b] is shown in the Fig. 2.12. The control aims to switch the third leg such that 2ω-power ripple is exchanged by the stored energy in L and C_{FC} component of the active filter, the power decoupling principle is the same as presented in [Krein *et al.*, 2012]. However, the energy stored in the inductor is also considered. In Fig. 2.12, the decoupling power ripple between B and C is given by,

$$p_{FC} = v_c i_{FC} + L\frac{di_{FC}}{dt} i_c \tag{2.19a}$$

$$= 0.5V_{c_m}^2 C_{FC}(1 - \omega^2 LC_{FC}) sin(2\omega t + 2\varphi) \tag{2.19b}$$

To decouple the $2\omega-$power ripple, the addition of the $2\omega-$ripple power component of (2.1c) and p_{FC} in (2.19b) should equate to zero i.e. $p_r + p_{FC} = 0$. This implies,

$$P_o cos(2\omega t - \theta) = 0.5V_{c_m}^2 C_{FC}(1 - \omega^2 LC_{FC}) sin(2\omega t + 2\varphi) \tag{2.20}$$

Here V_{c_m} is the maximum value of the voltage across the C_{FC} and i_{FC} is the current through L. $P_o = 0.5V_{rms}I_{rms}$. To decouple the power ripple the control follows $P_o = 0.5V_{c_m}^2 C_{FC}(1 - \omega^2 LC_{FC})$ and $\theta = -0.5\varphi + \frac{\pi}{4}$.

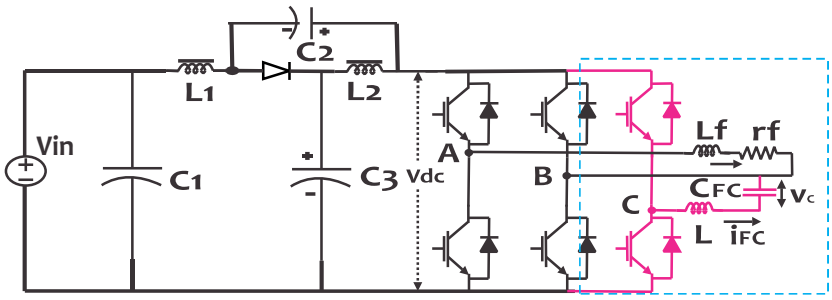

Figure 2.12 : Mixed type active decoupling circuit for the quasi-ZSI [Ge *et al.*, 2016b]

Table 2.2 : Design of Minimum Value of Filter Capacitor

Topology or Filter type	Filter location	Minimum design value	Reference
1) E-Cap	DC-link at DC side	$C_{dc} = \frac{P_o}{\omega V_{dc} \Delta v}$	[Krein *et al.*, 2012]
2) LC series filter (See Fig. 2.24(h))	Embedded with centre taping of transformer in half-active bridge in DC-DC-AC converter	$C_{FC} = \frac{P_{in}(P_{in} - V_{in} I_{trans})}{\omega V_c V_{in}(2P_{in} - V_{in} I_{trans})}$	[i. Itoh and Hayashi, 2010]
3) LC filter in H-Bridge type active filter (See Fig. 2.24(f-g))	Embedded with active filter at DC side	$C_{FC} = \frac{2P_{in}}{\omega V_{cm}^2 (1 - \omega^2 L)}$	[Harb *et al.*, 2013]
4) Flying capacitor (See Fig. 2.25(f))	Flying capacitor in modified boost- derived DC-DC-AC converter	$C_{FC} = \frac{2W}{\omega(v_u^2 - v_l^2)}$	[Watanabe *et al.*, 2018]
5) Extra third leg and LC filter with H-Bridge(See Fig. 2.12)	Embedded with active filter at AC side	$C_{FC} = \frac{4V_m I_m}{4V_m I_m \omega^2 L + V_{dc}^2 M_{32} \omega}$	[Ge *et al.*, 2016b; Liu *et al.*, 2016]
6) E-cap at DC-link	At DC-link of two-stage converter	$C_{dc} = \frac{1.359S}{\omega \Delta v V_{dc}}$	[Ahmad *et al.*, 2012]
7) Capacitors and Inductors (See Fig. 2.6(i))	quasi-Z Source network	$C_1 = C_2 = \frac{(1-2D_{sh})^2 + \sqrt{(1-2D_{sh})^2 (\frac{V_m I_m}{2V_{dc} i_{Lr}})^2 - (\frac{4\omega L I_{dc}(D_{sh}-1)}{V_{dc}})^2}}{4\omega^2 L}$ $L_1 = L_2 = \frac{v_{cr}(1-2D_{sh})}{2\omega i_{Lr}}$	[Ge *et al.*, 2016a]
8) E-cap at DC-link with control strategy proposed in [Hu *et al.*, 2015]	E-cap at DC-link of two-stage converter	$C_{dc} = \frac{2T_{ac}\Delta P}{\Delta v(2V_{dc} + \Delta v)}$	[Hu *et al.*, 2015]
9) Capacitors (See Fig. 2.22(d))	High gain q-SBI Network	$C_1 = \frac{D_{sh}(1-D_{sh})(1-2D_{sh})}{2v_1\%(1-4D_{sh}+2D_{sh}^2) f R_L}$ $C_2 = \frac{(1-D_{sh})^2}{2v_2\%(1-4D_{sh}+2D_{sh}^2) f R_L}$	[Nguyen *et al.*, 2018a]
10) CPS-PAF (See Fig. 2.8(a))	Embedded with active filter at DC side	$C_{FC} = \frac{0.422\pi P_{in}}{\omega(V_u^2 - V_l^2)}$	[Kyritsis *et al.*, 2007]
11) LC filter (See Fig. 2.25(e))	Embedded at AC side	$C_{FC} = \frac{V_m I_m}{\omega V_c^2}$	[Fan *et al.*, 2012]

In Table 2.2, Input power, P_{in}; input voltage, V_{in}; Peak to peak ripple voltage across C_{FC}, v; Upper voltage limit of v, V_u; Lower voltage limit of v, V_l; Average voltage across filter capacitor (C_{FC}), V_c; Maximum voltage across filter capacitor, V_{cm}; Transformer current, I_{trans}; maximum voltage/current at inverter output, V_m/I_m ; DC-link voltage, V_{dc}; DC-link current, I_{dc}; Modulation index, M_{32}, series inductance with C_{FC}, L; Apparent output power of inverter, S; Peak-peak DC-link voltage ripple, Δv; Shoot-through duty, D_{sh}; Desired amplitude of 2ω-ripple in through inductor, i_{Lr}; Desired amplitude of 2ω-ripple across C, v_{cr}; Time period of AC output, T_{ac}, Power mismatch during T_{ac}, ΔP; Capacitors used in [Nguyen *et al.*, 2018a], C_1, C_2; Peak-to-peak voltage ripple (of C_1,C_2), v_1, v_2; Simplified equivalent DC load, R_L; switching frequency, f; angular supply frequency of inverter, ω, Buffer energy, W.

2.3.3 Control-Oriented Compensation Techniques (CCTs) for Inverters with Front-end Converters or Control Circuits

Two-stage DC-DC-AC converters and single-stage DC-AC converters with front-end control circuits have capability to mitigate the ripple at input using the suitable control and the requirement of additional active filter in such systems is not a necessity. The main concept is to design a control scheme that restricts the propagation of SHC ripple towards the DC source(s) while forcing its flow through the DC-link capacitor. However, this causes a deliberated increase in 2ω-pulsation at the DC-link. This may affect the THD level of the output of the inverter. According to European standards (EN50160) for the public distribution systems, the low frequency voltage pulsation at the DC bus should be kept within 2% range. The limit of $2\% - 5\%$ is also considered in [Liu *et al.*, 2018; Shi *et al.*, 2018]. The THD level of output of the inverter should be kept within 5% and for the individual harmonic, it should be within 3% [IEE, 2013]. Therefore, an optimum design of the DC-link capacitor is involved. However, an optimum value of capacitance is not sufficient in the RE applications. The solar-PV, fuel-cell, wind-turbine possesses uncertain working characteristics and have poor dynamic performance at the large line-load transients with small or an optimum size of DC-link capacitor [Khajehoddin *et al.*, 2013]. According to [Ahmad *et al.*, 2012], for a 2.5 kW-boost-derived DC-DC-AC converter, a bulky 30 mF-capacitor is required at the DC-link to prevent large under/over-shoot at the load-transients in the absence of suitable controller. Therefore, along with ripple mitigation, the control should be robust enough to tackle the large line-load transients. Moreover, the control-oriented techniques without adding an auxiliary circuits still allow a 2ω-pulsation at the DC-bus up to some extent based on the optimum designed value of the DC-bus capacitance. Use of an active filter at the DC bus eliminates the SHC ripple. Fig. 2.13 shows block diagrams of the stand-alone and grid-connected two-stage DC-DC-AC converter with active-filter and without active-filter at the DC-link.

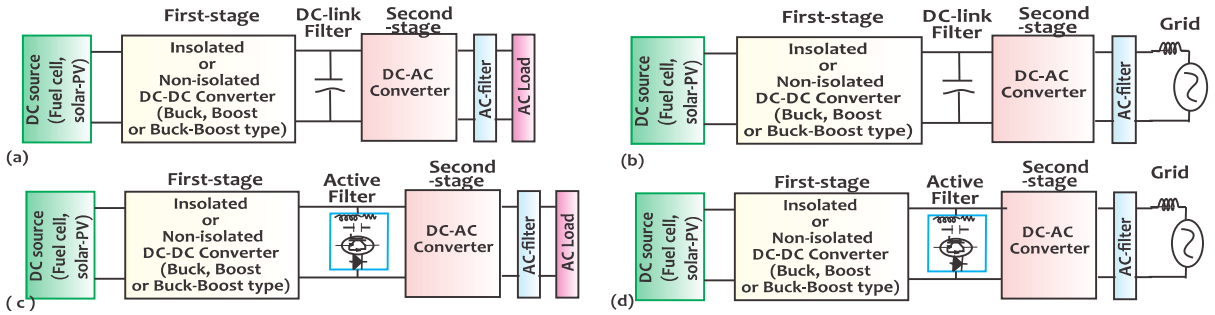

Figure 2.13 : Two-stage DC-DC-AC converter (a) Stand-alone without active-filter (b) Grid-tied without active-filter (c) Stand-alone with active-filter (d) Grid-connected with active-filter

Several control-oriented schemes with and without addition of the extra circuitry are reviewed in the following subsections.

CCTs Without Additional Active Filter

Kwon *et al*. have proposed a current-fed resonant push-pull converter and DC-AC converter based power conditioning system (PCS) for the fuel-cell application with a ripple-mitigation compensator [Kwon *et al.*, 2009]. The control block-diagram is shown in the Fig. 2.14(a). The control generates a duty (D_o) for the DC voltage regulation in the closed-loop. A feed-forward controller takes care of the SHC ripple by adding ripple-cancellation duty (D_r) to D_o. To reduce the ripple further, a perturbed duty (ΔD) is generated using the current control-loop and added to give overall duty ($D = D_o + D_r + \Delta D$). The performance of the feed-forward controllers is poor in terms of disturbance rejection and robustness against parametric uncertainty [Jung *et al.*, 2011]. Feedback control approaches are widely used in the different applications such as regulation, disturbance re-

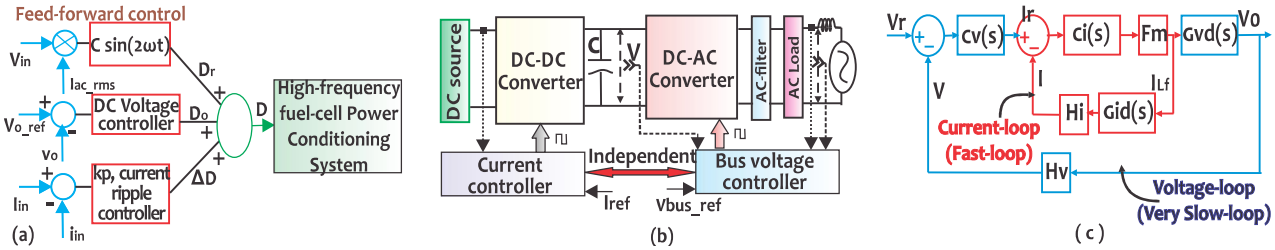

Figure 2.14 : (a) Feed-forward scheme [Kwon *et al.*, 2009] (b) Independent current & voltage loops[Jung *et al.*, 2011] (c) Dual loop control scheme[Liu and Lai, 2007a]

jection, robust control. In literature, the concept of the ripple-mitigation using the feed-back control in the two-stage converters is put forward in the two perspective. First one is based on the adopting a modified dual-loop control method. The method utilizes a current mode control (CMC). Second method is based on the output-impedance shaping. The method of output-impedance shaping can be implemented in a voltage mode control (VMC) i.e. using a single control loop also.

The CMC-based dual-loop control has an inner current-loop and an outer voltage-loop. To ensure the ripple-reduction at the input of the two-stage converter, the interaction between the inner-loop and outer-loop is avoided such that disturbances in the voltage-loop do not pass to the current-loop [Jung *et al.*, 2011; Khajehoddin *et al.*, 2013; Liu and Lai, 2007a] i.e. current-loop is not affected by 2ω-pulsation of voltage. One way to achieve this is, to make a separate current-loop control and voltage-loop control (see Fig. 2.14(b)) [Jung *et al.*, 2011]. However, in such schemes, the current-loop of the first-stage should be designed to get a very high gain at 2ω. This makes the real-time implementation challenging due to hardware limitations [Jung *et al.*, 2011]. Liu and Lai have proposed a dual-loop control method for the fuel-cell sourced DC-DC-AC converter [Liu and Lai, 2007a]. The Fig. 2.14(c) depicts the dual-loop control method. The basic concept of the ripple reduction proposed in [Liu and Lai, 2007a] is based on the bandwidth-shaping. Instead of making the independent current-loop and voltage-loop, the bandwidth (BW) of voltage-loop is reduced significantly. According to [Liu and Lai, 2007a], a reduction in the SHC ripple at the input can be achieved provided that the BWs of inner-loop and the outer-loop have a separation of half-decade (at least) from 2ω frequency. The basic idea is the minimization of SHC ripple component in the reference current of the inner-loop controller. However, the very low BW of the voltage-loop causes the poor system response at the load transients. Therefore, this method has a trade-off between the SHC ripple-reduction and dynamic performance. In Fig. 2.15, the effect of bandwidth of voltage-loop on the ripple-reduction and dynamic performance is depicted using simulation results. These results are presented for an $1-kW$ boost-derived DC-DC-AC converter having input voltage, 120 V; DC-link voltage, 380 V; $L = 1\ mH$; $C = 360\ \mu F$ and AC voltage 230 V, 50 Hz. In Fig. 2.15, the f_v and f_c are cut-off frequencies/BWs of voltage-loop and current-loop respectively. G_{vd} and G_{cd} are control to voltage and control to current transfer functions. Tv and T_c are closed-loop-gains of voltage-loop and current-loop respectively. The results of Fig. 2.15 are summarized in Table 2.3. Please see the Chapter 4 for the detailed analysis.

Table 2.3 : Comparison of Simulation Results of Fig. 2.15 for Different Values of f_v

Parameters	$f_v = 2.4Hz$	$f_v = 30Hz$	$f_v = 65Hz$
1) % 2ω-ripple in input current	4.5	21	125
2) %Overshoot/Undershoot in DC link voltage	+37/-29	+7.9/-10.5	+4.5/-4.7
3) Settling time (ms) of voltage at load application/ removal	600/250	130/50	20/10

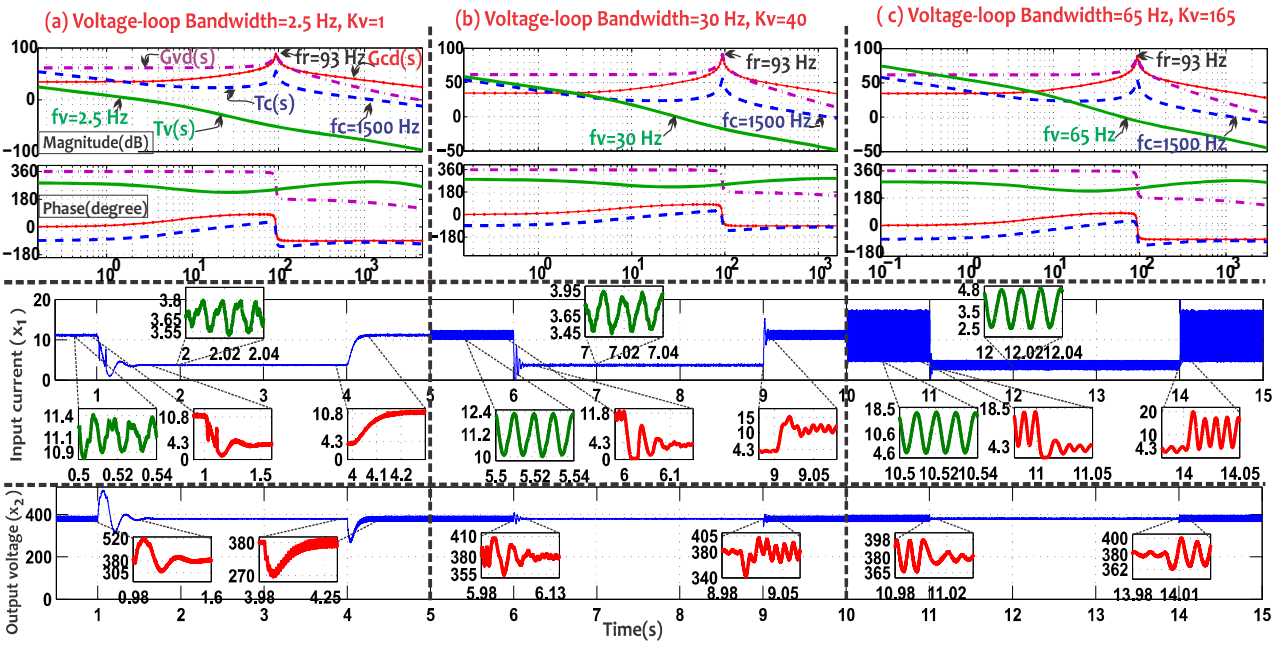

Figure 2.15 : Effect of the bandwidth of voltage-loop: there is trade-off between ripple-reduction and dynamic performance

Recently, 2ω-ripple problem is addressed in conjunction with the hybrid parameters of the DC-DC converter. These parameters relate the input-output behavior of DC-DC converter. A general input-output relation using the hybrid parameters of the two-port network (see Fig. 2.16) is given by [Wang *et al.*, 2014b],

$$\begin{bmatrix} \tilde{v}_o(s) \\ \tilde{i}_i(s) \end{bmatrix} = \begin{bmatrix} A_v(s) & Z_o(s) \\ Y_i(s) & A_i(s) \end{bmatrix} \begin{bmatrix} \tilde{v}_i(s) \\ \tilde{i}_o(s) \end{bmatrix} \tag{2.21}$$

$Z_o(s)$ and $Y_i(s)$ are output impedance and input admittance respectively, generally used for the stability analysis of the cascaded system. $A_o(s)$ is audio-susceptibility parameter used for the estimation of input-output noise-transmission and $A_i(s)$ is the back-current gain parameter. The parameters $Z_o(s)$ and $A_i(s)$ are used for the SHC ripple mitigation in the two-stage converters. However, $Z_o(s)$ parameter is widely explored in the output impedance shaping methods and a few methods have used $A_i(s)$ parameter (see Fig. 2.20) [Wang *et al.*, 2014b].

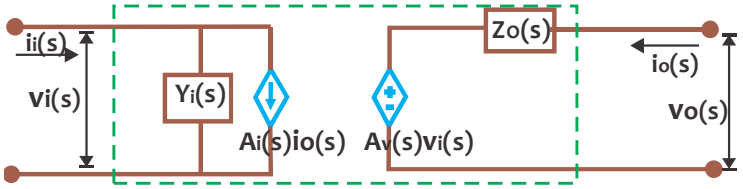

Figure 2.16 : Two-port network of DC-DC converter: Hybrid parameters

In the output-impedance shaping method, the control modifies the output-impedance of the front-end DC-DC converter such that the SHC ripple see more impedance in the direction of DC source than the DC-link capacitor branch. This method achieves the ripple-suppression at the input, however the control causes poor dynamic performance of system; the high output-impedance of system leads to poor system dynamics [Aldhaheri and Etemadi, 2017; D, 1976]. In

both the methods (i.e. dual-loop control method and output-impedance-shaping), there is a need to maintain the sufficient bandwidth of the voltage-loop throughout the desired frequency band of the operation.

Recently, some modified and improved control techniques have been proposed using the above mentioned concepts to minimize the SHC ripple at the DC input and to improve the system response simultaneously [Bojoi *et al.*, 2010; Chen *et al.*, 2014; Chiang *et al.*, 2016; Gu *et al.*, 2014; Jung *et al.*, 2011; Khajehoddin *et al.*, 2013; Ksiazek and Ordonez, 2014; Liu *et al.*, 2018; Wang *et al.*, 2014b; Zhang *et al.*, 2014, 2015, 2018b; Zhu *et al.*, 2015]. These control schemes use resonant filters, for instance, notch-filter (NF) or band-pass filter (BPF) in the current or voltage loop. The basic principle is to minimize the 2ω-ripple in the reference of input current or to sufficiently reduce the bandwidth of the voltage-loop at 2ω only while maintaining high bandwidth of the voltage-loop at the other frequencies. Nevertheless, the similar methods have been presented in the earlier work in the context of the power-factor correction (PFC) AC-DC converter [Mitwalli *et al.*, 1996; Prodic *et al.*, 2003; Sun *et al.*, 2016; Tang *et al.*, 2015a; Vitorino *et al.*, 2017]. It is to be noted that the focus of this work is limited to review the existing literature in the context of the DC-AC power converter or inverter. The bandpass filter (BPF) and notch filter (NF) are generally used to mitigate the SHC ripple without affecting the dynamic performance of the system. The characteristics of BPF and NF are shown in the Fig. 2.17(a) and Fig. 2.17(b) using the Bode-plot. The BPF allows to pass a certain

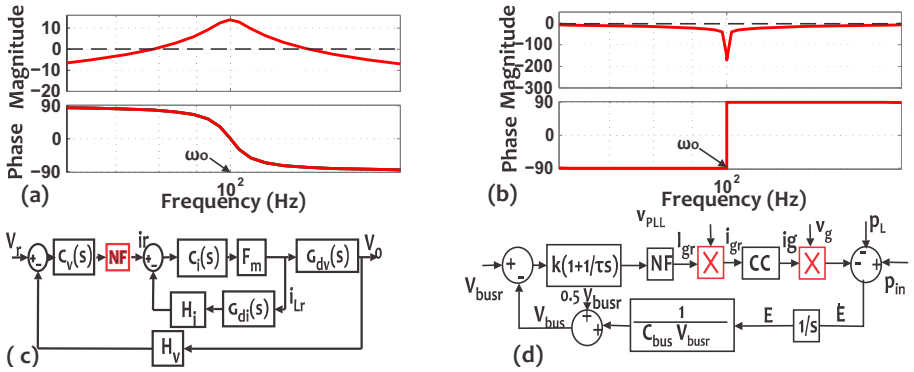

Figure 2.17 : (a) Bode plot of BPF (b) Bode plot of NF (c) NF-CR control scheme [ZhengWei *et al.*, 2012] (d) Control scheme based on NF proposed in [Khajehoddin *et al.*, 2013]

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range of the frequencies of the input signal. The output signal leads the input signal by $\pi/2$ *rad* in 0 to ω_o range and lags by $\pi/2$ *rad* beyond the ω_o. Therefore, a total of π *rad* phase-shift occurs for a transform of the input signal to the output signal. The NF filter has inverse characteristics of the BPF. The NF allows all the frequencies except the frequencies located in a very narrow range of the resonance frequency (ω_o). A notch-filter also gives a phase-change of π *rad* for a transform of the input signal to the output signal. However, the phase is negative for the frequencies below ω_o.

In [ZhengWei *et al.*, 2012], the authors have proposed NF-added to the voltage-loop in the dual-loop control for the front-end DC-DC converter. Here, a stand-alone operation of the two-stage DC-DC-AC is considered. The reference inductor current is generated by passing the output of voltage controller through NF. Therefore, the method is named as notch-filter inserted current reference (NF-CR) scheme. The control block-diagram is shown in the Fig. 2.17(c). The NF attenuates 2ω-signal in reference of the inductor current. This minimizes the SHC ripple in input current. In [Jung *et al.*, 2011], a control scheme is proposed for a grid-connected two-stage converter. A current controller is used with the first-stage and DC bus control is achieved by the grid-connected DC-AC converter. The method adopts a grid-side based 2ω-ripple compensation. A quasi-notch filter (quasi-NF) is added in the voltage-loop of the second-stage of the converter. The transfer

function of quasi-NF is,

$$G_{NF}(s) = \frac{s^2 + \frac{\omega_o}{Q_z}s + \omega_o^2}{s^2 + \frac{\omega_o}{Q_p}s + \omega_o^2} \tag{2.22}$$

Here, Quality factor, Q is related as $|Q|_{dB} = |Q_p|_{dB} - |Q_z|_{dB}$. $|Q_z|_{dB}$ and $|Q_p|_{dB}$ are the quality factors of zero and pole respectively. The quasi-NF provides a much smaller voltage-loop gain than the current-loop gain at 2ω. This minimizes the SHC ripple at the input. This method retains the good dynamic performance of the system at all other frequency except the neighborhood frequencies about and at 2ω. However, Q of the quasi-NF should be designed properly. Similar to [Jung *et al.*, 2011], an another grid-side based 2ω-ripple compensation is adopted in [Khajehoddin *et al.*, 2013]. The control scheme is shown in the Fig. 2.17(d). The control avoids the interaction of current-loop and voltage-loop at 2ω. However, the control design is involved to develop an LTI model from the time varying system model (see Fig. 2.17(d)); the two multiplications just before and after the current controller (CC) make model time varying. Furthermore, in a grid-connected system, maintaining the good performance of the phase-locked loop (PLL) is another challenge. All the three methods have used notch filter. The use of the notch-filter may introduce a significant negative phase-shift to the frequencies lower than the characteristic frequency of notch filter [Zhang *et al.*, 2014]. This may introduce instability to the system.

In [Zhang *et al.*, 2014], Zhang *et al*. have proposed a voltage mode control (VMC) based band-pass filter incorporated into the inductor feedback path for a buck-derived two-stage converter (see Fig. 2.18(a-c)). The method is based on the output-impedance shaping. In Fig. 2.18(a), a virtual impedance $(Z_v(s))$ is added in series with the inductor. The concept is, to increase the impedance of inductor branch at 2ω frequency such that the impedance of DC-link capacitor branch is less than the impedance of inductor branch. This compels the SHC ripple to pass through the capacitor instead of the inductor branch. Using Fig. 2.18(b), the impedance of the inductor branch

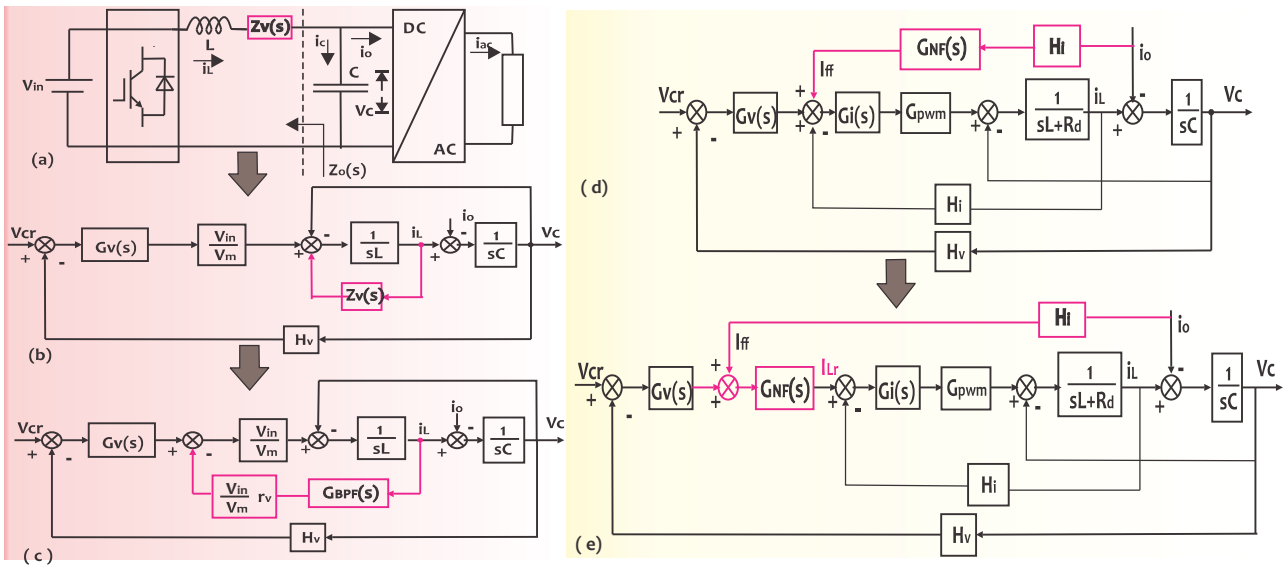

Figure 2.18 : (a)-(b)-(c) A BPF based control scheme proposed in [Zhang *et al.*, 2014] (d) NF-LCFFS and (e) NF-CR-LCFFS proposed in [Zhu *et al.*, 2015]. In Fig. 2.18 and Fig. 2.19, V_{in} input voltage, i_L inductor current, i_c capacitor current, i_o inverter input current, v_c DC-link capacitor voltage, R_d equivalent series resistance of inductor, R_c capacitor's ESR, G_{pwm} PWM transfer function, i_{Lr} reference inductor current, Z_o, Z_{o1} output impedances

is,

$$Z_o(s) = -\frac{v_c(s)}{i_L(s)} = \frac{sL + Z_v(s)}{1 + G_v(s)\frac{V_{in}}{V_m}H_v} \tag{2.23}$$

Here, G_v is voltage-loop controller, H_v is voltage sensor gain, V_m is PWM gain. $Z_v(s)$ is the virtual impedance added in the current feedback path. Suppose $Z_v(s)$ is a virtual resistance, *say* r_v. Therefore, the method can be named as virtual resistance scheme (VRS) [Zhang *et al.*, 2014]. In (2.23), an increase in $Z_o(s)$ is achieved by increasing the value of r_v. However, this decreases the magnitude of the loop-gain in the low frequency range [Vlatkovic *et al.*, 1992]. To balance this, the gain of $Gv(s)$ can be decreased. However, this reduces the bandwidth of voltage-loop and hence degrades the dynamic performance of the system. Therefore, there is a trade-off between the design of r_v and bandwidth of the voltage-loop. Eventually, the results are the same as of the dual-loop control of [Liu and Lai, 2007a]. This problem is solved by adding a BPF in the current feedback path instead of using a constant r_v only (see Fig. 2.18(c)). The BPF is tuned at 2ω and hence provides a high gain at 2ω only. This adds a high virtual impedance in series of inductor branch at 2ω. This reduces SHC ripple at the DC input without affecting the dynamic performance. However, adding a BPF leads a $-\pi/2$ to $\pi/2$ phase-rotation about the characteristic frequency of the BPF. This limits the bandwidth of voltage-loop. Therefore, in [Zhu *et al.*, 2015], Zhang *et al*. further extended their work to resolve the challenges of [Zhang *et al.*, 2014] by adopting the current mode control (CMC) approach for the buck-derived two-stage converter. The work has presented different improved control strategies. The first control strategy, namely notch filter-inserted load current feed-forward scheme (NF-LCFFS), is realized by adding an NF in the load current in a feed-forward way (see Fig. 2.18(d)). It is worth noting that the load current feed-forward control schemes improve the dynamic performance at the load-transients [Redl and Sokal, 1986]. Therefore, the dynamic performance of the system is better. The NF attenuates the 2ω-ripple in the current-loop, therefore the SHC ripple reduces at the input of the two-stage converter. However, the voltage-loop in the Fig. 2.18(d) may contaminate the reference current of the inner-loop. Therefore, a further improvement is proposed by merging NF-CR scheme of [ZhengWei *et al.*, 2012] with the NF-LCFFS, and hence called NF-CR+LCFFS. It is worth to note that the NF-CR scheme has an NF already to minimize 2ω-ripple from the current reference of the inner-loop. A simplified block diagram is shown in the Fig. 2.18(e) where the two NFs are transformed to one. A single NF added at the output of the summing point after the voltage controller eliminates the requirement of the two NFs. This scheme almost eliminates the SHC ripple and also improves the dynamic performance of the system. However, the feed-forward schemes are susceptible to the disturbances and lack of the robustness as mentioned before. Moreover, NF may induce instability to the system as it affects the bandwidth of the voltage-loop. A detailed analysis and comparison of the control schemes of [Zhang *et al.*, 2014] and [Zhu *et al.*, 2015] are presented in [Zhang *et al.*, 2015]. A voltage control mode based load-current feed-forward scheme (VMC-LCFFS) is proposed in [Shi *et al.*, 2016b]. The control block-diagram of the VMC-LCFFS is shown in the Fig. 2.19(a). The SHC ripple reduction utilizes the concept of modification in the reference value of DC-bus voltage in agreement with the desired pulsation in the DC bus voltage at 2ω. This makes DC-bus capacitor to have nearly all the SHC ripple. It is to be noted that the bus voltage is no longer constant but pulsates at 2ω (due to the addition of ΔV_{cr} term with V_r). A BPF is required with the load current feed-forward path to take-out the SHC ripple from the load current (i_o) which then generates a desired ΔV_{cr} that is to be added in V_r. The presence of integrator in the LCFFS path result into continuous integration action. This results into the rapid growth of the DC-bias in the LCFFS controller that leads to incorrect voltage tracking. Therefore, a high-pass filter (HPF) is also added at the end of LCFF path (see Fig. 2.19(b)). The scheme minimizes the SHC ripple while retaining the good dynamic performance. However, the control design is involved and the control of the VMC-LCFFS depends on the accuracy of the system parameters. A simple CMC-based control method for the said problem is proposed in [Bojoi *et al.*, 2010]. This control scheme is similar to the control scheme proposed in [Shi *et al.*, 2016b].

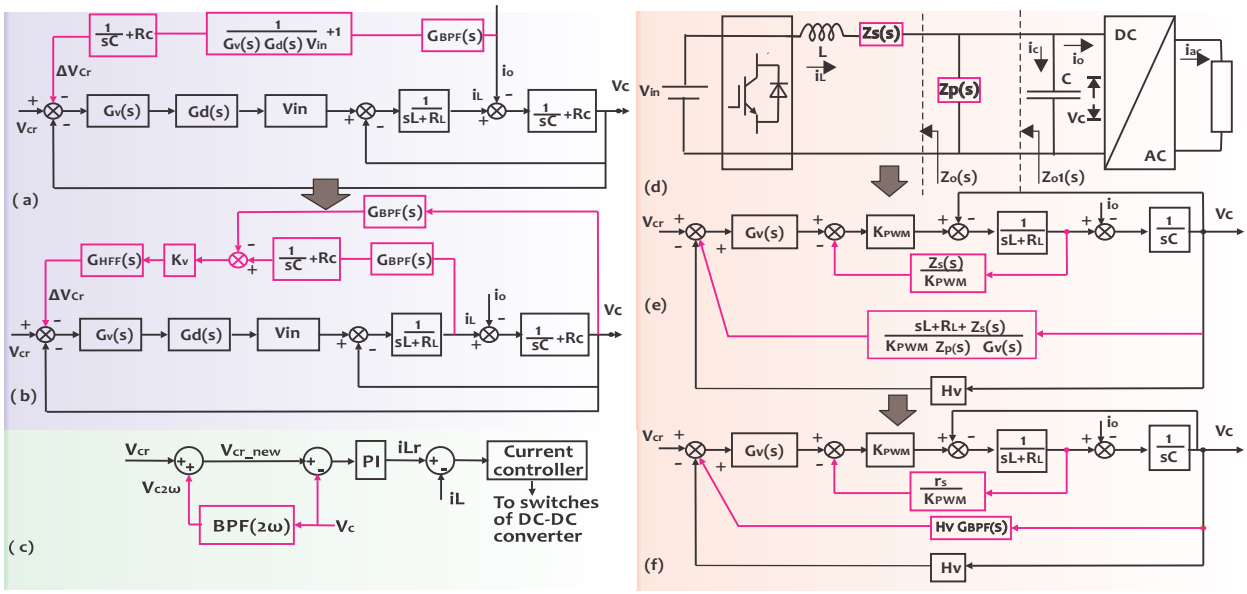

Figure 2.19 : (a)-(b) VMC-LCFFS proposed in [Shi *et al.*, 2016b] (c) CMC-based control scheme proposed in [Bojoi *et al.*, 2010] and (d)-(e)-(f) BPF-CVFS proposed in [Zhang *et al.*, 2015].

The control block diagram is shown in the Fig. 2.19(c). The DC-link voltage reference is modified by adding $V_{c_{2\omega}}$. The $V_{c_{2\omega}}$ is extracted by passing the DC-link voltage through a BPF. The modified reference voltage $V_{cr_{new}}$ having 2ω voltage ripple cancels 2ω-voltage ripple of the actual DC-link voltage (v_c). This results in a ripple-free current reference in the current control-loop. However, the use of BPF in control scheme limits the bandwidth of voltage-loop. A comparison of these control schemes is given in the [Zhang *et al.*, 2015] in the perspective of the output-impedance shaping. A similar control scheme i.e. BPF-incorporated capacitor voltage feedback scheme (BPF-CVFS) as presented in [Bojoi *et al.*, 2010] is discussed in [Zhang *et al.*, 2015]. However, this control scheme is based on VMC method unlike the CMC method of [Bojoi *et al.*, 2010]. The block-diagram of BPF-CVFS is shown in the Fig. 2.19(d-f). These all control schemes of [Zhang *et al.*, 2014; Zhu *et al.*, 2015] are discussed for a buck-derived DC-DC-AC converter. These schemes are further explored for the boost converter in [Zhang *et al.*, 2018b].

An effective use of the NF and BPF is proposed in [Wang *et al.*, 2014b] with the back-current gain based approach (using $A_i(s)$). The control block-diagrams are shown in the Fig. 2.20(a-b). $A_i(s)$

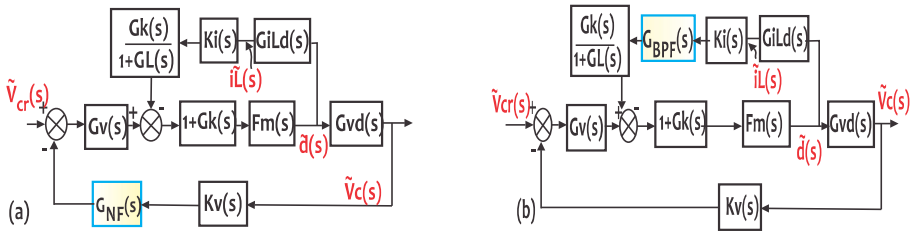

Figure 2.20 : Back-current gain based scheme with (a) NF (b) BPF

relates input current $(i_{in}(s)$ with the output current $(i_o(s)$ of a system (e.g. DC-DC converter). In [Wang *et al.*, 2014b], it is established that for a VMC based control, the voltage-loop has a little effect on the 2ω-ripple attenuation. However, the 2ω ripple reduction can be achieved for $\omega_o < 2\omega$. ω_o is the resonance frequency of LC circuit of the DC-DC converter. This is achieved by using average

CMC scheme. However, this scheme also trade-off between ripple-reduction and dynamic performance. Therefore, further improvements in the back-current gain control scheme are made using (i) NF embedded in the voltage feedback branch and (ii) BPF embedded in the current feedback branch.

An SHC-ripple mitigation technique is proposed in [Liu *et al.*, 2014] for a fuel-cell sourced current-fed dual half bridge (CF-DHB) converter. A phase-shift control scheme is adopted that regulates the DC voltage and minimize the SHC ripple. The optimized duty is set to 0.5. The PI controls the DC-link voltage and a proportional resonant (PR) controller (tuned at 2ω) suppresses 2ω ripple at the source. The PR controller modifies the main phase-shift angle to eliminates the input current ripple. The PR controller is similar to an integrator having infinite DC gain at characteristic frequency. The integral behavior of the PR may slow down the system dynamics. Tuning PR to very low ω_o forces a difficult implementation of it on the low cost controller board (such as 16-bit DSP) [Teodorescu *et al.*, 2006]. In [Xue *et al.*, 2015], authors have proposed a sinusoidal charging scheme for the dual-active-bridge based Si-charger and GaN-charger with the reduction in size of the capacitor at the DC-link using resonant controller and rotating frame control approach. The objective is achieved by injecting 2ω-ripple into the battery for the charging purpose. The size of DC-link capacitor decreases to 84% for Si-charger and 90% for GaN charger. However, this advantage comes after the ripple injection to the battery. The recent studies have addressed several detrimental effects of 2ω-ripple on the battery life [He *et al.*, 2014]. Therefore, a long-term testing is needed for such schemes. In [Liu *et al.*, 2018], Liu *et al*. have proposed a novel ripple compensator for a boost-derived-PV grid-connected inverter with battery-storage. The control scheme utilizes a double channel current feedback control to minimize the SHC ripple in the input current. The basic idea is to regulate the 2ω-voltage ripple in the DC-link voltage by adding a small disturbance of 2ω (*say* D_f) in the average duty (D_o). The Fig. 2.21(a) shows the control block-diagram. In the Fig. 2.21(a), G_f is a third-order general integrator (ToGI) filter (see Fig. 2.21(b)) to extract 2ω-component. A grid-side based bus voltage control is adopted. The voltage error of

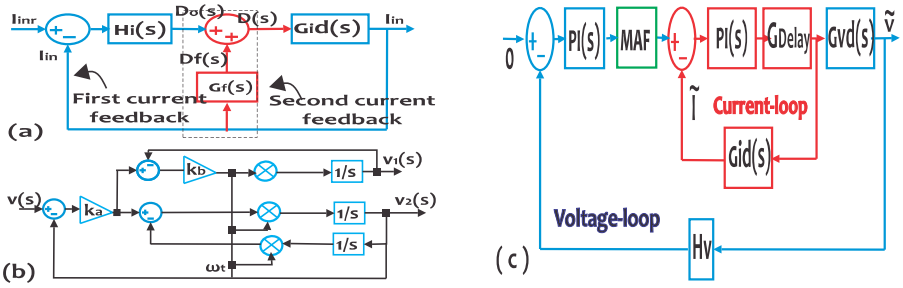

Figure 2.21 : (a) Double input feedback and (b) third-order general integrator proposed in [Liu *et al.*, 2018] (c) MAF based dual-loop control proposed in [Shi *et al.*, 2018]

voltage-loop is passed through an NF. This eliminates the 2ω-component from the grid-side current reference. The current-error in the current-loop of the bus-voltage control is passed through proportional-resonant controller, this control the sinusoidal waveform of the grid current. A gain is multiplied with the output of G_f to regulate the value of 2ω-ripple. A large value of the gain minimizes the SHC ripple. However, this may induce instability to the system. Therefore, there is a trade-off between the stability and the ripple-reduction using a current feedback in the double-channel current feedback control. Use of multiple integrator in the 2ω ripple-filter design may slow down the system dynamics. In [Shi *et al.*, 2018], authors have proposed a dual-loop control for the boost-derived two-stage converter. The control scheme uses a moving average filter (MAF) in the voltage-loop to make the voltage-loop gain very low at 2ω. The control block diagram is shown in the Fig. 2.21(c). This scheme is similar to NF-CR of [ZhengWei *et al.*, 2012]. However, unlike NF-CR, this scheme can attenuates multiple of 2ω as well. In [Ksiazek and Ordonez, 2014],

another control scheme based on the MAF is proposed to control the swinging bus. The MAF has several advantages such as fastest step response, easy to implement using low-cost control-board, reduces random noise and notches the multiple of 2ω. However, the performance of MAF based on time-domain is better than the frequency-domain.

ZSI, quasi-ZSI, quasi-SBI eliminates the requirement of the multiple stages. These can boost the input voltage and are capable of the shoot-through operation. In [Zhou *et al.*, 2016], authors have proposed a modified shoot-through duty based unipolar-SPWM technique as shown in the Fig. 2.22(b). The conventional technique is shown in the Fig. 2.22(a). The control forces the volt-

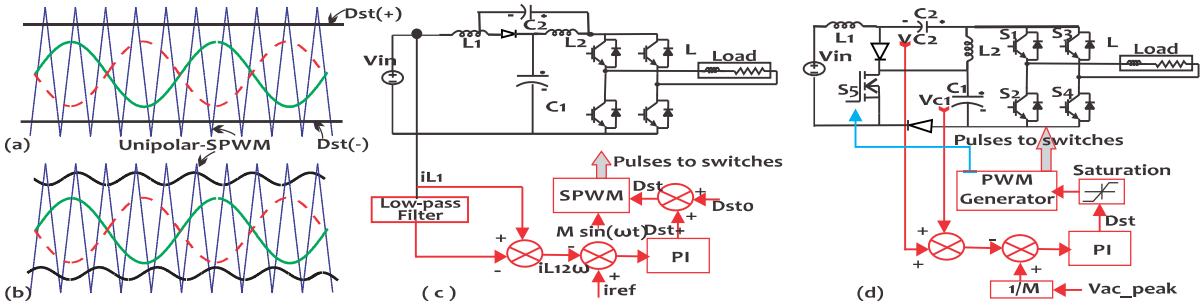

Figure 2.22 : (a) Conventional shoot-through duty based-unipolar SPWM proposed (b) Modified shoot-through duty based-unipolar SPWM proposed in [Zhou *et al.*, 2016] (c) The low-pass filter based control scheme proposed in [Ge *et al.*, 2016a] (d) control scheme proposed in [Nguyen *et al.*, 2018a]

age across the capacitors of the quasi-ZSI network to swing at 2ω or to store the all 2ω-decoupling power. This reduces the ripple at the DC input. However, in comparison to conventional method, the modified scheme introduces more voltage stress on the switches i.e. 53% more than conventional scheme. An optimum design of the quasi-ZSI network parameters is given in [Ge *et al.*, 2016a]. However, a part of the SHC ripple still flows through the quasi-ZSI network. The inductors store the decoupling power temporarily. It is better to transfer the stored decoupling power to capacitors; the power density of the capacitor is higher than inductor. Therefore, a PI regulator based control scheme is proposed in [Ge *et al.*, 2016a]; the control scheme is shown in the Fig. 2.22(c). The input current is passed through a low pass filter. This gives the DC current component which then subtracted from the actual input current to give SHC ripple. A PI controller generates the required pulsation in the equivalent shoot-through duty. The control scheme confines the ripple in the capacitors and minimizes in the inductor current and input current. However, this method has a trade-off between stability and speed of response. In [Nguyen *et al.*, 2018a], a new quasi-SBI topology for the high voltage gain with a benefit of SHC ripple minimization is proposed. A thorough study is carried out to design the impedance network. A control scheme is added to keep the input free of ripple. The control method is shown in the Fig. 2.22(d). The voltages of the capacitors are added and then subtracted from the reference voltage. The DC-link voltage reference is generated based on the output voltage and modulation index. The voltage error is regulated to generate desired shoot-through duty. The application of this topology is limited to the low-power applications. The components count is more than the conventional quasi-SBI.

Most of the above discussed control schemes implement a linear control. The linear control establishes stability close to operating point only. Generally, in the RE energy systems, the large disturbances are frequent or very uncertain. Therefore, further improved and non-linear control approaches are proposed recently. In [Ahmad *et al.*, 2012], authors have proposed a dual-loop control method for the boost-derived-DC-DC-AC converter (see Fig. 2.23(a)). The ripple-reduction is achieved by adopting the output-impedance shaping. The control utilizes a sampled series feed-

back as the inner-loop. The series-feedback increases the output-impedance of front-end converter. A parallel feedback is added as outer-loop to regulate the DC-link voltage. However, the two feedback channels impose trade-off between the system dynamics and the ripple-reduction. Therefore, a non-linear compensator is added in between the voltage-error generation point and current controller. The non-linear compensator gives high gain at the load-transients to compensate the undershoot/overshoot in the DC-link voltage. However, the gain of the non-linear compensator may rise to very high value and also an abrupt change in the gain may induce instability to the system. Therefore, a fine design of the non-linear compensator is required. A swing bus-voltage control is proposed in [Galvez and Ordonez, 2015] for a stand-alone fuel-cell buck-derived two-stage converter. A nonlinear natural switching surface (NSS) based boundary control takes care of the very large input voltage-swing at 2ω. The controller minimizes the DC-link voltage swing and hence distortion in the output AC voltage. However, the practical implementation of such discontinuous variable frequency schemes based on the sliding mode control may introduce chattering effect in the switching [Bartolini *et al.*, 2000]. A fixed-frequency PWM-based SMC minimizes the chattering effect. In [Gautam *et al.*, 2018], authors have proposed an adaptive switching function to minimize the SHC ripple at the input of the boost-derived two-stage converter using the fixed-frequency based-SMC. The switching function is a combination of the inductor current error (e_1) and α times voltage error (e_2). α is power function of the e_2 i.e. $\alpha = \psi e_2^{\beta}$. β and ψ are design parameters. The profile of α is shown in the Fig. 2.23(b). For a very small value of α, the output-impedance is high, hence the ripple reduces at the input. At the line-load transients, α changes monotonically to converge the system dynamics at a faster rate. However, during the transients the Z_{out} decreases, this may inject the ripple to the DC source.

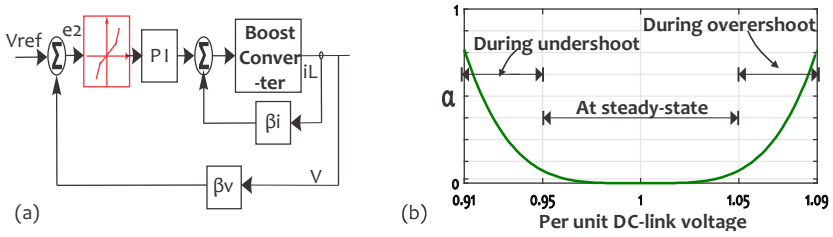

Figure 2.23 : (a) Non-linear compensator technique proposed in [Ahmad *et al.*, 2012] (b) Adaptive-SMC based ripple-mitigation technique proposed in [Gautam *et al.*, 2018]

It is to be noted that the control schemes presented in this Section still require a large size capacitor or an optimized value of the capacitance at the DC-link at the input-end of DC-AC converter [Zhang *et al.*, 2018a]. The decrease in the SHC ripple at the input of converter results in the increased second-order pulsation at the DC-bus/DC-link. The pulsation at the DC-link are kept within the desired limit by choosing an optimum size of DC-link capacitor. Though the system performance at the line-load transients is better despite the optimum size of the DC-link capacitor which is achieved by different linear or nonlinear control approaches, however, the allowed variation in the DC-link voltage may cause increased THD level. To further minimize or eliminate the 2ω-pulsation in the voltage at the DC-link, an auxiliary circuit or active filter is added. In the next subsection, two-stage DC-DC-AC converter with the auxiliary circuit or with the external active filter are discussed.

Control-Oriented Compensation Techniques with Auxiliary or Extra Active Filter

In this section, active decoupling methods for the two-stage converters with isolation and withput isolation are discussed. In [Wai and Lin, 2010], an active filter circuit connected at DC bus as shown in the Fig. 2.24(a) is proposed for the boost-derived two-stage converter. This filter is similar to the filter proposed in [Christidis *et al.*, 2016]. An SMC based nonlinear control

techniques is used in [Wai and Lin, 2010]. The sliding mode controller regulates the active filter such that the filter injects a suitable compensation current in the DC-bus to cancel the effect of the 2ω-ripple. The compensation current is generated using ADLINE neural filter. However, the design of the neural filter is a challenge. The voltage of the C_b in the Fig. 2.24(a) should kept higher than the DC-bus voltage. Therefore, the system has a higher voltage than DC-link that causes the safety concern. A block diagram of the 360 W-Texas Instruments UCC28180EVM-573 front-end evaluation board integrated with the buck-boost type bidirectional active filter is shown in the Fig. 2.24(b) [Mellincovsky *et al.*, 2017a, 2018]. To control the active filter, a multiresonant direct voltage regulation technique is used to decouple the 2ω-power ripple at the DC-link. The control

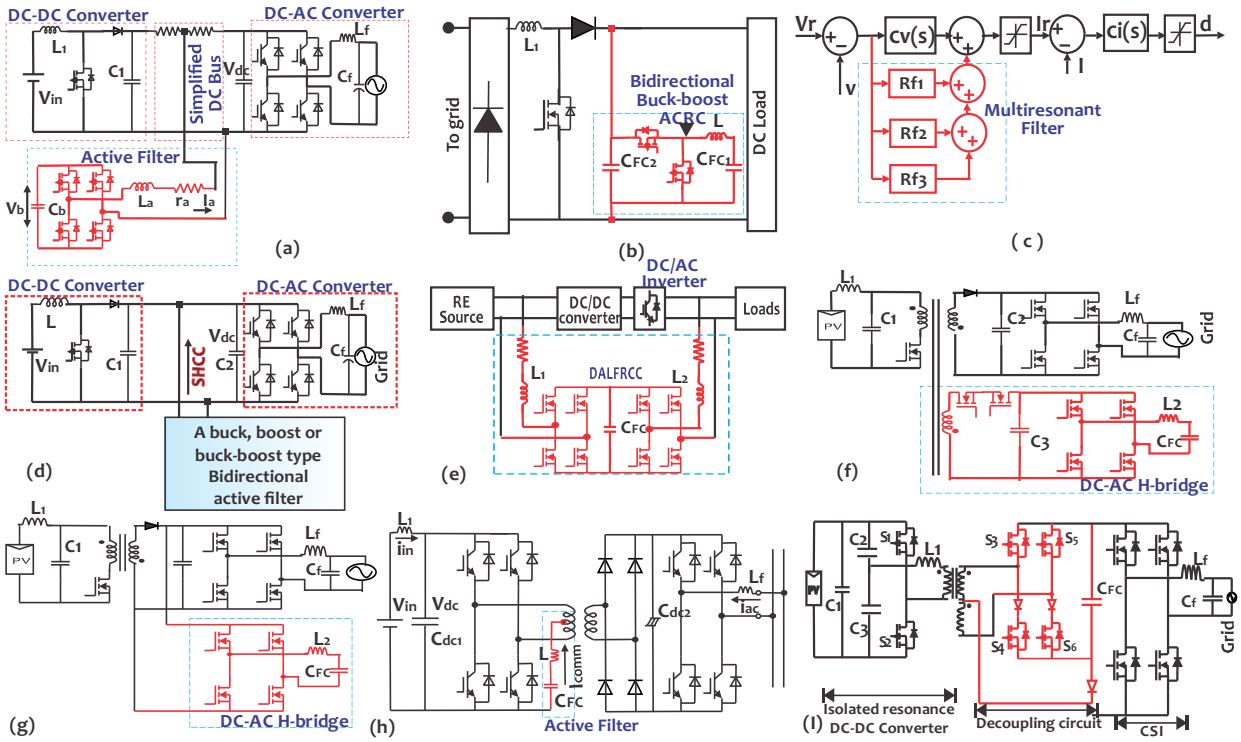

Figure 2.24 : (a) Active filter proposed in [Wai and Lin, 2010] (b) Active filter proposed in [Mellincovsky *et al.*, 2017a, 2018] (c) Control scheme for active filter proposed in [Mellincovsky *et al.*, 2018] (d) Active filter proposed in [Zhang *et al.*, 2018a] (e) DALFRCC [Wai and Lin, 2011] (f) integrated H-bridge active filter and (g) auxiliary winding based H-bridge active filter proposed in [Harb *et al.*, 2013] (h) Common-mode operation based technique for half-active bridge proposed in [i. Itoh and Hayashi, 2010] (i) DC to single-phase AC grid-connected converter[Watanabe and Itoh, 2017]

scheme makes the active filter to mimic an infinite capacitance parallel to the DC-link. The active filter is controlled using a modified dual-loop control scheme as shown in the Fig. 2.24(c). The parallel resonant filters tuned at the multiple of 2ω are added in the voltage-loop. The filters attenuate multiple of 2ω components from the reference current of inner-loop. The multiresonant resonant filters are similar to MAF used in [Krein *et al.*, 2012]. The control scheme affects the grid frequency. At the load-transients, the voltages across the DC-link capacitor and active filter side capacitor show abnormal behavior and hence the load-transient behavior of the system is a challenge. For the circuit of active filter (buck/boost/buck-boost type) shown in the Fig. 2.24(d), an one-cycle control method has been proposed in [Zhang *et al.*, 2018a]. The switches of active filter are controlled such that per cycle average value of the current at the output of the active filter tracks 2ω-current ripple at the DC-link. The control utilizes the peak-value of ripple storage capacitor, therefore a peak detector is required to realize the peak voltage control. A bidirectional dual-active

low frequency ripple control circuit (DALFRCC) shown in the Fig. 2.24(e) can alleviate the ripple from the input and a 90% compensation of SHC voltage ripple at DC-bus can be achieved [Wai and Lin, 2011]. However, the active filter has eight switches. This makes the system costly and complex. Additionally, two linear neural filters are used to generate the compensation current commands corresponding to i_a and i_b (see in Fig. 2.24(e)). A sliding mode controller is proposed for the injection of compensation currents at DC bus and AC output terminal. However, design of the neural filters is complex and a challenge. The integrated and auxiliary winding based inverter topologies as shown in the Fig. 2.24(f) and Fig. 2.24(g) respectively are proposed in [Harb *et al.*, 2013]. The active filter or ripple-port are the H-bridge inverter. The control scheme is based on the power ripple balancing given by (2.10)-(2.15). The SPWM technique is used for the main inverter and ripple-port DC-AC converter. The active filter eliminates the large E-cap. However, the number of switching devices is increased. In [i. Itoh and Hayashi, 2010], an economical active filter with no extra switching devices is proposed for an isolated half-active bridge two-stage DC-DC-AC converter. In the Fig. 2.24(h), the main circuit with active filter is shown. An LC filter circuit is connected between the center-taping connection point of the primary winding of the transformer and the return wire of the active-bridge at primary. The control scheme of LC filter is based on the common mode operation method. The control scheme reduces the size of the capacitor at the DC link and also the switching devices are the same as used in the conventional system. However, the rating of the switching devices is increased due to the flow of the active filter current in the transformer and the first-stage of the converter. The control of the active filter limits the transformation ratio of the transformer. Fig. 2.24(i) shows a circuit of a resonance type DC-DC converter, power decoupling circuit and current source inverter (CSI). The control scheme achieves a power decoupling by controlling the charging and discharging of the buffer capacitor (C_{FC}) such that the input power is equal to the output power. Therefore, the input is ripple-free while C_{FC} takes all the pulsation. The resonance type DC-DC converter makes a series resonance circuit. The quality factor of this circuit should be kept very high in order to ensure stability. To improve the efficiency of the system, the size of the inductor in the resonating circuit should be decreased.

2.3.4 Some Other Topologies and Techniques

In Fig. 2.25(a-c), the buck, boost and buck-boost differential inverter (DI) topologies are shown respectively [Xu *et al.*, 2018; Yao *et al.*, 2015; Zhu *et al.*, 2013]. In [Yao *et al.*, 2018], a generalized power decoupling method is proposed for the differential inverters with the non-linear load. Firstly, a generalized ripple-mitigation analysis is presented based on the waveform control method. Secondly, a feedback-linearization based control is proposed for the differential inverters to eliminate the non-linearity of the boost and buck-boost type differencial inverters. To mitigate the $2\omega-$ripple problem, a similar method as proposed in [Mellincovsky *et al.*, 2018] using multiresonant filter is proposed. According to analysis presented in [Yao *et al.*, 2018], the buck-type DI has lowest switch voltage stress and small decoupling capacitor. However, the DC-link voltage should be kept high in such topology. The boost-type DI requires low DC-link voltage. However, the voltage stress on the capacitors and current stress on the switches are high. The buck-boost type DI achieves the lowest DC-link voltage requirement and it can compensate the most of the harmonics. However, this topology suffers the highest switch-voltage stress. In [Zhu *et al.*, 2013], authors have proposed a waveform-control (WFC) method [Jang and Agelidis, 2010] based ripple-mitigation in the fuel-cell sourced differential boost inverter [Caceres and Barbi, 1999] as shown in the Fig. 2.25(b). A brief of the WFC is as follows [Zhu *et al.*, 2013],
In the Fig. 2.25(b), the voltage across the AC load is given by the sum of the voltages across the capacitors v_{c1} and v_{c2}. The two voltages are out of the phase. This implies,

$$v_{c1} = V_{off} + 0.5V_m sin(\omega t) \tag{2.24a}$$
$$v_{c2} = V_{off} + 0.5V_m sin(\omega t - \pi) \tag{2.24b}$$

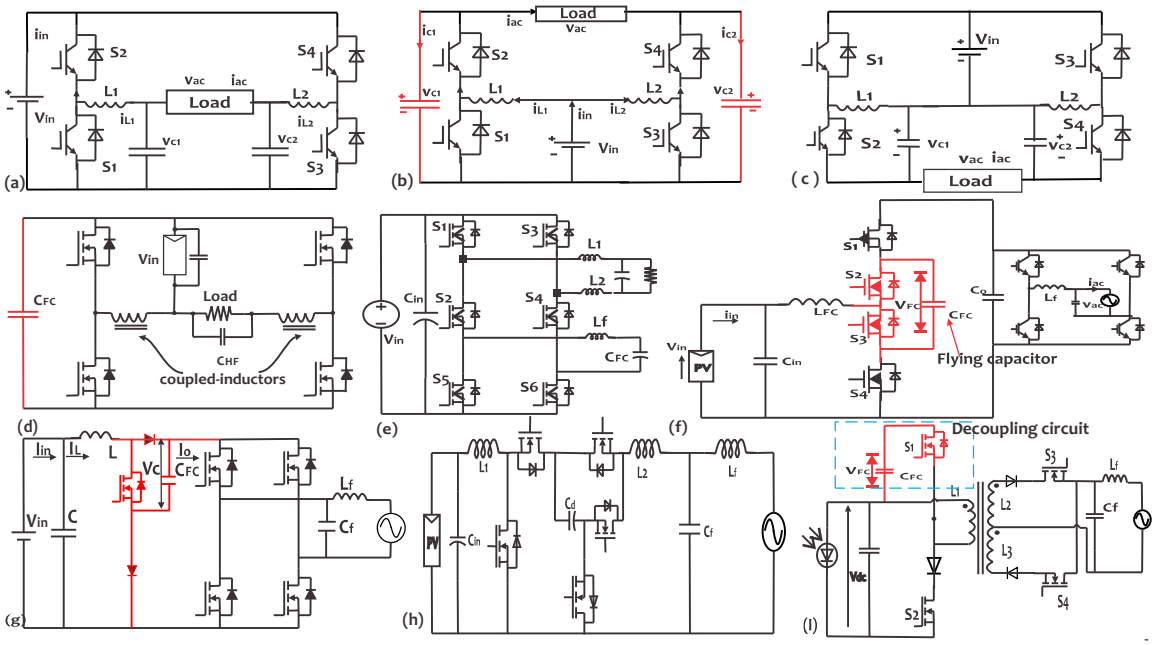

Figure 2.25 : Some other topologies and ripple mitigation techniques:(a) Buck-type differential inverter (b) Boost-type differential inverter (c) Buck-Boost-type differential inverters (d) Coupled-inductor based PV inverter (e) Six-switch topology (f) Flying capacitor based topology (g) Modified-boost-derived two-stage converter (h) Cuk converter based five-switch single-phase inverter (i) Flyback type single-phase utility interactive inverter

Here, V_{off} is offset-voltage of capacitors. V_m is maximum value of output AC voltage (v_{ac}) and ω is angular frequency of AC power supply. The instantaneous output AC voltage is,

$$v_{ac} = v_{c1} - v_{c2} = V_m sin(\omega t) \tag{2.25}$$

The basic idea of ripple-reduction is to reshape the waveform of voltages across the capacitors without affecting the output AC voltage. For this, a function $x(t)$ is added in (2.24) as follows,

$$v_{c1} = V_{off} + 0.5V_m sin(\omega t) + x(t) \tag{2.26a}$$
$$v_{c2} = V_{off} + 0.5V_m sin(\omega t - \pi) + x(t) \tag{2.26b}$$

Suppose $x(t) = Xsin(2\omega t + \phi)$ with amplitude X and a phase ϕ with respect to the reference. For $C_1 = C_2 = C$, the current through the capacitors are,

$$i_{c1} = 0.5\omega CV_m cos(\omega t) + 2\omega CX cos(2\omega t + \phi) \tag{2.27a}$$
$$i_{c2} = -0.5\omega CV_m cos(\omega t) + 2\omega CX cos(2\omega t + \phi) \tag{2.27b}$$

In the Fig. 2.25(b), the input current (i_{in}) is,

$$i_{in} = i_{L1} + i_{L2} \tag{2.28}$$

Here, $i_{L1} = \frac{i_{ac}+i_{c1}}{1-D_1} = \frac{(i_{ac}+i_{c1})v_{c1}}{v_{in}}$ and $i_{L2} = \frac{i_{ac}+i_{c2}}{1-D_2} = \frac{(i_{ac}+i_{c2})v_{c2}}{v_{in}}$, where $i_{ac} = I_m sin(\omega t)$ and D_1 and D_2 are the duty cycles of the switches S_1 and S_3 respectively. Using these in (2.28) gives,

$$i_{in} = \frac{V_m I_m + 2\omega X^2 C sin(4\omega t + \phi) - V_m I_m cos(2\omega t) + 0.5\omega CV_m^2 sin(2\omega t) + 8\omega XCV_{off} cos(2\omega t + \phi)}{2V_{in}} \tag{2.29}$$

To eliminate 2ω-ripple from the input current, 2ω-component of (2.29) should be zero. This gives,

$$X = \frac{V_m\sqrt{I_m^2+(0.5\omega V_m C)^2}}{8\omega V_{off} C} \tag{2.30a}$$

$$\phi = 0.5\pi - sin^{-1}\frac{I_m}{\sqrt{I_m^2+(0.5\omega V_m C)^2}} \tag{2.30b}$$

The waveform control method does not add extra circuitry to the system for ripple-mitigation. However, the tolerance of capacitors and inductors may affect the performance of WFC method [Abeywardana *et al.*, 2016b]. An improved version of the WFC is proposed in [Abeywardana *et al.*, 2016b] applying a rule based control (RBC) method on the WFC. In the RBC, the values of X and ϕ are perturbed accordingly to achieve ripple mitigation despite the variations in system parameters (inductors and capacitors). However, in the RBC, a large perturbation may lead to the poor performance of ripple-reduction and very small perturbation may affect the dynamic performance of the system. To get rid-off dependence of WFC on the system components, authors of [Abeywardana *et al.*, 2016b] further proposed an input current feedback control method in [Abeywardana *et al.*, 2016a]. The ripple-reduction method is based on the dual-loop control scheme similar to NF-CR-LCFFS proposed in [Zhu *et al.*, 2015]. In [Xia *et al.*, 2017b], a coupled-inductor based PV inverter with an advantage of the power decoupling is proposed. The circuit of this topology is shown in the Fig. 2.25(d) which is the variant of inverter proposed in [Xia *et al.*, 2017a]. An input voltage high bandwidth controller is proposed for this circuit to keep 2ω-ripple in the capacitor (C_{FC}). This results in the ripple-free input voltage. In this topology, the common-mode leakage is a problem due to its transformer-less configuration. In [Liu *et al.*, 2011], a six-switch topology is proposed. The proposed topology is shown in the Fig. 2.25(e). This topology has a combined feature of the inverter and rectifier. The switch S_2 is shared by rectifier and inverter both. The phase difference of modulation references are varied to achieve 2ω-ripple reduction at the DC link. However, in this topology, the phase difference is constrained by the input and output unlike the conventional topology where the phase difference can be kept between $-\pi$ *rad* to $+\pi$ *rad*. The conventional front-end DC-DC boost converter in a two-stage converter can be modified into a flying capacitor DC-DC converter to replace the large size electrolytic capacitor with the film capacitor [Watanabe *et al.*, 2018]. The circuit diagram of the flying capacitor based topology is shown in the Fig. 2.25(f). The flying capacitor (C_{FC}) in the circuit of the Fig. 2.25(f) can be used for the voltage boosting and 2ω-power-decoupling. The control scheme forces the voltage of the flying capacitor to fluctuate at 2ω to decouple the ripple. This minimizes DC-link voltage fluctuation. However, a PI controller is used for the purpose whose gain should be adjusted to handle the load-transients. Therefore, further optimization in the control design is required. An another modified version of the boost-derived two-stage converter is proposed in [Ohnuma *et al.*, 2015]. The circuit diagram is shown in the Fig. 2.25(g). There are four switching modes of the operation. In the first and fourth modes, the modified boost-circuit functions like the conventional boost converter. In the second mode, the buffer capacitor is charged with the required decoupling energy and in the third mode, the stored energy is supplied to the inverter-load. Therefore, the DC-link capacitor is not required to supply the 2ω-ripple power. This makes the DC-link ripple-free. However, at the high switching frequency, the switching loss increases due to extra diode. In [Jamatia *et al.*, 2016a], authors have proposed a five-switch single-phase inverter topology for 2ω-ripple-mitigation. The proposed topology is based on the Cuk converter. The circuit diagram is shown in the Fig. 2.25(h). The interaction between input and output is avoided using a switching sequence to decouple the ripple at the input. However, the circuit contains more number of the components in comparison to the conventional inverter. A flyback type single-phase utility interactive inverter with the power-decoupling capability is proposed in [Shimizu *et al.*, 2006]. The control achieves the ripple-free input current by storing the decoupling power in the capacitor, C_{FC} of the circuit in Fig. 2.25(i). The proposed topology is simple, cost-effective and small in the size. However, an optimum design is required for C_{FC}, V_c and L_1 to perform the boost-operation and power-decoupling.

2.4 CONCLUSIVE DISCUSSION AND OPEN CHALLENGES

This Chapter has reviewed several power decoupling techniques based on the passive power decoupling techniques, and active power decoupling techniques and its subcategory nominated as control-oriented compensation techniques for the single-phase inverters. The work is summarized in the Table 2.4-Table 2.7. The Tables tabulate several power-decoupling techniques, their merits and demerits, and involved challenges.

The PPTs utilizes passive components (L,C) for the power decoupling. Use of E-cap is the most simple and conventional technique. Other than the cost, size and weight of E-cap, the reliability of E-cap is a major concern. Even though the film-capacitor minimizes the reliability problem, it adds the cost, weight and size to the system. The use of film capacitor with the power-electronics circuit as the active filter gives one of the best possible solutions to eliminate E-cap. A comparatively small size film capacitor is used in the APTs. The APTs can be applied to the DC-side and AC-side or mixed-type applications. The DC-side application of APTs is easy and does not affect the H-bridge circuit. However, the control scheme should be designed accordingly. The basic control approach is, to balance the decoupling power at the DC-link by the power exchange with the film capacitor. The AC side APT is comparatively better on the basis of the efficiency of system due to its application at the AC side itself. However, the application of these techniques interfere the main H-bridge circuit. This modifies the modulation index of the inverter. This may lead to under-utilization of the power-electronics devices and increased stress on the components. The control is also a challenge. In both DC side and AC-side applications of the APTs, the number of the components increases. This reduces the over-all efficiency of the system and increases the size, cost and complexity of the control method.

The two-stage DC-DC-AC converters and the single-stage converters with front-end control-capability have inbuilt option of the active control. The front-end DC-DC converter can be utilized for the input SHC ripple-mitigation purpose. The software based control-oriented compensation techniques (CCTs) are generally utilized in such systems. The dual-loop control scheme and output-impedance shaping scheme are two popular CCTs. The former scheme aims to minimize the SHC ripple in the reference current of the inner-loop in order to compensate the SHC ripple in the input current by significantly reducing the bandwidth of voltage-loop. The later scheme aims to increase the output impedance of the front-end converter such that the SHC ripple is forced to flow through the DC-link capacitor branch. However, both the schemes suffer the poor dynamic performance. The addition of resonant filter in the current or voltage loop has shown improved dynamic performance. The addition of notch-filter with resonance frequency at 2ω in voltage-loop in the dual-loop mode control scheme provides enough separation between voltage-loop and current loop and hence the 2ω-ripple reduces at the input of the system. This scheme improves the dynamic performance of the system, however, this limits the bandwidth of the system for a wide-range frequency operation due to the addition of negative phase-shift by the notch-filter for the frequencies below the resonance frequency. A poor-design of the resonant filter may induce instability. In case of voltage mode control scheme, an addition of band-pass filter with the resonance frequency at 2ω is used to increase the output-impedance of the front-end converter to achieve the mitigation of 2ω-ripple. A good dynamic performance of the system is achieved with this scheme, however, a phase rotation of π rad/s by the band-pass-filter limits the voltage-bandwidth of the system.

The nonlinear control approaches are generally preferred in the system with the large line-load disturbances such as renewable energy sources based power systems. Furthermore, the renewable energy sources are sensitive to low-frequency ripple. This ripple may cause the fuel-starvation and heating in the fuel-cell and improper MPPT operation of the solar PV and fuel-cell systems. Therefore, the non-linear control approaches are suitable in such applications. The non-linear control approaches perform well at the large line-load transients in comparison to the linear

controllers. The nonlinear controls such as SMC and ISMC add high degree of robustness against the matched uncertainty. Nevertheless, in the literature, a few nonlinear control techniques are proposed for the mitigation of the SHC ripple problem. The added features of the robustness and the stable wide range of operation at the large line-load transients over the linear controls, the nonlinear control approaches are to be explored thoroughly in the context of the mitigation of $2\omega-$ripple problem in the single-phase inverter.

Z-source inverters and quasi-Z source inverters are the emerging competitive technologies for the medium/high power applications. Similarly, the switched-mode boost inverters and quasi-switched boost inverters are emerging technology in the low-power applications especially for the microinverter applications. Unlike the two-stage converters, these all topologies constitute a single-stage units and have the capability of shoot-through operation. The reduction in the size of components of front-end networks of such converters, for instance, Z source or quasi-Z source network in the presence of 2ω-ripple is a challenge. Nonetheless, quasi-ZSI and quasi-SBI have inbuilt front-end control capability, and therefore ripple mitigation at the input can be achieved through the suitable control only without adding additional active filter.

To summarize, the reliability of E-cap, control and compact design of active filter, stability, dynamic performance and robustness of system against the uncertain characteristics of the RE/alternative energy sources based systems are open challenges. A flowchart, shown in the Fig. 2.26, is proposed here to conclude the literature reviewed in this Chapter.

In the next Chapter, a new adaptive sliding mode control is presented to mitigate the second-order harmonic ripple at the input of two-stage DC-DC-AC converter. The proposed control scheme is based on the output-impedance shaping. Besides the ripple mitigation at the input, the proposed controller ensures better dynamic performance at the large line-load transients in comparison to the existing linear control.

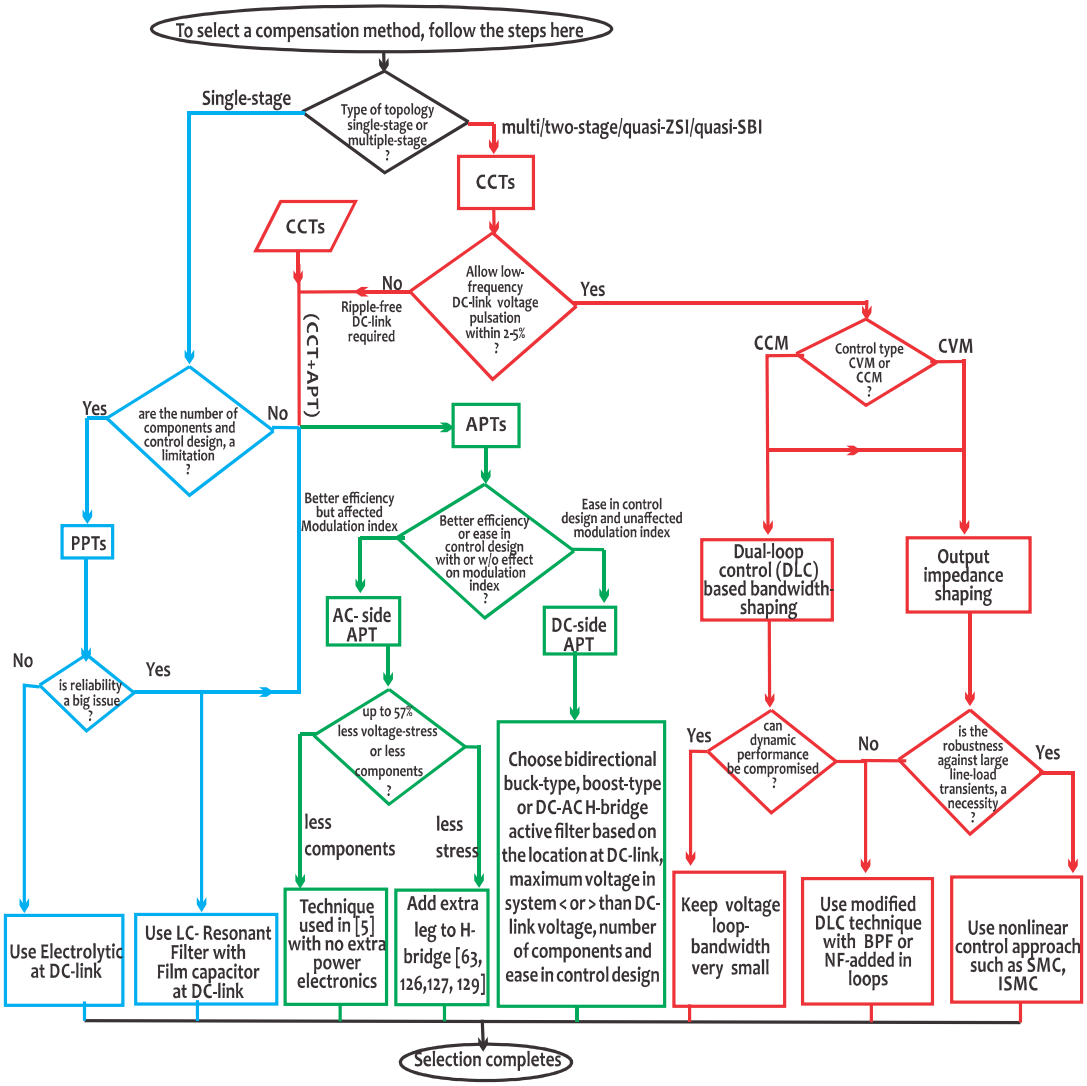

Figure 2.26 : Algorithm for the selection of suitable $2\omega-$ripple compensation technique in a broader sense

Table 2.4 : Summery of Passive and Active Techniques

Figure and Ref.	Technique	Extra Components	Scheme or tool	Merits	Challenges
Fig. 2.11(a) [Serban, 2015]	APT (AC-side)	2-C	Passive components	No extra switches addition	Efficiency affected, utilization factor of storage elements$<50\%$
Fig. 2.8(f) [Krein *et al.*, 2012]	APT (DC-side)	4-S,1-L,1-C	Ripple-port Circuit	Better system life	More switches
Fig. 2.8(d) [Wang *et al.*, 2011]	APT (DC-side)	2-S, 1-L, 1-C	Buck-type filter (bidirectional)	No voltages $> V_{DC-link}$ in the system	DCM operation causes high current stress
Fig. 2.6 [Rodriguez *et al.*, 2002] [Liserre *et al.*, 2006] [Wenyi and Chen, 2009] [Rahim and Selvaraj, 2010] [Araujo *et al.*, 2010] [Nguyen and Choi, 2018]	PPT	A large size E-cap	E-cap	Simple and conventional technique	Reliability issue, high, ESR value low-ripple handling capacity
Fig. 2.6(f) [Fukushima *et al.*, 2009] [Jang *et al.*, 2007]	PPT	1-L,1-C	Inductive filter	Easy and smaller	Large size inductor
Fig. 2.11(g) [Iyer and John, 2015]	APT (DC-side)	6-S, 2-C, 1-L, 1-Txr	Hybrid filter	Small size buffer	More components capacitor and lossy
Fig. 2.12 [Ge *et al.*, 2016b]	APT (AC-side)	2-S, 1-C, 1-L	Integrated filter	Small capacitors in qZSI	One extra leg
Fig. 2.6(k) [Makovenko *et al.*, 2017]	PPT		LC-resonant filter	Cost-effective with LC	resonance problem, tedious L-C design
Fig. 2.8(b) [Cai *et al.*, 2014]	APT (DC-side)	2-S, 1-C, 1-L	ALFRCD	Small filter size	Possibility of short-circuiting for $v_{FC} < v_{DC-link}$
Fig. 2.11(f) [Kyritsis *et al.*, 2007]	APT (AC-type)	2-S, 2-C, 1-L 1-Txr, 1-Rcr	CPS-PAF Buck/ Boost type	Possible problem of short-circuiting solved	LFT and a rectifier required,Bulky and complex system

Table 2.5 : Summery of Passive and Active Techniques (Continued...)

Figure and Ref.	Technique	Extra Components	Scheme or tool	Merits	Challenges
Fig. 2.8(e) [Christidis *et al.*, 2016]	APT (DC-side)	4-S, 1-L, 1-C	FB-RCR	LFT and rectifier are not required	4-switches are required
Fig. 2.10(b) [Liu *et al.*, 2017]	APT (DC-side)	2-S, 1-C, 1-L	Buck-boost type filter for qZSI	Smaller size of Z-source network	Challenging control design compared to H-bridge
Fig. 2.10(c) [Liang *et al.*, 2018]	APT (DC-side)	Battery	quasi-ZS network with battery	Detailed design of asymmetric quasi-ZS network is available	Only a part of $2\omega-$ripple can be reduced
Fig. 2.11(b) [r. Zhu *et al.*, 2016]	APT (AC-side)	2-S	Ripple-confinement	100% utilization of storage elements	One extra leg besides H-bridge, more voltage stress on switches
Fig. 2.11(c) [Chen *et al.*, 2015]	APT (AC-side)	2-S, 1-C, 1-L,	SVPWM Based 2-E-cap	Current and voltage stress is less for a range of power-factor	One extra leg besides H-bridge, total power rating increase by 50%
Fig. 2.11(d) [Bhowmick and Umanand, 2018]	APT (AC-side)	2-S, 1-C, 2-L	Active filter	Stress on switches reduces by 70% for all power factor $(p.f.)$	One extra leg besides H-bridge
Fig. 2.11(e) [Morsy and Enjeti, 2016]	APT (AC-side)	2-S, 1-C, 1-L	Active filter	Switch-stress reduces by 70% for all $p.f.$	High cost of GaN switches
S=Switch	C=capacitor	L=inductor	Txr=Transformer	Rcr=Rectifier	

Table 2.6 : Summery of Control-oriented Compensation Techniques in DC-AC Converters with Front-end Converter or Control Circuits

Fig. and Ref.	Topology	Scheme or tool	Basic concept	Remarks
Fig. 2.17(c) [ZhengWei *et al.*, 2012]	Two-stage; stand-alone; Push-pull forward type DC-DC-AC converter	NF-added; voltage-loop(CMC)	NF attenuates 2ω-ripple in reference current of current-loop	NF adds negative phase for frequencies$< \omega_o$ may cause instability
Fig. 2.17(d) [Khajehoddin *et al.*, 2013]	Two-stage;Grid-connected; isolated-phase-shift DC-DC-AC converter	NF-added voltage-loop, grid-side bus voltage control	Similar to [ZhengWei *et al.*, 2012]	Same as in [ZhengWei *et al.*, 2012] complex control design
Fig. 2.19(d-f) [Zhang *et al.*, 2015]	Two-stage; buck-derived DC-DC-AC converter	BPF-CVFS (CVM)	2ω variation in reference bus voltage	Same as in [Zhang *et al.*, 2014]
Fig. 2.14(a) [Kwon *et al.*, 2009]	Two-stage;Grid-connected Current-fed resonant push-pull DC-DC-AC converter	Feed-forward control	Feed-forward generates ripple cancellation duty	Easy to implement, poor disturbance-rejection, lacks robustness
Fig. 2.18(e) [Zhu *et al.*, 2015]	Two-stage; stand-alone Buck-derived DC-DC-AC converter	NF-LCFFS (CMC)	NF in load current feed-forward path decreases Z_o everywhere except at 2ω	NF adds negative phase for frequencies$< \omega_o$
Fig. 2.18(e) [Zhu *et al.*, 2015]	Two-stage; stand-alone; buck-derived DC-DC-AC converter	NF-CR-LCFFS (CMC)	NF-CR-LCFFS decreases Z_o everywhere except at 2ω	NF adds negative phase shift, limited bandwidth
Fig. 2.23(a) [Ahmad *et al.*, 2012]	Stand-alone;Boost-derived DC-DC-AC converter	PI+Non-linear compensator	Output-impedance shaping	Instability problem due to high controller gain
Fig. 2.21(b) [Liu *et al.*, 2018]	Residential PV and Battery system	Double channel current feedback control, ToGI	Ripple-free duty control based	Trade-off b/w ripple-reduction and stability
Fig. 2.21(c) [Shi *et al.*, 2018]	Boost;buck-boost derived power converters	MAF or multi-resonant filter	Notching effect at multiple of 2ω	Attenuates 2ω-ripple and its multiple; a negative phase-shift occurs due to NF
Fig. 2.14(b) [Jung *et al.*, 2011]	Two-stage; Grid-connected Boost-derived converter	quasi-NF-added voltage-loop (grid-side control)	Notch-filter substantially reduces voltage-loop BW	quasi-NF adds negative phase for frequencies$< \omega_o$
Fig. 2.14(b) [Jung *et al.*, 2011]	Two-stage; Grid-connected Boost-derived DC-DC-AC converter	Independent current loop & voltage-loop	No interaction between loops	Theoretically; a large reduction in 2ω-ripple; difficult implementation

Table 2.7 : Summery of Control-oriented Compensation Techniques in DC-AC Converters with Front-end Converter or Control Circuits (Continued...)

Fig. and Ref.	Topology	Scheme or tool	Basic concept	Remarks
Fig. 2.14(c) [Liu and Lai, 2007a]	Two-stage; stand-alone; DC-DC-AC converter	Dual-loop control(CMC)	Kept a very low bandwidth (BW) of voltage-loop	Trade-off b/w ripple-reduction and dynamic performance
Fig. 2.20(a-b) [Wang *et al.*, 2014b]	Half-active bridge DC-DC-AC converter	Back-current gain based control	Very small back-current gain at 2ω or minimum approach	NF adds negative phase; BPF causes π *rad* phase rotation; limited BW
Fig. 2.19(c) [Bojoi *et al.*, 2010]	Current-fed push-pull based DC-DC-AC converter	Similar to (CMC) [Shi *et al.*, 2016b]	2ω-variation in reference bus voltage to generate ripple-free current reference	Bandwidth limitation
Fig. 2.18(a) [Zhang *et al.*, 2014]	Two-stage; Buck-stand-alone derived DC-DC-AC converter	VRS	A virtual resistance increases Z_o	poor dynamic performance
Fig. 2.18(c) [Zhang *et al.*, 2014]	Two-stage;stand-alone Buck-derived DC-DC-AC converter	NF-CR; (CVM)	BPF in current feedback path increases Z_o at 2ω	a phase rotation of π *rad* caused by BPF limits voltage-loop bandwidth
Fig. 2.19(a-b) [Shi *et al.*, 2016b]	Two-stage; stand-alone Buck-derived DC-DC-AC converter	LCFFS (VMC)	Pulsation in DC-link voltage forces the ripple to follow capacitor branch	DC-link pulsates at 2ω; performance depends on system parameter's accuracy
[Liu *et al.*, 2014]	CF-DHB DC-DC-AC converter	Phase-shift control; PR controller	PR modifies the main phase-shift control	PR limits the BW; sluggish dynamics
[Xue *et al.*, 2015]	Dual-active bridge based GaN and Si-charger	Low-pass filter based control	sinusoidal charging forces ripple injection into battery	battery life may be affected
[Galvez and Ordonez, 2015]	Stand-alone; fuel-cell based DC-DC-AC converter	NSS	four quadrant control	may suffer chattering problem
Fig. 2.23(b) [Gautam *et al.*, 2018]	Stand-alone;Boost-derived DC-DC-AC converter	adaptive-SMC	Output-impedance shaping	Ripple-reduction affected during transients