# 3
# Biocompatible and Natural Polymers as Gate Dielectrics

Biocompatible and natural polymers are utilized as promising gate dielectric candidate for the fabrication of high-performance OFETs, employing their inherent properties of flexibility and compatibility with both organic semiconductors and plastic substrates. Moreover, these materials can be easily processed with energy-efficient solution-processed methods at low temperatures. The use of biocompatible and natural polymers as gate dielectrics in device fabrication represents a significant advancement in the development of sustainable, eco-friendly electronics. Apart from these advantages, polymer dielectrics exhibit multiple disadvantages such as leakage current issues and unstable electrical characteristics under different electrical and environmental conditions. This issue can be addressed by using different dielectric strategies such as crosslinking of polymers, formation of bilayer polymer dielectrics, and integrating thin inorganic high-*k* dielectric layer along with pristine polymers, suppressing the leakage current and facilitating low-voltage operation in devices. In this chapter, various polymers such as polyvinylpyrrolidone (PVPy), a synthetic biocompatible polymer along with natural polymers such as egg albumen, silk fibroin, chitosan, gelatin, and cellulose derivatives, are being explored either as single layer or as bilayers with other polymers and inorganic $HfO_2$ dielectric. Neat TIPS-Pentacene and a blend of polystyrene (PS) and TIPS-Pentacene are used to form the active layer. All these devices exhibited good p-channel transistor characteristics either on glass or flexible substrates, confirming their suitability as gate dielectrics in OFETs.

## 3.1 INTRODUCTION

Utilization of biocompatible and nature-originated materials in device fabrication is important to enhance the biodegradability (W. Li et al., 2020), eventually helping towards the reduction of E-waste, which has become a serious concern for environment and health in recent times (Hsu et al., 2019). The properties of materials and fabrication processes are vital factors in deciding the performance of any device (Wu et al., 2021). Though organic semiconductors are the primary functional layer in OFET devices, gate dielectric plays a crucial role in achieving high performance in OFETs with additional functionalities (Sirringhaus et al., 2010). The conducting channel in OFETs exists in the first few monolayers of the semiconductor in the vicinity of the surface of the gate dielectric, therefore surface properties including morphology, dipole disorder, and trapping sites play a crucial role in charge transportation (Y. Wang et al., 2019). Moreover, high gate capacitance density ($C_i$) is essential in achieving low voltage operation in OFETs (Haase et al., 2019; Konwar, Saxena, Rahi, et al., 2022). Numerous synthetic and biocompatible polymers are being investigated as gate dielectrics in OFETs, providing secure interaction with biological tissues and making them ideal for applications in bioelectronics, wearable devices, and implantable systems (M. Irimia-Vladu et al., 2010). Among many biocompatible synthetic polymers, polyvinylpyrrolidone (PVPy) is one of the easily dissolvable and human-friendly polymers, that offers non-toxicity, water solubility, thermal stability, cross-linkability due to the presence of carbon-oxygen double bond, and good environmental stability, ensuring its suitability as a gate dielectric in transistors (J. Li et al., 2020). In addition, PVPy is extensively employed as additives in medicinal and personal care items, alongside as a reducing agent and surface stabilizer in the synthesis of nanoparticles (Hosseini et al., 2023; Kurakula & Rao, 2020). However, PVPy lacks biodegradation due to its synthetic polymer backbone, making it unsuitable

for fully sustainable or "green" electronics where biodegradability is an important consideration. Although this synthetic polymer provides excellent biocompatibility and flexibility, the natural polymers are considered as suitable eco-friendly candidate due to their enhanced eco-friendliness, inherent biodegradability, and lower environmental footprint compared to petroleum-based synthetic materials.

### 3.1.1 Natural Polymers

Natural polymers are crucial material components for biodegradable electronics, derived from various renewable resources like plants, animals, bacteria, and algae (Pradhan et al., 2020). These materials have remarkable characteristics, including strong mechanical stress capabilities, exceptional biocompatibility, and faster degradability in comparison to conventional synthetic polymers (Jia et al., 2021). Moreover, the chemical structure of polymer dielectrics can be easily modified with the help of molecular design and chemical synthesis due to the presence of an abundant number of functional groups to add novel functionalities and applications to these polymers. These polymers have made significant contributions in diverse areas, including in food industry, tissue engineering, regenerative medicine, sensors, and more. Many natural polymers provide good insulating properties which make them suitable dielectric candidates in various devices like transistors, capacitors, resistors, etc. Various plant or animal-based natural polymers such as silk fibroin, egg-albumen, gelatin, chitosan, and cellulose are introduced as a gate dielectric for the fabrication of eco-friendly and biodegradable OFETs (Cao & Uhrich, 2018; W. Li et al., 2020). Figure 3.1 shows the chemical structure of different natural polymers.

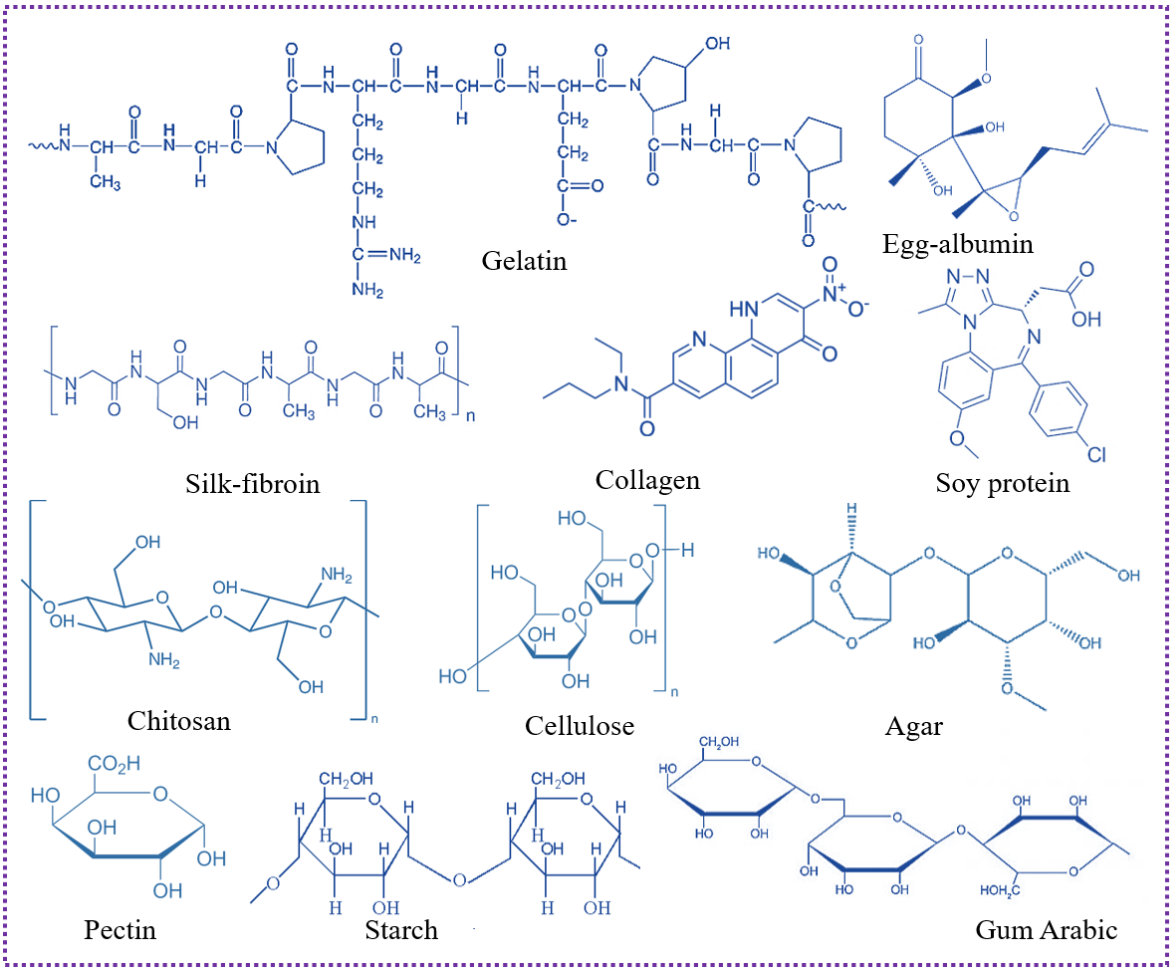



**Figure 3.1 :** Chemical structures of various proteins and polysaccharides used as gate dielectrics in eco-friendly OFETs.

Furthermore, the presence of functional groups enables these natural dielectrics to function as solid-state electrolytes, facilitating the formation of an electrical double layer (EDL) when subjected to a gate electric field (Cunha et al., 2017; Lee et al., 2018a; Luo et al., 2019; M. Singh et al., 2017). This characteristic is advantageous for achieving low operating voltage in devices like transistors. The key functional group carboxyl (-COOH) is mainly present in gelatin polymer which releases protons ($H^+$) and forms negatively charged carboxylate ions ($-COO^-$) under an electric field or in the presence of water. The amino ($-NH_2$) group is primarily found in the amino acids chain of gelatin and chitosan, and positively charged ammonium ions ($-NH_3^+$) are formed due to accepting protons in slightly acidic conditions. Another key functional group hydroxyl (-OH) is found abundantly in different natural polymers like cellulose, chitosan, silk-fibroin, and gelatin, which forms hydrogen bonds with water molecules and supports the dissociation of other functional groups. These functional groups further dissociated into mobile ions under different circumstances like interaction with water molecules or doping with ionic liquids and applying an external electric field to assist the ionic conductivity (J. Li et al., 2021).

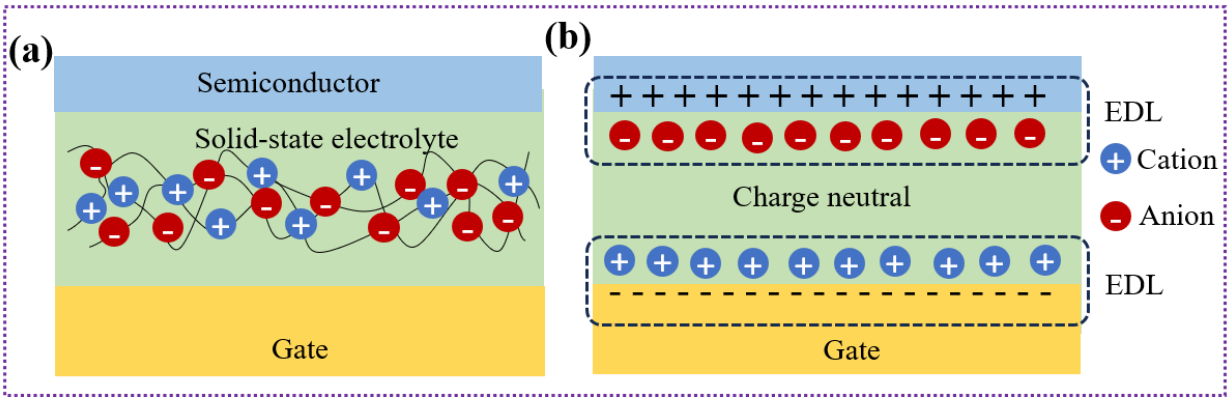



**Figure 3.2 :** Mechanism of solid-state electrolyte gate dielectric in OFETs. (a) Charge distribution and presence of mobile ions with polymer matrix in electrolyte without applying any gate bias. (b) Charge distribution in semiconductor and electrodes for applying negative gate bias with the formation of EDL.

Figure 3.2 illustrates the mechanism of solid-state electrolyte gate dielectric in OFETs considering a p-type semiconductor. Upon application of negative gate voltage, cations move to the gate electrode and dielectric interface, whereas the anions migrate towards the dielectric: semiconductor interface (Xie & Frisbie, 2013). Therefore, to balance the ionic charge holes are accumulated in the semiconductor near the dielectric interface. The combination of ionic charges along with their counter charges, results in the formation of EDL at both interfaces. The gate potential is primarily declined into the EDLs only, resulting in a charge neutralized and field-free bulk of the electrolyte layer. EDL is known as nanometre thick capacitors with a very small effective distance of around 1 nm between ion and charges, resulting in high capacitance density, enabling to operation of the devices at low voltage while generating very high charge carrier density for a small applying voltage (Duan et al., 2020). Table 3.1 summarizes the performance of transistors with different natural polymers as gate dielectrics. The presented table mainly provides a comprehensive overview of the various natural polymers that have been explored as gate dielectrics over a decade along with their performance parameters, rather than highlighting a direct comparison among them.

**Table 3.1 :** A comprehensive overview of performance parameters of transistors using various natural polymers as gate dielectrics.

| Substrate | Dielectric | OSC | Op.V (V) | $V_{TH}$ (V) | μ ($cm^2/Vs$) | $I_{on}/I_{off}$ | Ref. |
|---|---|---|---|---|---|---|---|
| ITO-glass | Silk fibroin | P3HT | -3 | -0.77 | 0.21 | - | (Shi et al., 2014) |
| $Si/SiO_2$ | Alginate | pBTTT-C14 | -0.5 | -0.02 | 0.014 | 438 | (Dumitru et al., 2015) |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Paper | Cellulose | IGZO | <2 | - | 21 | ~$10^6$ | (Cunha et al., 2017) |
| ITO-glass | Starch | ITO | 1.5 | 0.2 | 14.9 | ~$10^7$ | (Guo et al., 2018) |
| ITO-PET | Triacetate cellulose | pBTTT | -50 | -0.12 | 0.031 | ~$10^3$ | (Bae et al., 2017) |
| ITO-glass | Natural rubber/PVPy | PTCDI-C8 | 20 | 0.83 | 0.027 | ~$10^3$ | (Rullyani, Ramesh, et al., 2018) |
| Cellulose Nanopaper | ICCN | C8-BTBT | -5 | -1.26 | 0.072 | ~$10^4$ | (Dai et al., 2018) |
| Paper | Gelatin/FeG | Pentacene | -5 | -1.4 | 8.0 | ~$10^3$ | (C. J. Lee et al., 2019) |
| Glass | Pea protein | IZO | 2 | 0.1 | 27.6 | 3×$10^6$ | (Luo et al., 2019) |
| Glass | Almond Gum | DPPTTT/PMMA | -3 | -0.80 | 0.75 | ~$10^3$ | (Seck, Mohammadian, Diallo, Faraji, Erouel, et al., 2020) |
| ITO-glass | Collagen-CTMA | Pentacene | -60 | -16.4 | 0.067 | ~$10^7$ | (Benas et al., 2020) |
| Glass | Gum arabic | DPPTTT/PMMA | -3 | -0.35 | 0.6 | >$10^2$ | (Seck, Mohammadian, Diallo, Faraji, Saadi, et al., 2020) |
| Glass | Egg-albumen | Pentacene | -1.5 | -0.9 | 0.55 | ~$10^3$ | (Mandal et al., 2021) |
| ITO-PET | Pectin | ITO | 1 | 0.02 | 14.5 | ~$10^7$ | (Liu et al., 2022) |
| Si | C-dextran | C8-BTBT | -30 | -10.43 | 7.72 | ~$10^5$ | (Yang et al., 2022) |
| Glass | Khaya Gum | DPPTTT/PMMA | -3 | -1.3 | 0.30 | ~$10^3$ | (Tall et al., 2022) |
| Ethyl cellulose | Chitosan | P3HT | -1 | -0.13 | - | ~$10^4$ | (Sharova et al., 2023) |
| Paper | Shellac | P(DPP-TVT) | -80 | 7.64 | 0.93 | ~$10^3$ | (Skaf et al., 2024) |
| Glass | Xanthan Gum | PBTTT-C14 | -1 | -0.2 | 0.017 | 56.50 | (Mandal et al., 2025) |

The dielectric properties of these materials have already been investigated in various oxide thin-film transistors (TFTs) and OFETs with thermally evaporated organic semiconductors. Transistors fabricated with oxide-based semiconductors exhibited low voltage operation in comparison to transistors with organic semiconductors (Cunha et al., 2017; Guo et al., 2018; Luo et al., 2019). In some cases, devices with thermally evaporated organic semiconductors also exhibit high performance either on rigid substrates or by integrating with other nanocomposites (C. J. Lee et al., 2019; Tall et al., 2022). However, high-performance OFETs with solution-processed organic semiconductors on flexible substrates are scarce in the literature. Even though these natural polymers offer various advantages as gate dielectrics, the high leakage current density and surface roughness of a few of these dielectric layers are not suitable for fabrication of transistor devices in general (S. J. Kim et al., 2015). To address these issues, in some cases, a thin polymer dielectric layer is coated over another polymer dielectrics to form the bilayer of natural polymers to facilitate better semiconductor film deposition over it, low leakage current density,

and high capacitance coupling for achieving high performance in devices. Moreover, the hygroscopic nature of these materials provides the ability to be used in a wide humidity range without degrading their film qualities. In addition, polymer gate dielectrics are integrated with high-*k* dielectrics such as $HfO_2$ (*k*~20-25), which is a very common way for the demonstration of high-performance devices. The hybrid bilayer gate dielectric helps to achieve low voltage operation as well as gate leakage reduction in organic devices (Held et al., 2015; Ortiz et al., 2010).

In the literature, most transistors incorporating natural polymers have been demonstrated on rigid glass substrates. Only a few studies have explored flexible or paper substrates operating at low voltages; however, these often used thermally deposited inorganic materials as the active layer. Furthermore, comprehensive assessments of electrical performance, mechanical flexibility, and environmental stability have generally been lacking in such reports. In this chapter, emphasis is placed on the use of solution-processed dielectric including PVPy, silk-fibroin, egg-albumen, chitosan, gelatin, and a cellulose derivative, along with solution-processed active layers to achieve cost-effective fabrication, enhanced transistor performance, and thorough evaluation of electrical, mechanical, and operational stability.

## 3.2 OFETs with PVPy Gate Dielectric

PVPy is a promising biocompatible synthetic polymer that is easily dissolvable in various organic solvents like ethanol, IPA, and deionized (DI) water, etc. (Pradhan et al., 2020). PVPy exhibits an acceptable dielectric constant (about 4-5), ensuring adequate gate capacitance for efficient charge modulation at low operating voltages. The excellent film-forming capability facilitates the production of homogenous and smooth thin films, essential for reducing charge trapping and enhancing interface quality with organic semiconductors. Additionally, PVPy is chemically tunable and can be cross-linked with other agents to increase its chemical and thermal stability. In earlier reports, PVPy and its composites with inorganic/organic materials have been explored as gate dielectric for organic transistors (S. Li et al., 2021; Rullyani, Ramesh, et al., 2018; Rullyani, Sung, et al., 2018; W. Zhang et al., 2020). However, most of these reported PVPy-based transistors utilized thermally evaporated semiconductors and were operated at high voltages (Rullyani, Ramesh, et al., 2018; Rullyani, Sung, et al., 2018; W. Zhang et al., 2020). Moreover, reports on OFETs with a single layer of PVPy dielectric and solution-processed organic semiconductors are difficult to find. Here, PVPy was explored as a gate dielectric in solution-processed OFETs for low-voltage operation. The blend of TIPS-Pentacene: PS was used to form the active layer in these devices. The fabricated devices exhibited -5 V operation with good p-channel characteristics, excellent repeatability, and bias-stress stability, confirming their suitability in practical applications. Moreover, environmental stability was also observed for up to 3 months. This work is published in conference proceedings (G. Konwar, S. Bhattacharjee, et al., 2023).

### 3.2.1 Device Fabrication

ITO-coated glass was used as a substrate to fabricate bottom gate top contact (BGTC) OFET devices. A 5 wt. % solution of PVPy (average molecular wt. of 40,000) in ethanol was prepared by stirring for 1 h at 60 °C. This solution was spin-coated at 1500 rpm and then annealed at 100 °C for 30 minutes for the formation of smooth gate dielectric layer. Thickness of ~0.65 μm was obtained for PVPy layer, measured using the Dektak XT surface profiler. For the active layer, separate 0.5 wt % solutions of TIPS-pentacene (≥99 % HPLC, Sigma Aldrich) and PS (average Mw ~280,000, Sigma Aldrich) were prepared in toluene by stirring at a temperature of 65 °C for 2.5 hours, and were mixed in equal volume (1:1) followed by again stirring for another 1 h at 65 °C to prepare the blend solution. The prepared blend solution was drop cast onto the dielectric layer. The thickness of the TIPS-Pentacene: PS polymer blend was ~1.2 μm, where the thickness of TIPS-Pentacene depends on the phase separation which is explained elsewhere (Bharti et al., 2016). Finally, gold (Au) top source/drain contacts were deposited through a metal shadow mask.

Figure 3.3 (a) shows the cross-sectional schematic of the device. The chemical structure of PVPy is shown in Figure 3.3 (b). A digital image of a fabricated array of transistors is shown in

Figure 3.3 (c). Fabricated devices were characterized in lab ambient using a Keithley 4200-SCS semiconductor parametric analyzer. Device parameters were extracted using the $I_{DS}$ equation of conventional transistors, for saturation region. $V_{TH}$ was measured directly from the maximum slope of the transfer plot of $(I_{DS})^{1/2}$ vs $V_{GS}$. To measure $C_i$, metal-insulator-semiconductor-metal (MISM) structure ITO/PVPy/TIPS-Pentacene: PS/Au was characterized for capacitance vs. frequency (*C-f*) characteristics using the LCR meter, for a frequency range of 40 Hz to 2 kHz, and ~14 nF/cm$^2$ was obtained at 40 Hz frequency.

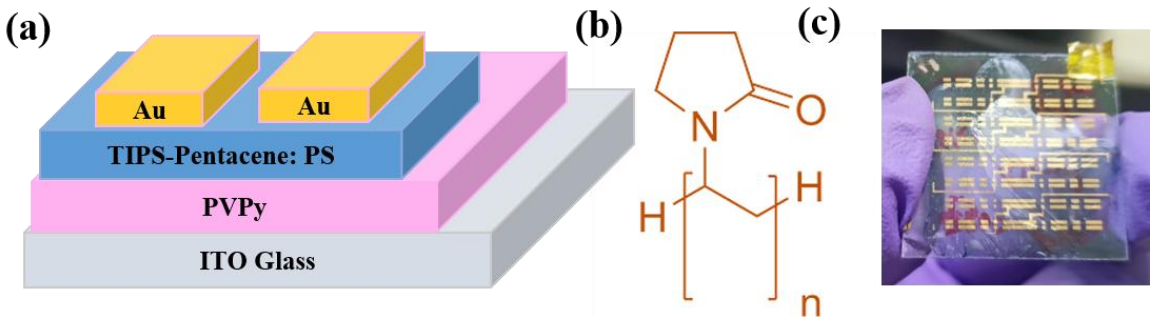



**Figure 3.3 :** (a) Schematic of the device structure, (b) chemical structure of PVPy, (c) digital picture of a substrate with fabricated devices.

### 3.2.2 Transistor Performance

Highly saturated output characteristics along with good transfer characteristics are observed in Figure 3.4 (a) & (b), respectively. $C_i$ derived from MISM structure was used for the extraction of $\mu_{sat}$ and $D_{it}$ values. Devices exhibited good p-channel characteristics with a maximum $\mu_{sat}$ of 0.3 cm$^2$ V$^{-1}$s$^{-1}$ with an average of 0.2 (± 0.1) cm$^2$ V$^{-1}$s$^{-1}$. A very low $V_{TH}$ of -0.20 V suitable for low voltage operation was obtained with *SS* of 0.68 V/dec., and a good on/off current ratio of $10^3$ was achieved. $D_{it}$ value of 9.13 (± 1.22) × $10^{11}$ cm$^{-2}$ eV$^{-1}$ was exhibited, confirming good dielectric: semiconductor interface.

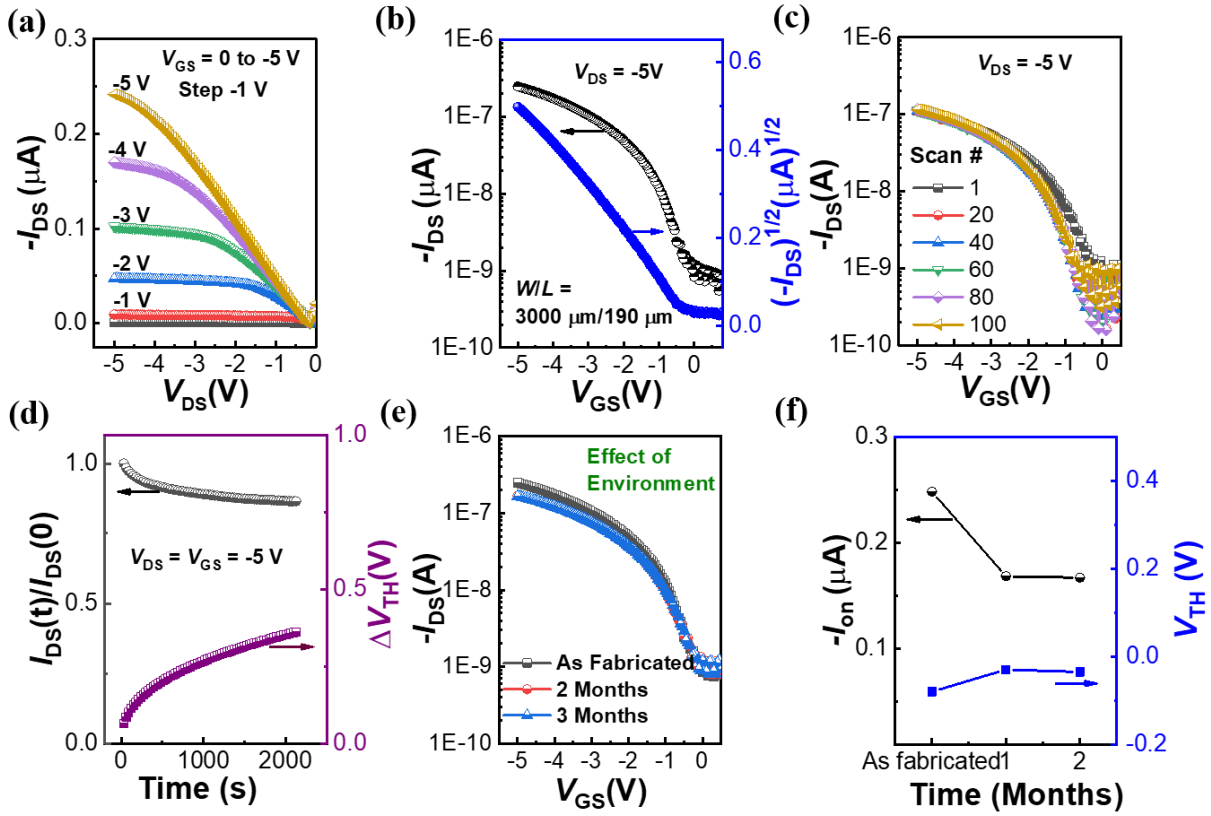



**Figure 3.4 :** Output (a), and transfer (b) characteristics of a typical fabricated device. (c) Repeatability of transfer curves, and (d) bias-stress stability. (e) Effect of environment on a particular device, and (f) variation in $I_{on}$ & $V_{TH}$ at different time intervals up to 3 months.

Further, excellent repeatability was demonstrated through the repeated scans of transfer characteristics for 100 continuous cycles as shown in 3.4 (c). The normalized drain current ($I_{DS}$ (t)/ $I_{DS}$ (0)) with time upon application of a constant bias-stress at $V_{GS}$ = $V_{DS}$ = - 5 V for 30 minutes, is shown in Figure 3.4 (d), showing a decay of less than 15% in the current. This figure also shows the shift in $V_{TH}$ ($\Delta V_{TH}$) over the stress period on right Y-axis which was extracted by using earlier reported formula (Tiwari et al., 2009). A typical shift of about 0.35 V was exhibited as shown in the plot, indicating high stability upon bias-stress. Such variation due to bias-stress is common due to the trapping of carriers at the dielectric: semiconductor interfaces (Bisoyi et al., 2014).

**Table 3.2 :** Summary of the performance parameters of PVPy dielectric based transistors

| $C_i$ (nF. cm$^{-2}$) | Op. V (V) | $k_{p,\,max}$ (nF. V$^{-1}$ s$^{-1}$) | $\mu_{max}$ (cm$^2$ V$^{-1}$ s$^{-1}$) | $\mu_{avg}$ (cm$^2$ V$^{-1}$ s$^{-1}$) | $V_{TH}$ (V) | SS (V/dec) | $D_{it}$ (cm$^{-1}$ eV$^{-1}$) | $I_{on}$/ $I_{off}$ |
|---|---|---|---|---|---|---|---|---|
| 14 | -5 | 10.0 | 4.2 | 0.20 | -0.2 | 0.68 | $9.13\times10^{11}$ | $10^3$ |

$C_i$ extracted at 40 Hz.

In addition, the effect of environment on a particular device was studied to investigate the operational reliability of fabricated devices in real applications. The device was kept under a lab environment for 3 months and characterized the transfer curve at different time intervals. The environment conditions were fairly similar with temperatures around 30 ± 5 °C, and relative humidity up to 60 % in the three months' duration for which the devices were investigated for this study. The changes in humidity and temperature of the lab environment affect the transistor characteristics that can be seen from the transfer plot in Figure 3.4 (e). Good environmental stability is attributed due to the hydrophobic property of PS binder, which effectively resists the degradations of dielectric/semiconductor interface. The corresponding changes in $I_{on}$ and $V_{TH}$ are shown in Figure 3.4 (f). As can be seen, a high environmental stability was observed for up to 3 months. ~ 30 % reduction in $I_{on}$ and the value of $V_{TH}$ was shifted towards the positive side from -0.08 to -0.035 after being kept the devices in lab ambient for 3 months. The effect of humidity on organic materials is very common (Mandal et al., 2020a). However, the possible reason for exhibiting this stability is the presence of hydrophobic nature of PS binder, resisting the degradation in transistor performance (Bharti et al., 2016). These results imply that PVPy can be among suitable options for biocompatible gate dielectric in OFETs. Though PVPy has exhibited good dielectric properties, this work was not further investigated in this thesis due to its non-biodegradability property as this dissertation primarily focuses on minimizing the production of E-waste.

## 3.3 OFETs with Silk-fibroin Gate Dielectric

Silk fibroin (SF) is an animal-originated natural protein extracted from bombyx- mori silk cocoons and contains amino acids with a repetitive sequence of glycine (gly) and alanine (ala) (Zhu et al., 2016). The SF thin film is considered to be one of the promising gate dielectric materials due to its easy processability, high flexibility, biocompatibility, water solubility, and excellent resistance to organic solvents (Tao et al., 2014; Wang et al., 2011). Low voltage OFETs were reported in the literature with pristine SF layer using Pentacene and poly(3-hexylthiophene) as an active layer, however, their flexibility and electrical stability were not investigated (Shi et al., 2014; Wang et al., 2011). OFETs with bare SF experienced several limitations including high leakage current and instability in the environment (Li et al., 2014). A water-soluble polymer PVA was crosslinked with SF to improve the stability in devices by reducing the trap density of dielectric (Zhuang et al., 2016). Nevertheless, these devices were operated at a high voltage of -40 V. The incorporation of a thin high-k inorganic dielectric layer with polymer dielectrics can reduce the leakage current issue, which simultaneously facilitates low-voltage operation in OFETs (Held et al., 2015). In this work, SF was extracted from silkworm cocoons by a solution-processed method and used as a gate dielectric. However, the single layer of SF lacks electrical stability for repeated cycles. Hence, a thin $HfO_2$ inorganic layer was combined with an SF layer for the

demonstration of high-performance flexible OFETs. A widely explored air-stable TIPS-Pentacene was used as an active layer for excellent p-channel characteristics.

### 3.3.1 Experimentation

To extract SF, silk cocoons were collected from the local area of Assam, India. Figure 3.5 illustrates the various steps to extract SF from silkworm cocoons in our laboratory. Initially, cocoons were cut into small pieces and degummed by boiling in 0.5 M of $Na_2CO_3$ solution for 30 minutes. Further, it was rinsed in deionized water (DI) multiple times to remove the glue-like sericin protein and dried at room temperature for overnight. The dried silk fibermesh was dissolved in 9.3 M of LiBr solution at 60 °C for 4 hours. Further, the fibroin solution was dialyzed using a cellulose membrane-based dialysis cassette against DI water for a duration of 48 hours to remove the LiBr from the solution. SF solution was then centrifuged twice at 4000 rpm for 30 minutes and finally, the upper part of the solution was taken out and stored at 4 °C for subsequent process.

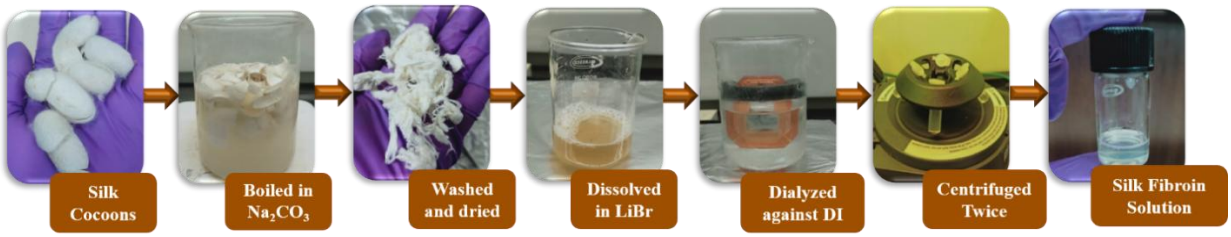



**Figure 3.5 :** Illustration of various steps of extracting SF aqueous-based solution from silkworm cocoons in our laboratory.

Devices with BGTC structure were fabricated on flexible ITO-coated PET substrate. A 40 nm thick $HfO_2$ layer was deposited on top of the substrate by ALD. SF solution was spin-coated at 2000 rpm for 30 s on top of the $HfO_2$ layer and the resulting film underwent annealing at 60 °C for 30 minutes to eliminate any residual solvent. TIPS-Pentacene solution was drop cast to form an active layer, using the same process explained in an earlier report (G. Konwar, S. Bhattacharjee, et al., 2023). Finally, thermally evaporated top Au contacts were deposited through a metal shadow mask.

### 3.3.2 Transistor Performance

The device schematic with BGTC structure is shown in Figure 3.6 (a). The $C_i$ value was measured through ITO/$HfO_2$/SF/Au structure and found to be 8.5 nF/cm² at 1 kHz. Suitable leakage current density in the range of $<10^{-7}$ A/cm² was obtained for this reported dielectric combination, which was similar to some of the other reports with natural protein gate dielectric (Raghuwanshi et al., 2020). Transfer and output characteristics of a typical p-channel device are shown respectively in Figure 3.6 (b) and (c), exhibiting very good saturation in output curve for -5 V operation. Electrical parameters were extracted for 10 OFETs are summarized in Table 3.3. These bilayer gate dielectric devices exhibited lower $V_{TH}$ values in comparison to devices with bare $HfO_2$ gate dielectric (Raghuwanshi et al., 2018). This is possible due to the utilization of SF as an interfacing layer on top of $HfO_2$, which supports the formation of a high-quality interface between the dielectric and semiconductor with a low density of trap states. The average interface trap density ($D_{it}$) for these OFETs is estimated to be 4.74 (±1.80) $\times 10^{11}$ cm$^{-2}$ eV$^{-1}$ using the obtained $SS$ and $C_i$ values in standard equation.

Further, the transfer curves were scanned for 100 consecutive times and shown in Figure 3.6 (d). Negligible variation is observed in the 'on' current ($I_{on}$), however, the off current ($I_{off}$) increases on continuously recording the transfer characteristics as shown in the plot. Figure 3.6 (e) shows the bias-stress induced changes in normalized $I_{DS}$ over the stress period for ~2 hours. A typical gradual decay of ~20 % is observed in $I_{DS}$, indicating good bias-stress stability for an OFET. This decay mostly occurred due to the trapping of charge carriers in the bulk of the semiconductor and at the dielectric-semiconductor interface (Bisoyi et al., 2014). Corresponding bias-induced shift in $V_{TH}$ was also extracted using an earlier reported method and found to be -0.48 V after the stress

period (Tiwari et al., 2009). Figure 3.6 (f) shows the transfer characteristics of a particular OFET under flat and different bending conditions. Relatively stable p-channel characteristics are observed even after bending the device at r = 7 mm. Decay in $I_{DS}$ was observed after repeated bending, probably due to the formation of cracks in TIPS-Pentacene crystal or due to degradation of the quality of dielectric film and dielectric: semiconductor interface (Jiang et al., 2021).

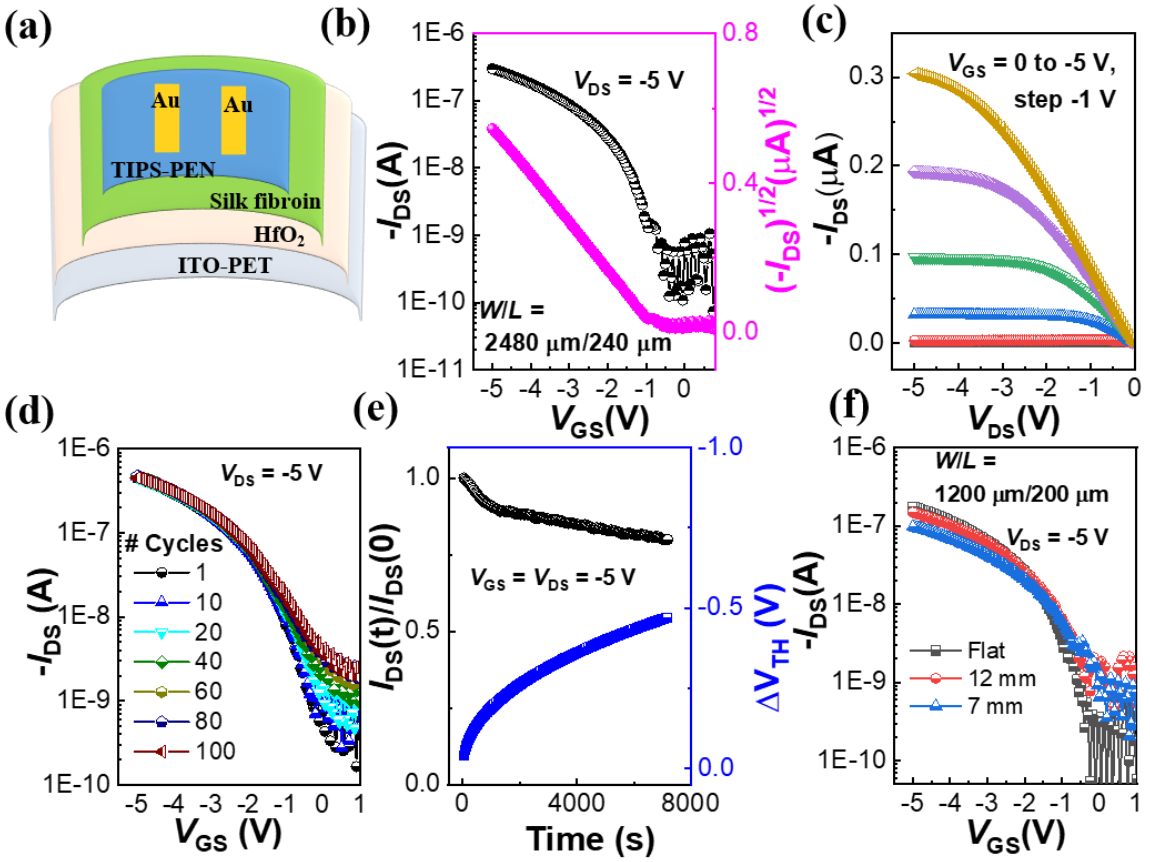



**Figure 3.6** : (a) Device schematic with $HfO_2$/silk-fibroin bilayer gate dielectric. Transfer (b), and output (c), plots for a p-channel device. (d) Transfer characteristics for 100 continuous scans. (e) Normalized $I_{DS}$ plot upon application of constant bias ($V_{GS}$ = $V_{DS}$ = -5 V ) for ~2 hours. (f) Transfer curves measured under different bending conditions.

**Table 3.3 :** Summary of the performance parameters of PVPy dielectric-based transistors.

| $C_i$ (nF. cm$^{-2}$) | Op. V (V) | $k_{p,max}$ (nF. V$^{-1}$ s$^{-1}$) | $\mu_{max}$ (cm$^2$ V$^{-1}$ s$^{-1}$) | $\mu_{avg}$ (cm$^2$ V$^{-1}$ s$^{-1}$) | $V_{TH}$ (V) | SS (V/dec) | $D_{it}$ (cm$^{-1}$ eV$^{-1}$) | $I_{on}/I_{off}$ |
|---|---|---|---|---|---|---|---|---|
| 8.5 | -5 | 14.0 | 1.6 | 0.90 | -0.38 | 0.60 | 4.74×10$^{11}$ | ~10$^3$ |

$C_i$ extracted at 1 kHz.

## 3.4 OFETs with Egg-Albumen Gate Dielectric

The use of emerging edible natural materials in OFETs paves the way for the formation of cost-effective, and eco-friendly smart systems. Egg-albumen, an edible dielectric derived from egg white is another most easily processable inexpensive natural protein, exhibiting good dielectric properties for transistors. Additionally, the water solubility and edibility make it suitable for ingestible and disposable electronics (Cortés-Ramírez et al., 2024). Egg albumen mainly consists of ovalbumin (~54 %) with hydrophilic key functional groups of -–COOH, –$NH_2$, –SH, and –OH, which supports ionic conductivity through the proton conduction (Guo, Li, et al., 2020). In literature, egg albumin exhibits a dielectric constant of ~ 6, which is better than other organic polymers like poly(methyl methacrylate), and polystyrene (Jeon et al., 2013). Moisture sensitivity and leakage current issues in egg-albumen limit the stability of devices. These issues can be suppressed by thermal curing (Jeon et al., 2013), encapsulation, and integration of other

inorganic materials to form hybrid gate dielectrics. Most of the earlier reports utilized oxide-based or thermally evaporated organic semiconductors with egg-albumen (Guo, Li, et al., 2020; Jeon et al., 2013; S. J. Kim et al., 2015; Mandal et al., 2021). However, it is rare to find a solution-processed organic semiconductor with egg-albumen dielectric. In this regard, two types of dielectric combinations were demonstrated with egg albumen. In Type-I devices, a unique hybrid gate dielectric combination of $HfO_2$/egg albumen was explored for demonstration of low-voltage operated p-channel flexible organic transistors (Konwar, Rahi, et al., 2022). Widely explored air-stable TIPS-Pentacene was used as a solution-processed semiconductor layer. However, the use of oxide dielectric is not suitable for biodegradability aspects. Therefore, another bilayer dielectric combination of egg-albumen/gelatin (Type-II) was demonstrated with TIPS-pentacene: polystyrene blend active layer (Konwar, Saxena, Raghuwanshi, et al., 2022d). The addition of a gelatin layer on top of egg-albumen layer may facilitate the desired dielectric properties in the bilayer gate dielectric. Moreover, it offers better dielectric surface by suppressing the roughness of the egg albumen layer. Both these devices exhibit excellent electrical characteristics at -5 V operation with good repeatability and operational stability.

### 3.4.1 Experimentation

Both types (Type-I & Type-II) of devices were fabricated on flexible ITO-PET substrate with BGTC structures. For Type-I devices, a 40 nm thick $HfO_2$ was deposited over ITO using ALD at 100 °C to form the first dielectric layer. Egg albumen, directly extracted from the chicken eggs was ultrasonicated for 15-20 minutes for thorough mixing to prepare a uniform solution to be deposited over $HfO_2$. This solution was then spin-coated at 3000 rpm for 60 s followed by annealing at 100 ℃ for 30 minutes. For semiconductor layer, 0.5 wt. % solution of TIPS-Pentacene in toluene was prepared at 65 ℃ and was drop casted over gate dielectric. In type-II devices, the egg solution was prepared by diluting in deionized (DI) water at a 1:1 volume ratio to reduce viscosity. The prepared solution was spun over the substrate at 2000 rpm for 60s followed by annealing at 105 °C for 10 minutes to reduce moisture content. Gelatin (300 A type) solution was prepared in DI with 10 wt. % by stirring at 60 °C for 2 hours. It was spin-coated over the albumen layer at 2500 rpm for 60 s and annealed at 50 °C for 36 hours to form a thin capping layer. The blend of TIPS-pentacene and polystyrene was deposited to form the active layer as reported earlier. Au top contacts were deposited through a shadow mask using thermal evaporation in both types of devices. Figure 3.7 shows the schematic of Type-I and Type-II devices.

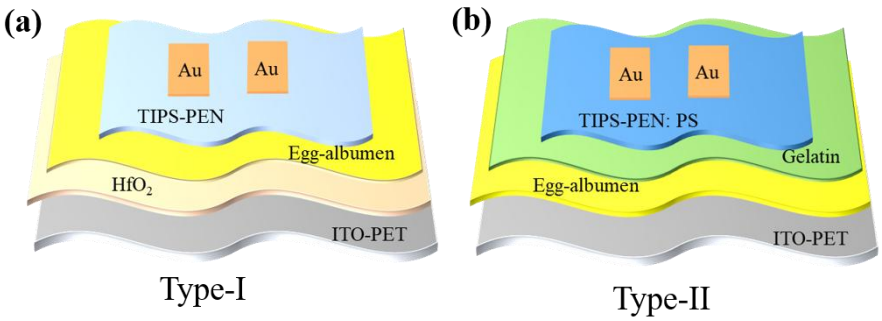



**Figure 3.7 :** Device schematic with BGTC structure for HfO2/egg-albumen (a), egg-albumen/gelatin (b), gate dielectric on a flexible ITO-PET substrate.

### 3.4.2 Transistor Performance

Figure 3.8 summarizes the electrical characteristics of both the devices, showing transfer, output, and repeatability for each type. To evaluate the electrical parameters in Type-I devices, $C_i$ was measured across MIM structure of ITO-$HfO_2$/egg albumen-Au and estimated to be ~10.0 (±0.5) nF/cm² at 1 kHz frequency. On the other hand, $C_i$ was measured through MISM structure of ITO-egg albumen/gelatin-TIPS-Pentacene: PS-Au in Type-II devices, and found to be 7.0 (± 0.5) nF/cm² at 1.0 kHz. The transfer and output characteristics of a particular p-channel device for Type-I and Type-II are shown in Figure 3.8 (a & b) and (d & e), respectively. Excellent switching in transfer curves and outstanding saturation in output characteristics are observed for these devices at -5 V operation. The thin $HfO_2$ layer in Type-I devices helps in mitigating the leakage

issue in these devices. Albumen is a good ion conductive film where mobile ions are generated due to the interaction between water molecules and amino acids. In this biopolymer, $H_2O$ molecules are dissociated to form $H_3O^+$ ions and a side chain of $(CH_2)_2$-$COO^-$ (Guo, Xu, et al., 2020). On applying an external electric field through $V_{GS}$, protons migrate and accumulate at the semiconductor dielectric interface and form an EDL to enhance the gate capacitance density, which is highly dependent on operating frequency.

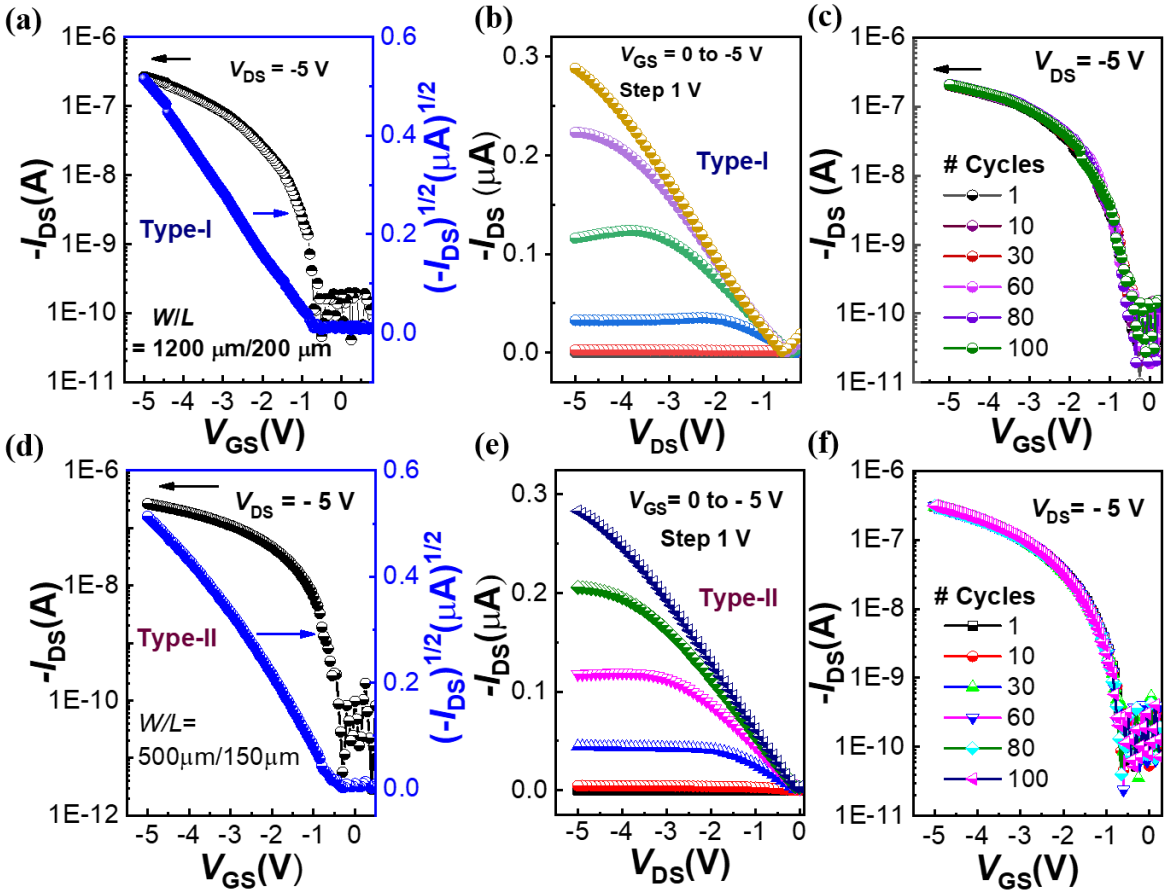



**Figure 3.8 :** Transfer, output, and repeatability characteristics for Type-I (a-c), and Type-II (d-f), devices respectively

Table 3.4 summarizes the extracted electrical parameters including process transconductance ($k_p$). From the table, it can be summarised that Type-II devices exhibit better performance in terms of all parameters. One of the major reasons behind this the smooth surface morphology of obtained film for egg-albumen/gelatin bilayer (RMS ~0.5 nm) as compared to egg-albumen (RMS ~1.0 nm) non-diluted layer on $HfO_2$ surface. In addition, the use of TIPS-Pentacene: PS blend layer supports a high-quality dielectric-semiconductor interface resulting by vertical phase separation (Bharti et al., 2016). The combined effects of blend active layer and the bilayer natural gate dielectrics have resulted in high performance in transistors. The good dielectric: semiconductor interface is confirmed by the low value of $V_{TH}$ and $SS$.

**Table 3.4 :** Extracted electrical parameters for bilayer gate dielectric combinations of HfO2/egg albumen and egg albumen/gelatin transistors.

| Device Type | Op. V (V) | $k_{p,max}$ (nF $V^{-1}$ $s^{-1}$) | $\mu_{max}$ ($cm^2$ $V^{-1}$ $s^{-1}$) | $\mu_{avg}$ ($cm^2$ $V^{-1}$ $s^{-1}$) | $V_{TH}$ (V) | SS (V/dec) | $D_{it}$ ($cm^{-1}$ $eV^{-1}$) | $I_{on}/I_{off}$ |
|---|---|---|---|---|---|---|---|---|
| I | -5 | 10.0 | 1.0 | 0.55 | -0.7 | 0.30 | $5.2\times10^{11}$ | $10^3$ |
| II | -5 | 12.6 | 1.8 | 1.10 | -0.5 | 0.26 | $1.50\times10^{12}$ | $10^4$ |

Further, to study the electrical stability, transfer curves for both devices were scanned continuously for 100 cycles and exhibited excellent repeatability as shown in Figure 3.8 (c & d). In

addition, cyclic stability was investigated for devices with $HfO_2$/egg-albumen by applying continuous voltage pulses, exhibiting steady switching characteristics (Konwar, Rahi, et al., 2022). Whereas bias-stress stability was performed for devices with egg-albumen/gelatin dielectric and a decay of 19 % was obtained after 1 hour stress period, which is common for any polymer-based OFET devices (Konwar, Saxena, Raghuwanshi, et al., 2022d). From these results, it can be summarized that coating a thin polymer layer on top of egg-albumen layer provides good dielectric properties in OFETs. However, it is still challenging to utilize a single layer of egg-albumen layer as gate dielectric with solution-processed organic semiconductor. Thus, this dissertation does not focus on additional exploration of the egg albumen as gate dielectric in OFETs.

## 3.5 OFETs with Chitosan Gate dielectric

Apart from natural proteins, polysaccharide-based dielectrics show promising characteristics to be used as biodegradable gate dielectric candidates in OFETs. Chitosan (CS) is a linear polysaccharide derived from the deacetylation of chitin that is mostly synthesized from various living organisms such as shrimp, crabs, insects, etc. CS contains amino polysaccharide molecules having a strong positive electrical charge and is available in various forms including nanoparticles, microspheres, hydrogels, fibers, and others. It offers prominent functional and biological characteristics of non-toxicity, and antimicrobial properties for biomedicine, drug delivery systems, food industry, wastewater treatment, and tissue engineering. CS exhibits ion-conducting behavior due to the presence of hydroxyl and protonated amine groups in their backbone, making it an excellent proton-conducting gate dielectric layer in transistors (Feng et al., 2016). However, achieving a homogenous, defect-free film is challenging due to the viscosity and gel-like properties of CS solution. The dielectric characteristics of CS have been examined in many oxide-based transistors owing to its high capacitance density, thermal and mechanical stability, and potential towards biodegradable electronics (Kumar et al., 2020; Min & Cho, 2020). Nonetheless, challenges such as surface roughness and leakage current require additional attention to enhance the performance of devices utilizing solution-processable OSCs. Similarly, gelatin has been considered to be a very promising gate dielectric as it provides a very smooth surface morphology which further helps to grow high-quality semiconductor crystals (Raghuwanshi et al., 2020). An optimal gate dielectric with reduced leakage current and high capacitance density is essential to demonstrate high-performance devices. Adding a thin gelatin layer on the top of chitosan can suppress the leakage issue by providing a high-quality dielectric: semiconductor interface. Here, we have demonstrated flexible OFET devices with a bilayer of chitosan and gelatin gate dielectric. TIPS-Pentacene: PS blend was chosen to form the active layer due to vertical phase separation providing a high-quality dielectric-semiconductor interface, as previously demonstrated by our group (Raghuwanshi et al., 2018).

### 3.5.1 Device Fabrication

OFET devices were demonstrated on ITO-coated PET substrate with BGTC structure. Chitosan (CS) (≥75% deacetylated) was purchased from Sigma Aldrich. To prepare the dielectric solution, 2 wt. % CS was dissolved in aqueous acetic acid at 50 °C for 6 hours. The prepared solution was spin-coated at 2500 rpm for 60 s and further annealed at room temperature for 24 hours to form a better film. Gelatin solution with 10 wt. % was prepared d in DI at 60 °C for 2 hours. Further, the prepared solution was spin-coated on top of the CS layer using the same spin-coating conditions, i.e., at 2500 rpm for 60 s, followed by 36 hours of annealing at 50 °C to form a thin encapsulation layer. The blend TIPS-Pentacene: PS layer was deposited over the bilayer gate dielectric through the drop-casting process as mentioned in the previous section. Finally, Au top contacts were deposited through a shadow mask.

### 3.5.2 Transistor Performance

Figure 3.9 (a) shows the schematic of the device structure on a flexible substrate. Transfer and output characteristics are shown in Figure 3.9 (b) and (c), respectively. All these devices had shown excellent p-channel behavior with high saturation in output characteristics for -5 V

operation. $C_i$ value was determined using the MISM structure of ITO/CS/gelatin/TIPS-Pentacene: PS/Au and found to be 7.5 (± 0.5) nF/cm² at 1.0 kHz, which is the lowest possible frequency attainable in Keithley 4200. Important electrical parameters such as $\mu$, $V_{TH}$, $SS$, $I_{on}/I_{off}$, and $D_{it}$ were extracted from transfer characteristics at the saturation region, as discussed in the previous chapter. The thin gelatin layer minimizes the top surface roughness of chitosan leading to a suitable interface with active layer. Also, the TIPS-pentacene: PS blend helps to accomplish higher current conduction by reducing the charge trapping sites at the interface of the bilayer gate dielectric. Summary of average device parameters for 10 OFET devices is given in Table 3.5.

**Table 3.5 :** Extracted electrical parameters for OFETs with chitosan/gelatin bilayer gate dielectric.

| $C_i$ (nF. cm$^{-2}$) | Op. V (V) | $k_{p,max}$ (nF. V$^{-1}$ s$^{-1}$) | $\mu_{max}$ (cm$^2$ V$^{-1}$ s$^{-1}$) | $\mu_{avg}$ (cm$^2$ V$^{-1}$ s$^{-1}$) | $V_{TH}$ (V) | SS (V/dec) | $D_{it}$ (cm$^{-1}$ eV$^{-1}$) | $I_{on}/I_{off}$ |
|---|---|---|---|---|---|---|---|---|
| 7.5 | -5 | 12.0 | 1.6 | 1.1 | -0.5 | 0.16 | $7.6\times10^{11}$ | $>10^3$ |

Further, the transfer curves were scanned continuously for 100 cycles. A highly repeatable overlapping behavior was observed as shown in Figure 3.9 (d). A very small change in $I_{DS}$ and $V_{TH}$ was observed as shown in Figure 3.9 (e), specifying excellent repeatability for practical applications. For bias-stress test, devices were subjected to a constant bias of $V_{DS} = V_{GS} = -5$ V for 1 hour, and the change in $I_{DS}$ with time was studied. The normalized $I_{DS}$ exhibits decay with time reaching 30% decay in one hour, which could be due to charge trapping at the functional groups like -OH present in natural dielectrics which causes more trap sites at semiconductor dielectric interfaces. The $\Delta V_{TH}$ was extracted as explained earlier and found to be increasing with time as expected, as shown in Figure 3.9 (f) (Mathijssen et al., 2007). Moreover, OFETs with pristine gelatin layer with TIPS-Pentacene: PS exhibited excellent transistor performance with electrical stability and circuit applicability (G. Konwar, S. Bhattacharjee, et al., 2023).

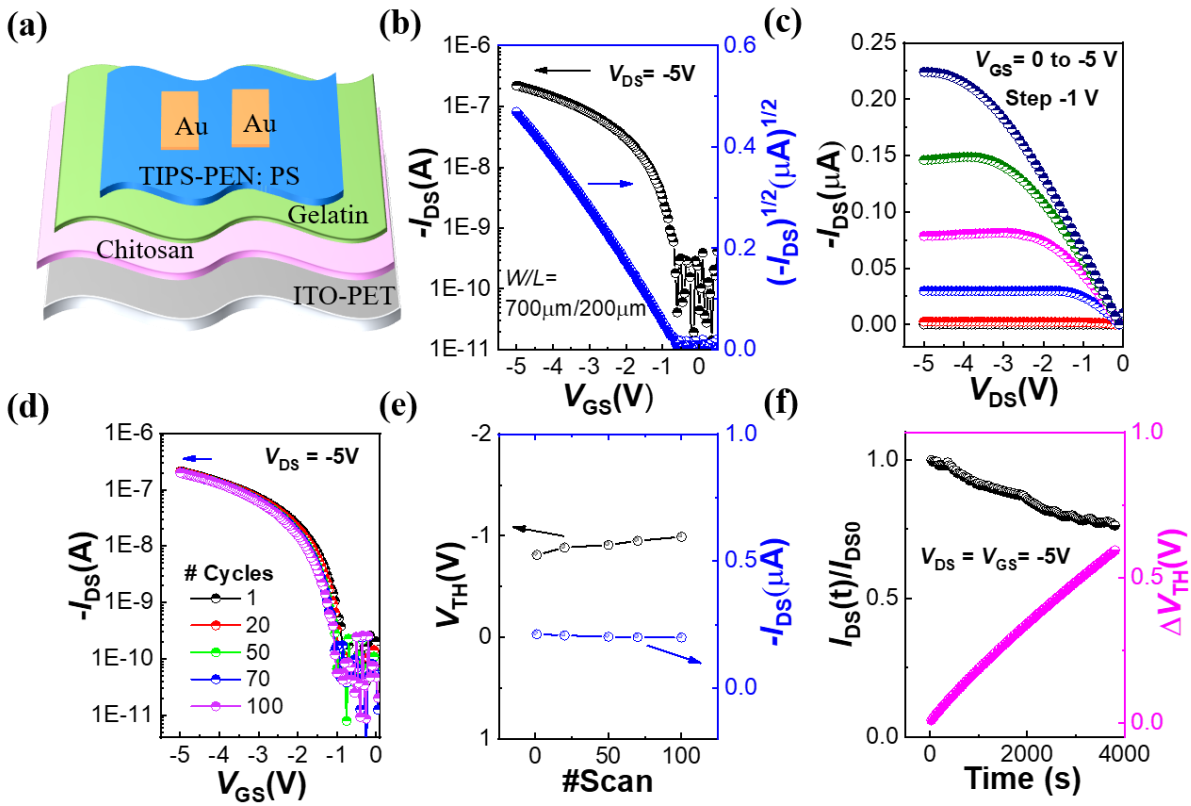



**Figure 3.9 :** (a) Device schematic; (b) Transfer and (c) output characteristics. (d) Multiple scanning for 100 cycles, (e) Changes in $V_{TH}$ and $I_{DS}$ during the scanning period. (f) Normalized $I_{DS}$, and change in $\Delta V_{TH}$ over stress period.

These findings suggest that the bilayer of natural biopolymers can be excellent emerging gate dielectric candidates for flexible and printable green electronic systems. The pristine form of the CS dielectric layer was not further investigated in this thesis due to its problem with film formation and leakage current issues. To improve the mechanical strength pristine CS was utilized as a tuning agent in combination with gelatin polymer for the enhancement of transistor stability upon bending as discussed later in Chapter 6.

## 3.6 OFETs with Cellulose Derivative Gate dielectric

Cellulose is one of the most abundantly available polysaccharides, derived from various renewable sources including plants, wood, cotton, seagrass, etc. Cellulose is composed of β-D-glucose units linked via β-1,4 glycosidic bonds containing hydroxyl (-OH) groups, enabling hydrogen bonding and easy functionalization for chemical modifications. In comparison to other natural proteins, cellulose offers high mechanical stability, and highly stable characteristics under varying humidity and temperature (Zhao et al., 2021), showing degradability in microbial activity making it a suitable eco-friendly and biodegradable candidate. However, cellulose has been synthetically modified into various versions to enhance the dielectric properties such as dielectric constant, temperature stability, and mechanical stability in comparison to the pristine form of cellulose (Bae et al., 2017; Bonardd et al., 2018; Cunha et al., 2022). Some of these synthesized versions have been utilized as gate dielectric in transistors. Among these, cyanoethyl cellulose (CEC), has been recently demonstrated as a potential gate dielectric for eco-sustainable devices (Gargi Konwar et al., 2023; G. Konwar & S. P. Tiwari, 2024). CEC is synthesized by the substitution of cyanoethyl group by Michael addition from alkalified cellulose and acrylonitrile, and its physical and chemical properties are highly dependent on the degree of substitutions (DS) (B. Wang et al., 2019). CEC has a high *k* value with some remarkably distinctive qualities, including excellent heat and acid tolerance, stability to microbial attack, low moisture regain rate, and outstanding mechanical qualities (Faraji et al., 2016). Integration of polar cyanoethyl groups strengthens the bonds between fibre chains and increases temperature stability (Sefain et al., 1994). In addition, it has low dielectric loss with high water resistance and self-extinguishing performance (Jia et al., 2015), compared to many other natural dielectrics reported earlier which offer lower *k* values. Due to these favorable properties, CEC can be an excellent gate dielectric for high-performance decomposable and biodegradable transistors Low voltage operation was achieved by strategies such as integration of nanoparticles in CEC for solution-processed p-channel OFETs (Faraji et al., 2016), however, similar other reports are difficult to find in recent years. Here, a pristine layer of CEC was demonstrated as gate dielectric with blend of TIPS-pentacene: PS as an active layer for flexible OFETs. Excellent p-channel behavior was obtained for -5 V operation with excellent electrical and operational stability.

### 3.6.1 Device Fabrication and Electrical Characterization

OFET devices with BGTC structures were fabricated on ITO-coated PET substrates. The substrate was first cleaned by immersing organic solvents as discussed earlier. CEC (~2.6 mol cyanoethylation) dielectric material was purchased from Sigma Aldrich and used directly without any purifications. For the preparation of dielectric solution, CEC was dissolved in N, N-Dimethylformamide (DMF) (HPLC, ≥99.5 %, Sigma Aldrich). CEC solution with 10% was prepared in DMF at 60 °C and continuously stirred for 24 hours. Solutions were spin-coated at 2000 rpm for 60 s after filtering through a polytetrafluoroethylene (PTFE) syringe filter with a pore size of 0.45 µm. Further, the films were annealed at 50 °C for 48 hours to form a smooth gate dielectric film. For the active layer, blend of TIPS-Pentacene: PS was drop cast on CEC dielectric and the same was left for drying at room temperature for the formation of semiconductor crystals. Finally, Au top source/drain contacts were deposited through a shadow mask using thermal evaporation.

Keithley 4200 SCS analyzer was used to characterize the devices in ambient conditions. Performance parameters including $k_p$, $V_{TH}$, $\mu$, and *SS* were extracted from the transfer plot. $C_i$ was measured through the ITO/CEC/TIPS-pentacene: PS/Au MISM structure were fabricated with the same process that was used for OFET devices. MISM is preferred for $C_i$ extraction over metal-

insulator-metal to consider the additional series capacitance of PS layer, which is known to be created by vertical phase separation of the TIPS-pentacene: PS blend. Here, $C_i$ value was measured at 1 kHz and found to be ~5.8 nF/cm$^2$, which was further used to calculate $\mu$ at saturation regime. The effect of bending was studied upon application of tensile stress for three different bending radii ($R_{bend}$) of 12, 7, and 5 mm.

### 3.6.2 Transistor Performance

Figure 3.10 (a) shows the schematic of the fabricated OFET with BGTC structure. AFM image of top surface of CEC layer was observed for a scanning area of 10×10 µm and a root mean square (RMS) value of 2.5 (±0.5) nm was obtained. Moreover, the leakage current density for CEC dielectric across the MISM structure for -5 V was obtained in the range of <$10^{-6}$ A/cm$^2$, indicating good insulating property of CEC gate dielectric layer for transistor operation.

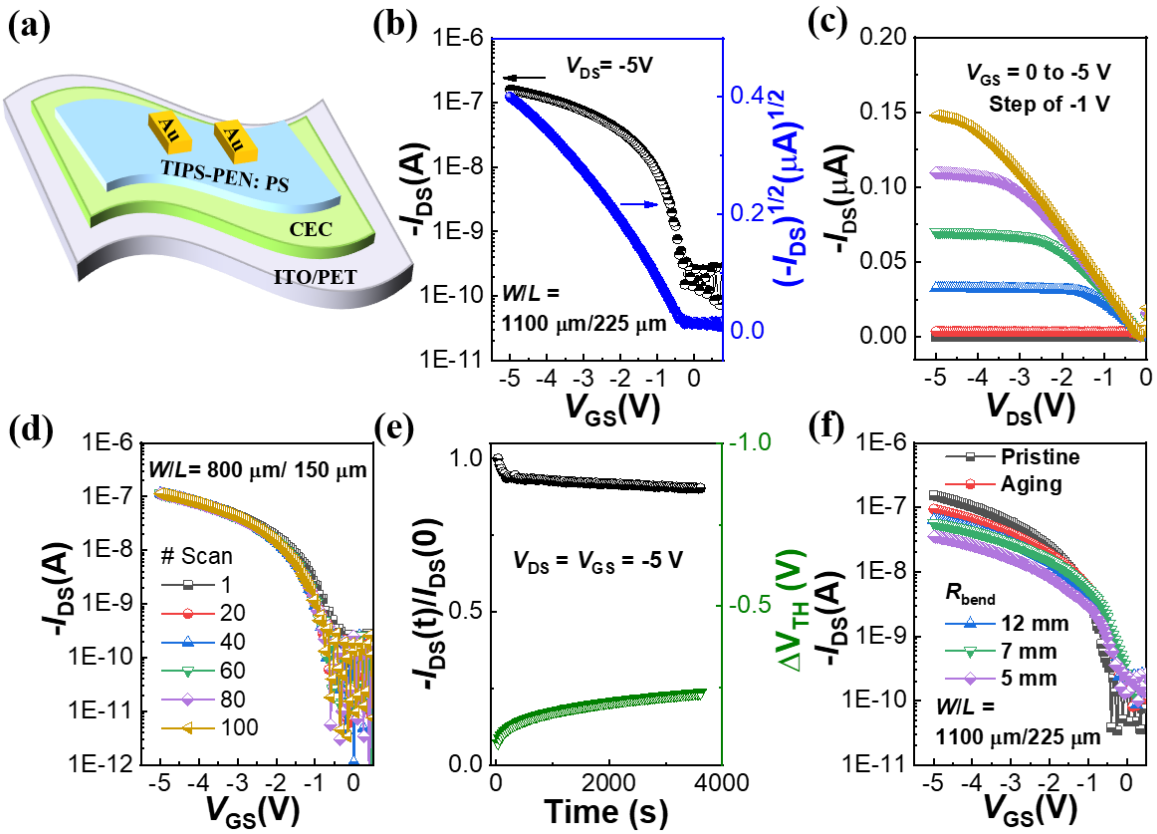



**Figure 3.10 :** (a) Device schematic using CEC as gate dielectric; (b) Transfer and (c) output characteristics, for single OFET. (d) Multiple scanning for 100 cycles, (e) Normalized $I_{DS}$, and change in Δ $V_{TH}$ over stress period.

The transfer and output characteristics for various $V_{GS}$ values are shown respectively in Figure 3.10 (b) and (c), exhibiting good saturation in characteristics for -5 V operation. The maximum and average $k_p$ values of 6.2 and 5.0 (±1.2) nF/V.s were exhibited with low $V_{TH}$ value of -0.20 (±0.13) V. These $k_p$ values are slightly better than those reported for devices with some other polysaccharide gate dielectrics such as triacetate cellulose and almond gum (Bae et al., 2017; Seck, Mohammadian, Diallo, Faraji, Erouel, et al., 2020). A suitable low *SS* value of 0.50 (±0.16) V/decade was extracted from these devices. Figure 3.10 (d) shows the repeatability plots of transfer characteristics for scanning up to 100 repeated cycles. Nearly overlapped transfer curves are observed from these devices. Extracted parameters are summarized in Table 3.6. Figure 3.10 (e) shows the bias-stress induced changes in $I_{DS}$ and $V_{TH}$ for a constant DC bias for 1-hour stress period. The normalized decay in $I_{DS}$ ($I_{DS}$(t)/ $I_{DS}$ (0)) was studied and shown in the left side of the Y-axis, showing an acceptable decay of ~ 10 %. This much degradation is quite obvious for a polymer based organic transistor, where variation upon application of bias stress is primarily

occurred due to the trapping of carriers from the channel into dielectric and at dielectric: semiconductor interface (Bisoyi et al., 2014). The plot of transfer characteristics for a single device under different device conditions such as in pristine case, exposure to ambient for 10 months, and application of bending with different radii ($R_{bend}$) (12, 7, and 5 mm) are shown in Figure 3.10 (f).

**Table 3.6:** Extracted electrical parameters with CEC gate dielectric for flexible OFETs.

| $C_i$ (nF. cm$^{-2}$) | Op. V (V) | $k_{p,max}$ (nF. V$^{-1}$ s$^{-1}$) | $\mu_{max}$ (cm$^2$ V$^{-1}$ s$^{-1}$) | $\mu_{avg}$ (cm$^2$ V$^{-1}$ s$^{-1}$) | $V_{TH}$ (V) | SS (V/dec) | $D_{it}$ (cm$^{-1}$ eV$^{-1}$) | $I_{on}$/ $I_{off}$ |
|---|---|---|---|---|---|---|---|---|
| 5.8 | -5 | 6.2 | 1.06 | 0.86 | -0.20 | 0.50 | $2.62\times10^{11}$ | ~$10^3$ |

For the investigation of shelf life, the devices were characterized after 10 months of fabrication and all crucial device parameters were extracted to study their stability in environment. In this experiment, the devices were kept in a lab environment which was fairly constant throughout the study. The same transistors were further investigated upon the application of tensile bending with varying the $R_{bend}$. The devices have shown good switching in transfer characteristics even after extreme bending and aging conditions due to the possible changes in humidity and temperatures in the lab during the experiments. The degradation in transistor characteristics might occur as a result of the formation of trap sites on the surface of semiconductor or at the interface of dielectric: semiconductor due to the adsorption of water molecules into these regions (Subbarao et al., 2015). Devices also exhibited good stability upon 200 continuous bending cycles (G. Konwar & S. P. Tiwari, 2024). To demonstrate transistor performance at low operating voltage, CEC was also investigated by combining with a thin $HfO_2$ layer (Konwar, Kim, et al., 2024); nevertheless, the use of an inorganic layer is not preferable for biodegradable electronics. Due to the good transistor performance with a single CEC layer, this gate dielectric was further explored with a paper substrate to demonstrate decomposable and biodegradable flexible OFETs.

## 3.7 Summary of Transistor Performance Parameters

Electrical parameters for various reported biocompatible and natural polymer dielectric combinations on different substrates are summarized in Table 3.7. The directly extracted electrical parameters from transfer curves such as $k_p$, $V_{TH}$, $SS$, and $I_{on}/I_{off}$. For natural polymer-based OFETs, $k_p$ value was discussed to avoid any incorrect estimation of performance parameters ($\mu$ and $D_{it}$) in case of under/overestimation of $C_i$ value which is dependent on frequency. In natural polymer-based OFETs, it is required to measure the capacitance for low frequencies due to the slow polarization of mobile ions.

**Table 3.7 :** Summary of performance parameters for the reported biocompatible and natural polymer gate dielectric combinations.

| Substrate | Dielectric | OSC | Op.V. (V) | $K_{p,max}$ (nF/V.s) | $V_{TH}$ (V) | SS (V/dec | $I_{on}$/ $I_{off}$ | Ref. |
|---|---|---|---|---|---|---|---|---|
| ITO-Glass | PVPy | TIPS-Pentacene: PS | -5 | 10 | -0.2 | 0.68 | ~$10^3$ | (G. Konwar, S. Bhattacharjee, et al., 2023) |
| FTO-Glass | Gelatin | TIPS-Pentacene: PS | -5 | 12.2 | -0.9 | 0.30 | >$10^3$ | (G. Konwar, S. Bhattacharjee, et al., 2023) |
| ITO-PET | $HfO_2$/Silk-fibroin | TIPS-Pentacene: PS | -5 | 14.0 | -0.38 | 0.60 | ~$10^3$ | (G. Konwar, et al., 2024, submitted) |
| ITO-PET | $HfO_2$/Egg-albumen | TIPS-Pentacene | --5 | 10.0 | -0.7 | 0.30 | $10^3$ | (Konwar, Rahi, et al., 2022) |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| ITO-PET | Egg-albumen/ gelatin | TIPS-Pentacene: PS | -5 | 12.6 | -0.5 | 0.26 | $10^4$ | (Konwar, Saxena, Raghuwanshi, et al., 2022d) |
| ITO-PET | Chitosan/ gelatin | TIPS-Pentacene: PS | -5 | 12.0 | -0.5 | 0.16 | $>10^3$ | (Konwar, Saxena, Raghuwanshi, et al., 2022a) |
| ITO-Glass | CEC | TIPS-Pentacene: PS | -5 | 9.0 | -0.4 | 0.70 | $\sim10^3$ | (Gargi Konwar et al., 2023) |
| ITO-PET | CEC | TIPS-Pentacene: PS | -5 | 6.2 | -0.2 | 0.50 | $\sim10^3$ | (G. Konwar & S. P. Tiwari, 2024) |
| ITO-PET | $HfO_2$/CEC | TIPS-Pentacene: PS | -3 | 6.6 | -0.80 | 0.34 | $\sim10^3$ | (Konwar, Kim, et al., 2024) |

From the table, it can be summarized that, all these dielectric combinations exhibit excellent p-channel transistor performance for low voltage operation (-5 V). Furthermore, devices incorporating a single layer of gelatin or CEC as gate dielectric exhibited transistor performance comparable to that of devices with bilayer dielectric combinations. This indicates that a single polymer dielectric layer of gelatin or CEC is sufficient to obtain stable and reliable device operation without the need of additional dielectric stacking, which make them promising candidate for further investigation in flexible OFETs. In this thesis, these two polymers were explicitly investigated on different substrates to demonstrate specific applications.

## 3.8 CONCLUSION

In this chapter, different biocompatible or biodegradable polymers such as PVPy, silk-fibroin, chitosan, egg-albumen, gelatin, and CEC were investigated as gate dielectrics in OFETs. A widely explored semiconductor TIPS-Pentacene or blend of TIPS-Pentacene: PS was utilized for the demonstration of excellent p-channel transistor performance. All these devices exhibited excellent characteristics for -5 V with good electrical and operational stability. PVPy, a highly soluble biocompatible dielectric was successfully demonstrated in transistors with TIPS-Pentacene: PS, exhibiting good transistor performance for up to 3 months in ambient. However, to focus more specifically on biodegradability aspects, this work was not further investigated in this dissertation due to the lack of biodegradability of this polymer. Further, a few promising natural polymers such as egg-albumen, silk-fibroin, chitosan, gelatin, and a synthesized cellulose CEC were explored with either as a single layer or as bilayer gate dielectric combinations. The pristine form of egg-albumen, silk-fibroin, and chitosan exhibited poor stability and high leakage issues, demanding suitable processing and dielectric modifications to be used as suitable gate dielectric candidates in OFETs. Devices with bilayer of natural polymers egg-albumen/gelatin and chitosan/gelatin showed better suitability in the direction of biodegradable electronics since the inorganic $HfO_2$ layer constraints the environment degradability. These two bilayer polymer gate dielectric devices exhibited almost similar performance due to the use of similar top layer gelatin in both cases. Here, the property of the gelatin layer was more dominated as compared to the bottom gate dielectric layers. Moreover, both gelatin and CEC dielectric exhibited promising dielectric characteristics as a single layer for the demonstration of high-performance OFETs. In this dissertation, both these gelatin and CEC polymers were investigated for enhancing the transistor performance along with additional functionality and decomposability for the development of eco-sustainable and biodegradable electronics.

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