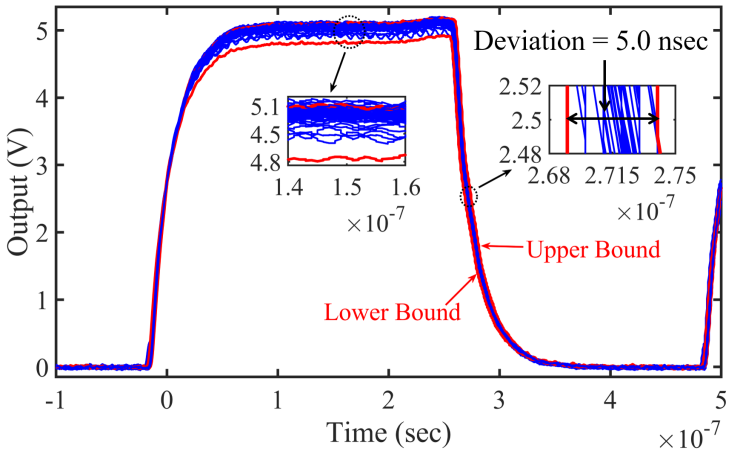
3
Proposition: Analytical Modeling of Variability-Aware Jitter

Variability issues, along with the presence of various noise sources, can significantly affect the performance of the system. This chapter presents an integrated approach to estimate the timing uncertainty in VLSI circuits, which considers variability issues and various noise sources together in the circuit. The proposed approach can play a critical role in order to obtain robust performance of the systems.

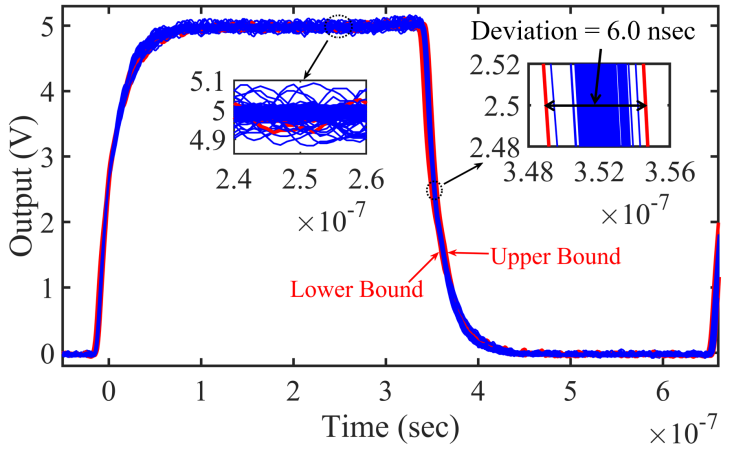
3.1 Introduction

To better understand the impact of variability issues on the performance of a system, let us first discuss a case study. In Figure 3.1.1, to depict the impact of variability, the output responses of several samples of a CMOS inverter IC are shown. Two cases are presented here, considering two different CMOS Hex Inverter ICs. In the first case, 60 CMOS inverters (using 60 samples of IC M74HC04) are taken. In the second case, 180 CMOS inverters (using 180 samples of IC SN74HC04) are taken. The output responses are obtained by applying the same biasing voltage and input data to all the samples in both the cases. The output responses obtained from all the samples are then overlapped over each other as depicted in Figure 3.1.1 for both the first and second cases. From both the figures, Figure 3.1.1(a) and 3.1.1(b), it can be observed that there is a significant deviation in the output responses obtained using different samples of inverters. The worst-case deviations are represented by upper bound (UB) and lower bound (LB). For a data rate of 3 Mbps, the timing variations in these extreme responses span up to 5.0 nsec and 6.0 nsec at the midpoint of the falling transition edge in 3.1.1(a), and in Figure 3.1.1(b), respectively. It is very clear that the output response of one sample of an IC model is significantly different from another one.

This disparity in output responses of inverters indicates that no single IC is precisely identical to the other ones, even though they are manufactured by the same manufacturer; i.e., every sample of CMOS inverters is slightly different from the other one and exhibits variability issues due to variations in fabrication process parameters such as channel length, oxide thickness, and doping concentration, etc. The values of these parameters may differ from their intended values during the fabrication. Consequently, the output response of the IC also varies from the actual output response, depicting a stochastic nature, and the performance of the IC degrades. The problems related to variability become even more acute due to the presence of noise in the system, and the performance of the system significantly degrades, which may be one of the reasons for the failure of an electronic system. Therefore, it is crucial to investigate the performance of circuits and measure the variations in their output responses due to noise and stochastic variations in



(a)



(b)

Figure 3.1.1: Measured output responses of CMOS Inverter: (a) 60 samples of IC M74HC04, and (b) 180 samples of IC SN74HC04.

the process parameters of the transistors. Designers should consider these factors during various design stages and employ some appropriate techniques to mitigate this problem to ensure the reliable and robust performance of the system.

Problems associated with variability issues and jitter estimation have been widely discussed in the literature [Saha, 2010], [Zhang *et al.*, 2013], [Vande Ginste *et al.*, 2012], [Dani *et al.*, 2022], and [Wang *et al.*, 1971], but all of them are separate studies. A detailed study on jitter estimation is already discussed in Chapter 2. Several works that study the variability issues in VLSI circuits are as follows. Article [Saha, 2010] provides a comprehensive overview of the various sources that can cause variability issues, and their impact on the performance of VLSI systems. The work in [Saha, 2014] presents a methodology to identify variability-sensitive parameters in nanoscale MOSFETs, map them to compact model parameters, and create statistical models for variability-aware VLSI design. Process variability in scaled CMOS technologies significantly impacts the functionality, yield, and reliability of modern integrated circuits. The work in [Chordia and Tripathi, 2022a] presents an automated framework for variability analysis of CMOS circuits using metaheuristic optimization techniques. It presents variability analysis of phase noise in 2.4 GHz CMOS oscil-

lator. Variability analysis in a CMOS oscillator using various stochastic approaches is presented in [Chordia and Tripathi, 2022b]. The work in [Zhang *et al.*, 2013] presents a simulator for statistical circuit analysis, which employs a polynomial chaos (PCE) approach for variability analysis. Several other contributions have been made in the literature to model jitter in the VLSI circuits. The work in [Dani *et al.*, 2022] presents a time domain jitter estimation considering process-voltage-temperature (PVT) variations of single-ended ring oscillator (SERO). The work [Souilem *et al.*, 2022] presents a study of power supply and ground-noise induced jitter (PGSIJ) simulation for a cascaded inverter output buffer. This analysis covers the I/O buffer transient simulation under power and ground supply voltage variation at the three corners of process, voltage, and temperature (PVT).

As discussed above, many contributions have been made in the literature that study variability problems and jitter analysis in VLSI circuits separately. This work attempts to investigate the performance of a system when there are variability issues along with the various off-chip noise sources. It presents the development of variability-aware model of power supply-induced jitter (PSIJ) in CMOS inverters. This could have significant implications for designing and optimizing integrated circuits in the presence of variability and noise. The specific contributions made by this work are as:

- It proposes an integrated approach that considers the effect of variability while estimating power supply-induced jitter in VLSI circuits.
- It develops a variability-aware model of power supply-induced jitter in CMOS inverters.
- The proposed investigation presents several examples considering simulation and measurement results to provide a comprehensive study.

3.2 Noise and Variability in CMOS Inverters

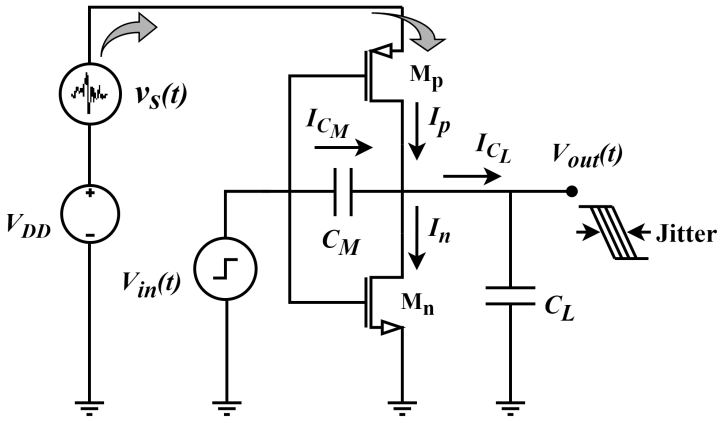


Figure 3.2.1: CMOS Inverter having power supply noise.

As discussed in the previous section, the performance of an integrated circuit degrades due to the presence of various noise sources and variability-related issues. In this section, as an example circuit, the behavior of the CMOS inverter is studied, considering the effect of power supply noise and variations in design parameters together. It employs the analytical approach presented in Chapter 2 to estimate jitter in CMOS inverters in presence of variability and PSN. For this,

variation in widths $\boldsymbol{W_p}$ and $\boldsymbol{W_n}$ (taken as random variables[1]) of the transistors pMOS and nMOS, respectively, along with PSN, are considered. The schematic of the CMOS inverter in the presence of PSN $\big($denoted by $v_s(t)\big)$ is shown in Figure 3.2.1. Here, $\boldsymbol{C_M}$ is the sum of gate-to-drain capacitance of pMOS (i.e., $\boldsymbol{C_{gd_p}}$) and nMOS (i.e., $\boldsymbol{C_{gd_n}}$). It is included in the analysis to consider the effect of initial overshoot in the output response.

$$\boldsymbol{C_M} = \boldsymbol{C_{gd_p}} + \boldsymbol{C_{gd_n}}. \tag{3.1}$$

Further, gate-to-drain capacitance is the sum of a part of gate-to-channel capacitance and gate-to-drain overlap capacitance per unit channel width and can be written as:

$$\boldsymbol{C_{gd_p}} = \frac{\boldsymbol{W_p} L_p C_{ox}}{2} + \boldsymbol{W_p} C_{ov},\ \boldsymbol{C_{gd_n}} = \frac{\boldsymbol{W_n} L_n C_{ox}}{2} + \boldsymbol{W_n} C_{ov} \tag{3.2}$$

where $\{\boldsymbol{W_p}$ and $L_p\}$ and $\{\boldsymbol{W_n}$ and $L_n\}$ are the channel width and channel length of pMOS and nMOS, respectively. Next, C_{ox} and C_{ov} are the oxide capacitance and gate-to-drain overlap capacitance per unit channel width, respectively. C_L is the load capacitance. Other parasitics are neglected to avoid the complexity of analysis. The rising edge of a fast-switching input signal is considered for the analysis. With the rising voltage level of the input signal, the operating modes of the transistors change; one of the transistors operates in cutoff mode, while an other one operates either in linear or saturation mode. The instantaneous fluctuation in power supply and the variability issues in the circuit shifts the transition edges of the output signal from their ideal positions (i.e., when $v_s(t) = 0$ and no variability issues are present in the circuit) and introduce jitter at the output. This output jitter depends on various parameters such as parasitics and sizes of the transistors, temperature, rise/fall time of the input data signal, and load capacitance [Arora *et al.*, 2021b]. The equation for the rising edge of the input signal can be expressed as:

$$V_{in}(t) = \begin{cases} 0, & \text{if} \quad t < 0 \\ V_{DD}(t/\tau), & \text{if} \quad 0 \le t < \tau \\ V_{DD}, & \text{if} \quad t \ge \tau \end{cases}, \tag{3.3}$$

where τ is the rise time of the input data signal. The corresponding falling edge of the output response has been considered to develop the analytical model of jitter induced due to the variations in design parameters and PSN source. The input-output plot of the CMOS inverter is shown in Figure 2.2.2 in the last chapter. Here, the entire falling edge of the output is divided into five different regions [2], based on the modes of conduction (saturation, linear, and cutoff) of the transistors M_n and M_p [Arora *et al.*, 2021b]. A small-signal noise source $v_s(t)$ is inserted at the supply terminal of the inverter, and it is represented in terms of the Taylor series to obtain the input-output relationships in different regions as given in equation (2.20).

3.2.1 Input-Output Relationship of Region-IV

Analytical equations are developed considering the width of the transistors as random variables ($\boldsymbol{W_n}$ and $\boldsymbol{W_p}$) in the presence of PSN. As shown in Figure 2.2.2, in Region-IV, the input voltage reaches V_{DD} and becomes constant to V_{DD}. The transistors (M_n and M_p) remain in saturation and cutoff modes, respectively [Riley and Hobson., 2011]. The output expression for this region can

[1]The random variables are denoted by bold letters.

[2]The word "region" should not be misconstrued by readers with the operating regions (such as linear, cut-off, and saturation) of the transistors. A different word "mode" has been used to mention the operating regions.

be written as:

$$\boldsymbol{V_{out}(t)} = \boldsymbol{V_{34}} - 0.5 \cdot \boldsymbol{\gamma_3}(V_{DD} - V_{TN})^2 \cdot (t - T_3), \tag{3.4}$$

where

$$\boldsymbol{V_{34}} = V_{DD} + \frac{\boldsymbol{\gamma_1} V_{DD}}{\tau}(T_3 - T_2 - 1) - \frac{\boldsymbol{\gamma_3} V_{TN}^3}{6V_{DD}} + \frac{\boldsymbol{\gamma_3}\tau}{3V_{DD}}\left[\frac{V_{DD}}{\tau}(T_3 - T_2) - V_{TN}\right]^3 + \sum_{n=1}^{N}\left[A_{s_n}\sin\phi_{s_n}\right. \tag{3.5}$$

$$\left. + \sum_{k=1}^{\infty}(s_{n_k} - \boldsymbol{b_{n_k}})(T_2 - T_1)^k + \sum_{k=1}^{\infty}(s_{n_k} - \boldsymbol{a_{n_k}})T_1^k\right], \tag{3.6}$$

where $T_2 = \tau(V_{DD} - |V_{TP}|)/V_{DD}$, $T_3 = \tau$ and $\boldsymbol{V_{34}}$ is the random variable depending on $\boldsymbol{W_n}$ and $\boldsymbol{W_p}$ directly/indirectly, and it needs to be added in the output expression to maintain the continuity between the Region-III and Region-IV. Next, $\boldsymbol{\gamma_1} = \boldsymbol{C_M}/(C_L + \boldsymbol{C_M})$, $\boldsymbol{\gamma_3} = \boldsymbol{\beta_n}/\{(1+\delta_n)(C_L + \boldsymbol{C_M})\}$, $\boldsymbol{\beta_n} = \mu_n C_{ox}\boldsymbol{W_n}/L_n$. δ_n is the constant term obtained from the bulk charge equation of nMOS device [Bisdounis *et al.*, 1998] and [Tsividis, 2004]. Output expressions for other regions can be found in Appendix A.

3.2.2 Dependence of Output Response on Temperature

As discussed in Section- 3.2.1, the proposed analytical approach uses only three device parameters for the estimation of jitter such as: gate to drain capacitors $\{\boldsymbol{C_{gd_p}}, \boldsymbol{C_{gd_n}}\}$, threshold voltages $\{V_{TP}, V_{TN}\}$ and transconductance parameters $\{\boldsymbol{\beta_p}, \boldsymbol{\beta_n}\}$. Device parameters (particularly threshold voltages and transconductance parameters) are affected by temperature variations [Khanna, 2023],[Klaassen and Hes, 1986], and [Tsividis, 2004]. Equation for threshold voltage (V_{TH}) can be written as:

$$V_{TH} = \phi_{ms} \pm 2\phi_F \pm \frac{\sqrt{2\varepsilon_0\varepsilon_s q N_s(2\phi_F + |V_{SB}|)}}{C_{ox}}, \tag{3.7}$$

where $+$ and $-$ denote n-channel and p-channel devices, respectively. N_s is the doping concentration of the substrate. ε_s is the dielectric constant of silicon, q is the charge of the electron, C_{ox} is the oxide capacitor per unit area, V_{SB} is the substrate bias voltage, and ϕ_{ms} is the metal-semiconductor work function.

$$\phi_{ms} = -\left(\frac{k_B T}{q}\right)\ln\left(\frac{N_G N_S}{n_i^2}\right), \tag{3.8}$$

where $n_i = KT^{3/2}\exp\left(-\frac{E_{g_0}}{2k_B T}\right)$ is the intrinsic carrier concentration and $\phi_F = \left(\frac{k_B T}{q}\right)\ln\left(\frac{N_s}{n_i}\right)$ is the Fermi potential. N_G is the doping level of poly-silicon gate, T is temperature in Kelvin, E_{g_0} is energy band gap at $T = 0$, k_B is Boltzmann constant, and K is a constant.

The value of the threshold voltage decreases almost linearly with temperature [Tsividis, 2004]. Therefore, its simplified expression can be approximated as:

$$V_{TH}(T) = V_{TH}(T_0) - k_{th}(T - T_0), \tag{3.9}$$

where k^{th} is a constant between 0.5 mV/K and 3 mV/K. The dependence of transconductance parameter ($\boldsymbol{\beta_p}$, and $\boldsymbol{\beta_n}$) can be seen through the temperature dependence of mobility of the charge carrier (μ_p and μ_n). The generalised expression for mobility (μ) at any temperature T can be written as:

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-k_\beta}, \tag{3.10}$$

where T_0 is the room absolute temperature, and k_β is a constant between 0.8 and 2.0. The expression for transconductance parameters ($\boldsymbol{\beta_p}$, and $\boldsymbol{\beta_n}$), respectively for nMOS and pMOS are as:

$$\boldsymbol{\beta_p}(T) = \mu_p(T) C_{ox} \left(\frac{\boldsymbol{W}}{L}\right)_p, \tag{3.11}$$

$$\boldsymbol{\beta_n}(T) = \mu_n(T) C_{ox} \left(\frac{\boldsymbol{W}}{L}\right)_n. \tag{3.12}$$

Further, the expressions of $\boldsymbol{\beta_p}$ and $\boldsymbol{\beta_n}$ can be written as:

$$\boldsymbol{\beta_p}(T) = \mu_p(T_0) \left(\frac{T}{T_0}\right)^{-k_{\beta_p}} C_{ox} \left(\frac{\boldsymbol{W}}{L}\right)_p, \tag{3.13}$$

$$\boldsymbol{\beta_n}(T) = \mu_n(T_0) \left(\frac{T}{T_0}\right)^{-k_{\beta_n}} C_{ox} \left(\frac{\boldsymbol{W}}{L}\right)_n. \tag{3.14}$$

3.2.3 Modeling of Jitter

For a fast-rising input signal, the transistor M_p operates in cutoff mode at the mid-point of the output response (i.e., at $V_{DD}/2$ level). Therefore, the effect of PSN does not directly appear in the output response of this region (i.e., Region-IV). However, its effect propagates from Region-I to all the successive regions through the random variables ($\boldsymbol{V_{12}}$, $\boldsymbol{V_{23}}$, and $\boldsymbol{V_{34}}$). These random variables are used to establish the continuity between {Region-I & Region-II}, {Region-II & Region-III}, and {Region-III & Region-IV}, respectively (Appendix A). The output response of Region-IV linearly varies with time, and it can be seen from (3.4); the intercept of this curve at $V_{DD}/2$ shift due to variation in $\boldsymbol{V_{34}}$ depending on noise and the random variables $\boldsymbol{W_n}$ and $\boldsymbol{W_p}$. This shift in the midpoint of the transition edges of the output response from its ideal position results in jitter at the output. The entire derivation is done by considering a constant value of phase ϕ_{s_n} for the nth sinusoid of the multi-tone noise, assuming an initial phase of the noise equal to $\phi_{s_{n_0}}$ for the ideal transition edge of the output signal. Its value varies for every transition edge of the input depending on the time period (T_d). The phase constant for j^{th} transition edge can be written as:

$$\phi_{s_{n_j}} = \phi_{s_{n_0}} + \omega_s T_d (j-1), \tag{3.15}$$

where T_d is the time period of the input. The output expression (3.4) of Region-IV with respect to j^{th} transition edge can be written as:

$$\boldsymbol{V_{out}(t,j)} = \boldsymbol{V_{34_j}} - 0.5 \cdot \boldsymbol{\gamma_3} (V_{DD} - V_{TN})^2 (t - T_3). \tag{3.16}$$

Since (3.16) is a linear equation, the intercept of $\boldsymbol{V_{out}(t,j)}$ at $V_{DD}/2$ determines the time stamp for j^{th} transition edge:

$$\boldsymbol{t_j} = \frac{\boldsymbol{2V_{34_j}} - V_{DD}}{\boldsymbol{\gamma_3}(V_{DD} - V_{TN})^2} + T_3. \tag{3.17}$$

The deviation of jth transition edge from its ideal time stamp T_0 (i.e., when $v_s(t) = 0$ and the typical values of the design variables are taken) determines **TIE** as:

$$\mathbf{TIE_j} = \boldsymbol{t_j} - T_0, \tag{3.18}$$

where t_j is the time stamp for j^{th} transition edge. The peak-to-peak deviation determines jitter at the output as:

$$\textbf{Jitter} = max(\textbf{TIE}_j) - min(\textbf{TIE}_j). \tag{3.19}$$

The terms V_{34}, and γ_3 carry the information of stochastic parameters and temperature.

3.3 Results and Discussion

This section presents a detailed discussion and validation of the proposed work, considering several examples (simulation, analytical, and measurement). The simulation results are obtained using the SPICE-based simulator, analytical results are obtained using the computational tool, and the measurement results are obtained using experimental setup. To estimate jitter at the output of inverter, 100 bits simulation is done. Section-3.3.1 presents a comparative analysis of simulation and analytical results considering different technology nodes. Section 3.3.2 presents a couple of measurement examples to validate the proposed work. The results presented in both the sections signify the impact of variability on power supply-induced jitter.

3.3.1 Simulation Results

Example-1:

In this example, a CMOS inverter is designed at 40nm technology node of UMC. An input data having data rate of 1.25 Gbps is considered, and a load capacitance of 10 fF is connected at the output. Figure 3.3.1, Figure 3.3.2, and Figure 3.3.3 depict the appended plots, where all the falling transition edges of the output signal are appended, considering three different cases. The dark blue line in these plots represents the ideal transition edge.

Case-A: In this case, the analysis is done considering only the effect of noise, and the variations in design parameters of the transistors are ignored. A small-signal sinusoidal noise source having an amplitude of 40 mV and frequency of 533 MHz is inserted at supply terminal of the inverter. A significant shift in each transition edge of the output from its ideal position can be seen in Figure 3.3.1(a) and Figure 3.3.1(b). Both figures depict the appended output plots obtained from analytical and simulation approaches, respectively. From these figures, it can be seen that both results are quite similar, and the respective jitter values for analytical and SPICE simulations without considering the effect of variability are 13.32 psec and 12.14 psec, respectively.

Case-B: In this case, the analysis is done only considering the effect of variability and the effect of PSN has been ignored. The width of the transistors (W_p and W_n) are design parameters that are subjected to random variations due to manufacturing inaccuracies, and these parameters are considered as random variables. 500 samples of each of the random variables are taken. Figure 3.3.2(a) and Figure 3.3.2(b) are the appended output plots obtained using the proposed approach and SPICE-based simulator, respectively. The deviation of the output transition edges from the ideal position is estimated at the midpoint (i.e., $V_{DD}/2$), and these deviations are 10 psec and 9.16 psec, respectively, for the proposed and SPICE simulations.

Case-C: In this case, the analysis is done by considering the effect of variability as well as the PSN together. A small-signal sinusoidal noise having an amplitude of 40 mV and frequency of 533 MHz is applied at the supply terminal of the inverter, and widths of the transistors W_p and W_n are considered as random variables. 500 samples of each random variable are taken. The appended output plots from the proposed and simulation approaches are shown in Figure 3.3.3(a)

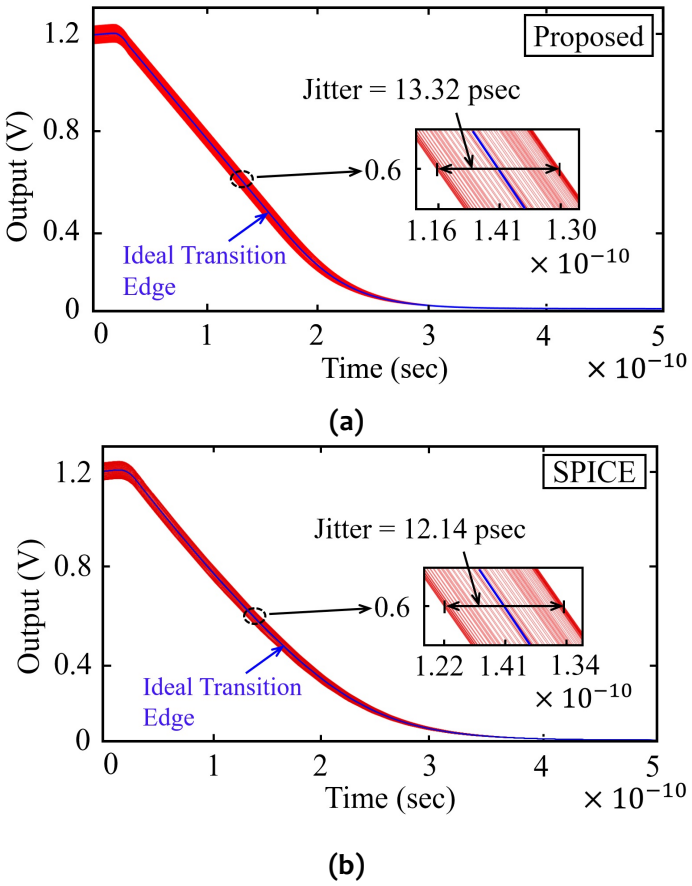


Figure 3.3.1: Appended output plots of CMOS inverter with only PSN in the circuit (a) proposed result and (b) SPICE-based simulation result.

and Figure 3.3.3(b), respectively. The estimated jitter values from both approaches are 22.40 psec and 21.09 psec, respectively.

It can be clearly seen that the value of jitter significantly increases when the effects of variability and PSN both are considered together.

Example-2:

In this example, the effect of temperature is investigated along with the noise. A CMOS inverter has been designed in 180 nm technology node of UMC. A DC power supply of 1.8 V is used, and a capacitor of 1 pF is used as a load. A data rate of 480 Mbps is applied at the input terminal of the inverter. Figure 3.3.4(a) depicts the falling edge of the output plots obtained at different temperatures. Further, three different cases are considered to study the effect of temperature and variability issues on power supply-induced jitter.

Case-A: In this case, only power supply noise is considered. A power supply noise with an amplitude of 30 mV and frequency of 409 MHz is applied at the supply terminal of the inverter, and the temperature is varied from -30 °C to 80 °C, and the corresponding jitter values are estimated at the output of the inverter. Figure 3.3.4(b) shows the estimated jitter using proposed and SPICE-based approaches.

Case-B: In this case, only the effect of variability is considered, and the PSN source has been

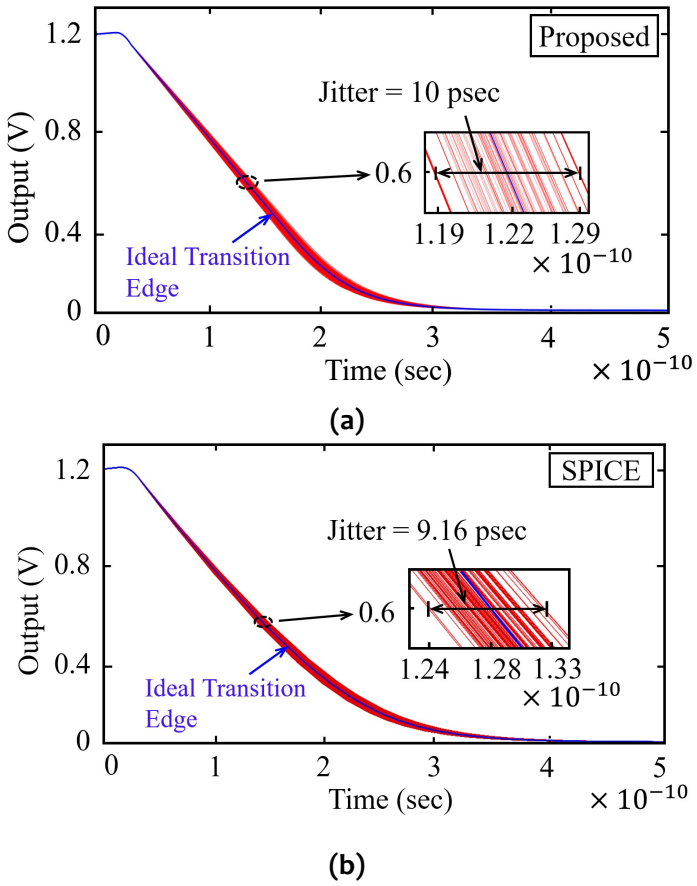


Figure 3.3.2: Appended output plots of CMOS inverter only considering variability issue in the circuit (a) proposed result and (b) SPICE result.

removed. The widths of the transistors (W_p and W_n) are considered as random variables and are subjected to random variations of $\pm 5\%$ ($\pm 3\sigma$). The simulations has been carried out by varying the temperature from -30 °C to 80 °C and corresponding jitter values are estimated as shown in Figure 3.3.4(b).

Case-C: In this case, power supply noise and variability issues both are considered together. The widths of the transistors (W_p and W_n) are considered as random variables and are subjected to random variations of $\pm 5\%$ ($\pm 3\sigma$). A power supply noise with an amplitude of 30 mV and frequency of 409 MHz is applied at supply terminal of the inverter. The estimated jitter from proposed and SPICE-based approaches are plotted with respect to temperature as shown in Figure 3.3.4(b). A significant amount of variation in jitter is observed with the corresponding increase in temperature.

In this experiment, since all other parameters such as substrate doping concentration (N_A), oxide thickness (t_{ox}), fermi-potential (ϕ_F), intrinsic carrier concentration of the semiconductor and doping level of poly-silicon gate (N_G) are the inherent parameters of the process design kit (PDK) file provided by foundry, these parameters are not accessible to the users. Therefore in this experiment, the parameters (V_{TN}, V_{TP}, β_n and β_p) are extracted with the help of simulation using (3.9) and (3.13), and are given in Table 3.3.1. The values of threshold voltages (V_{TN} and $|V_{TP}|$) decrease linearly with the temperature. Here, the value of constant k_{th} is 0.849 mV/K and -0.957 mV/K for nMOS and pMOS, respectively. The constant term k_{β_n} is 1.53 and k_{β_p} is 0.95, respectively, for

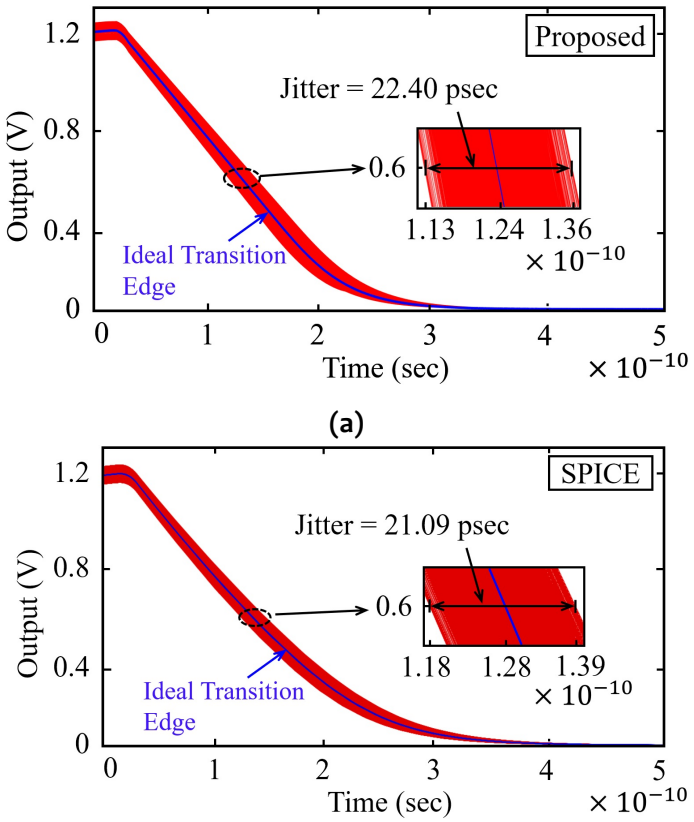


Figure 3.3.3: Appended output plots of CMOS inverter considering PSN and variability together in the circuit (a) proposed result and (b) SPICE result.

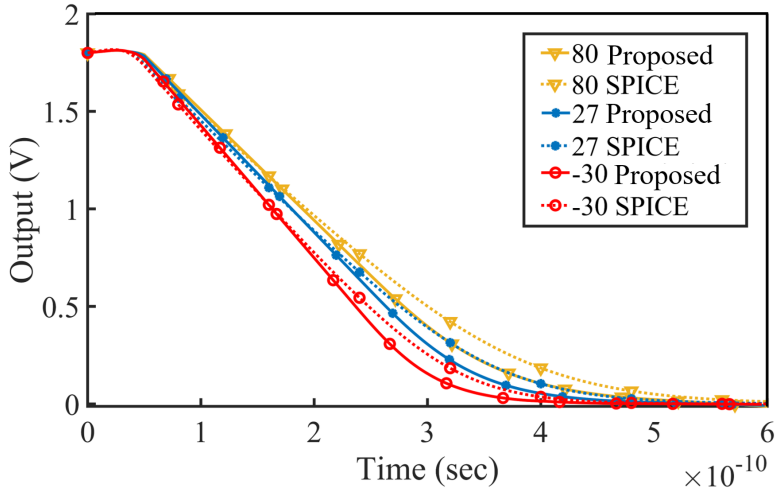
nMOS and pMOS transistors.

Table 3.3.1: Temperature dependent device parameters.

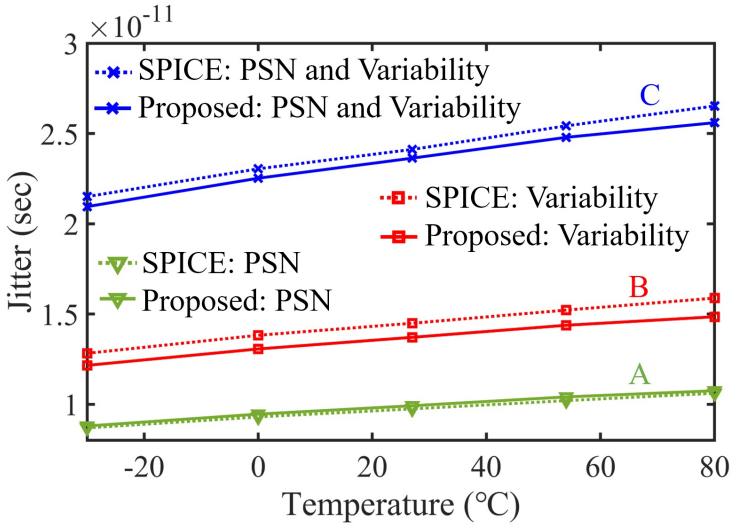
Temperature (°C)	V_{TN} (mV)	V_{TP} (mV)	β_n (mA/V^2)	β_p (mA/V^2)
−30	569.63	−552.983	21.7483	19.7236
0	544.14	−524.266	18.232	17.6841
27	521.19	−498.42	15.7616	16.1911
54	498.25	−472.574	13.7651	14.951
80	476.15	−447.685	12.1808	13.9493

Example-3:

In this example, the inverter circuit is designed in 180 nm technology node of UMC. A DC power supply of 1.8 V is used, and a load capacitor of 1 pF is used. An input data of 480 Mbps is applied. The distribution of jitter is shown with respect to random variations in the widths of the transistors (W_p and W_n). For this, a sinusoidal noise source with a frequency of 533 MHz and a peak-to-peak amplitude of 40 mV is inserted at supply terminal of the inverter. A probability density function (pdf) plot of jitter is shown in Figure 3.3.5, taking 900 samples of the random variables. The mean



(a)



(b)

Figure 3.3.4: (a) Output plots of CMOS inverter at different temperatures, (b) Variation in jitter with respect to temperature variation.

and standard deviation of jitter are {14.25 psec and 0.318 psec} and {13.20 psec and 0.299 psec}, respectively, for the results obtained from the proposed approach and SPICE-based simulator.

3.3.2 Measurement Setup and Results

The experimental setup is prepared to analyze and compare the variation in the output response of different inverters of the same vendor. For this, two function generators (Aplab DDS300 300 MHz dual channel and Tektronix AFG3021B 25 MHz single channel), one Oscilloscope (MSOX4054A 500 MHz 5 GSa/s), one Regulated DC Source (EDU36311A, triple output power supply) from Keysight, one breadboard, and some connecting probes are used. To perform the experiment, a 5 V DC power supply is used at V_{DD} terminal of inverter IC and a square wave having frequency of 1.5 MHz is applied at input terminal. A load capacitor of 100 pF is connected to the output. The

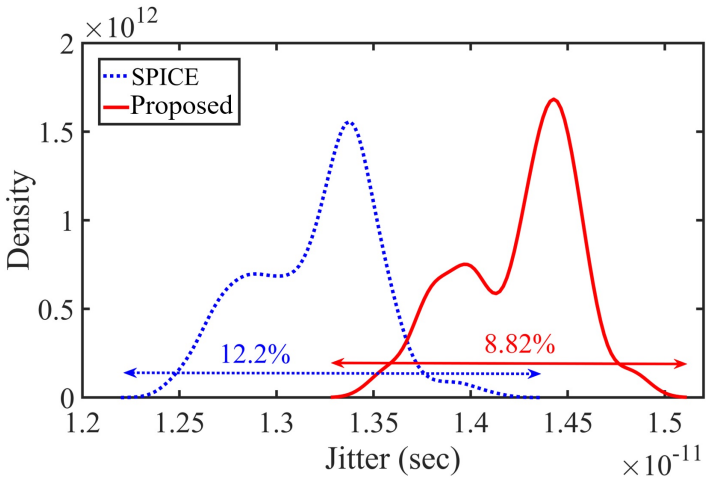


Figure 3.3.5: Probability density function (pdf) of jitter, considering PSN and variability.

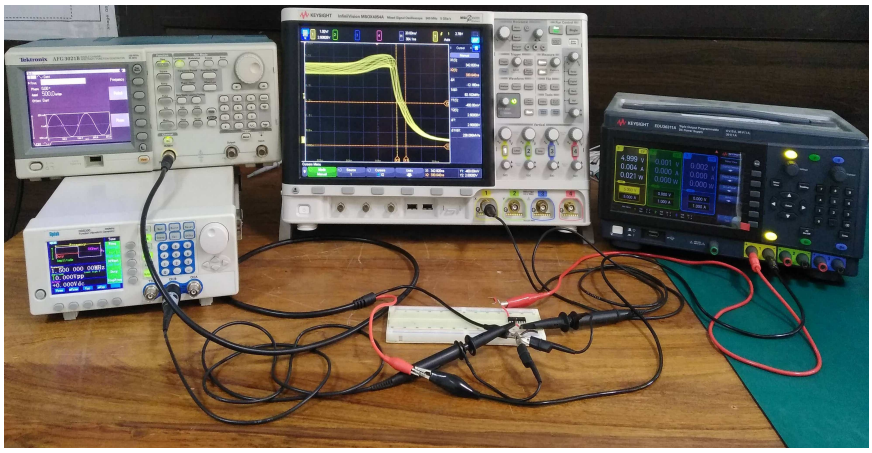
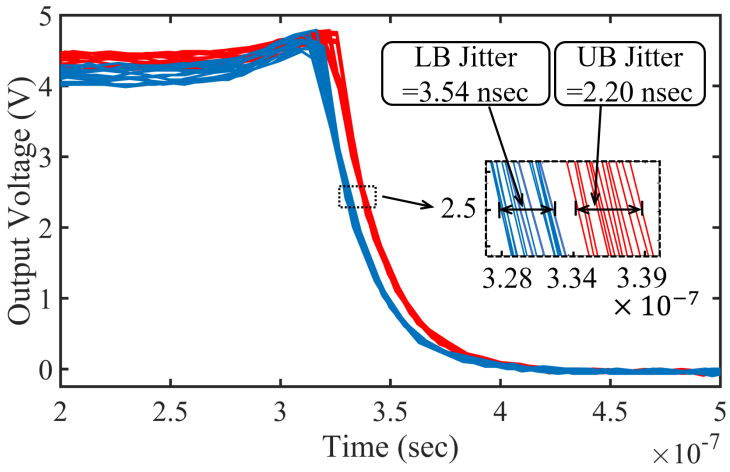


Figure 3.3.6: Experimental setup depicting power supply noise in the circuit.

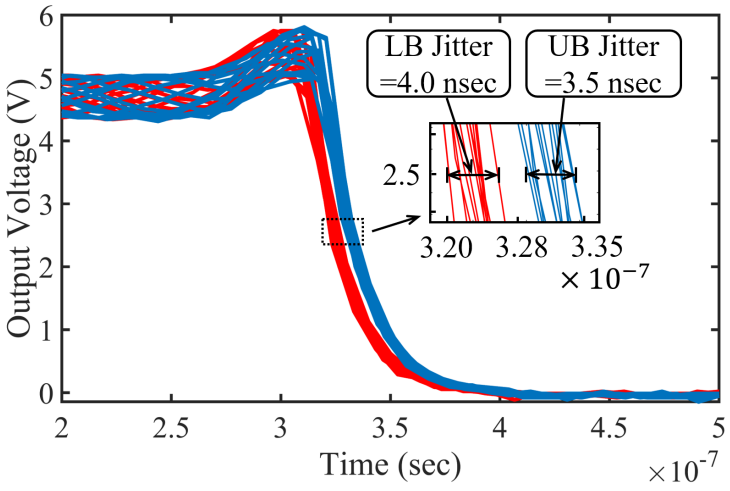
experimental setup is shown in Figure 3.3.6.

Example-4:

In this example, two case studies have been performed considering two different hex inverter ICs (M74HC04 and SN74HC04). The upper and lower bounds (UBs and LBs) are identified from the output responses obtained using both ICs as shown in Figure 3.1.1. In both the cases, a power supply noise with an amplitude of 500 mV and frequency of 5.733 MHz is connected along with the DC power supply. Then, the obtained UB and LB output responses are appended as shown in Figure 3.3.7(a) and Figure 3.3.7(b), for Case-A and Case-B, respectively. The power supply-induced jitter value for each upper and lower bound is estimated. For Case-A, jitter in lower and upper bounds are 3.54 nsec and 2.20 nsec, respectively, and the total timing deviation is 10.20 nsec, as shown in Figure 3.3.7(a). For Case-B, jitter in lower and upper bounds are 4.0 nsec and 3.5 nsec, respectively, and the total timing deviation is 12.80 nsec, as shown in Figure 3.3.7(b). In both the cases, significant amount of variations can be observed.



(a)



(b)

Figure 3.3.7: Jitter in the lower bound (LB) and upper bound (UB) output responses of the inverter samples in the presence of PSN for: (a) M74HC04 and (b) SN74HC04.

3.4 Application Case Study

With respect to the analysis discussed so far, an application case study is presented in this section to demonstrate how the performance of a system gets affected due to power supply noise, along with variability issues. Here, a chain of 10 CMOS inverters is designed at 180 nm UMC technology node, and a load capacitor of 70 fF is connected at the output terminal of the last stage. An input data having data rate of 240 Mbps is applied. The schematic of the chain of CMOS inverters is shown in Figure 3.4.1 [Illikkal *et al.*, 2022]. A power supply noise with an amplitude of 30 mV and frequency of 133 MHz is inserted at supply terminal of the inverter chain. The widths of the transistors (W_p and W_n) are taken as random variables and are subjected to random variation of ±5%. The estimation of jitter is done at the output of every stage with and without considering the effect of variability. The maximum difference of 8.73% between lower and upper jitter values is observed. Figure 3.4.2 depicts the variation in jitter. From the figure, it can be observed that

if there are variability issues in the circuit, its performance can degrade. This clearly shows the significance of variability-aware modeling of jitter.

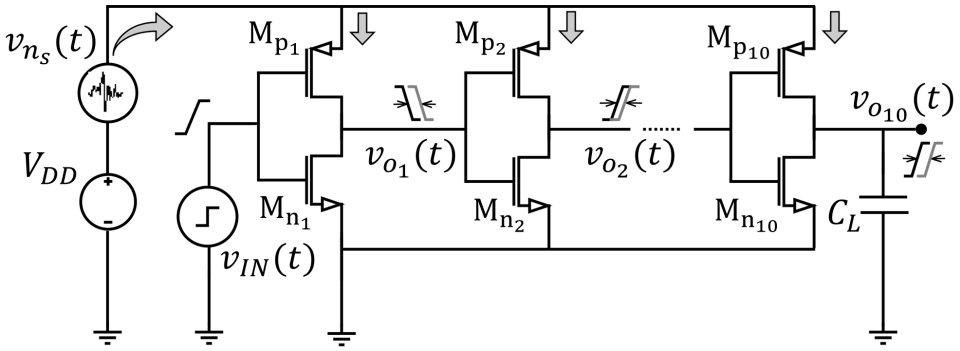


Figure 3.4.1: A chain of CMOS Inverters.

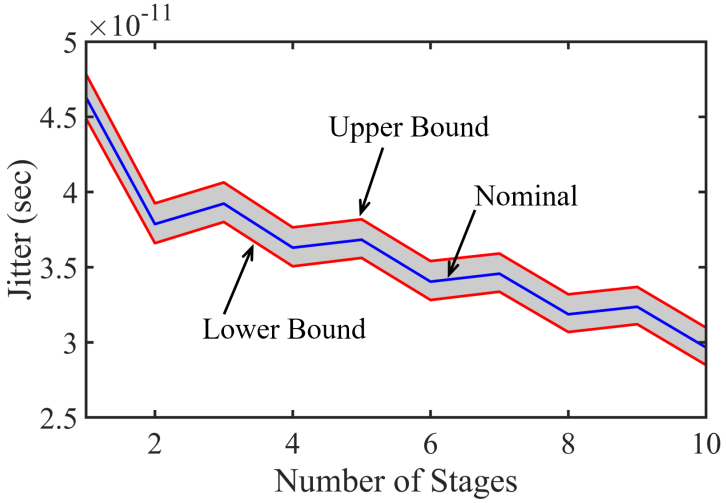


Figure 3.4.2: Variation in jitter at the output of different stages of a Chain of CMOS Inverters.

3.5 Summary

The work presented in this chapter introduces a new perspective on accounting timing uncertainties in high-speed VLSI circuit design. Taking CMOS inverter as a case study, the effect of variations in design parameters on power supply-induced jitter has been discussed thoroughly. Several examples (simulation and measurement) have been presented to validate the importance of this work. The results suggest that in order to achieve a robust design and maintain the timing budget of the overall system, variability-aware modeling of power supply-induced jitter in ICs is essential during various design stages. Thus, variability-aware modeling of jitter can be an important strategy for VLSI designers. It will help the designers to improve the performance of their design and meet the required specifications.