3

Single Pole Double Through(SPDT) Switching Circuit

3.1 INTRODUCTION

A single-pole double-throw (SPDT) switch plays an important role in the RF transceiver, which helps to direct a common input signal into two individual output streams at different time instant. Generally, a SPDT switch is dominantly used for TDD operation. The SPDT switch is followed by a duplexer as shown in Figure 3.1, where the series SPDT switch configuration is operated at 2.4 GHz [Misran *et al.*, 2012]. Many circuit designer have adopted conventional PCB design process for the implementation of SPDT switch at L, S, X and Ka bands [Hansen *et al.*, 2016],[Rave *et al.*, 2014b],[Shairi *et al.*, 2011b],[Shairi *et al.*, 2011a][Chen *et al.*, 2016],[Lim and Lim, 2014],[Jang *et al.*, 2018]. However, the conventional PCB fabrication approach is rarely employed in millimeter-wave applications due to the significant radiation loss and undesirable surface wave loss produced by the varied dimensions of a microstrip line . With the development of the modern 5G wireless communication system, the designated millimeter wave frequency bands should support the TDD scheme, and hence a new millimeter wave SPDT switch circuit is needed. The main challenge of designing such a circuit involves maintaining good isolation between two output ports while maintaining low insertion loss and good impedance matching in the desired path. Designing a millimeter-wave SPDT switch circuit at high frequencies requires additional considerations about PCB material and transmission line theory. As elaborated in Chapter 1, the Substrate Integrated Coaxial Line (SICL) presents substantial benefits for high-frequency applications, positioning it as a highly advantageous choice in millimeter-wave (mmWave) circuit

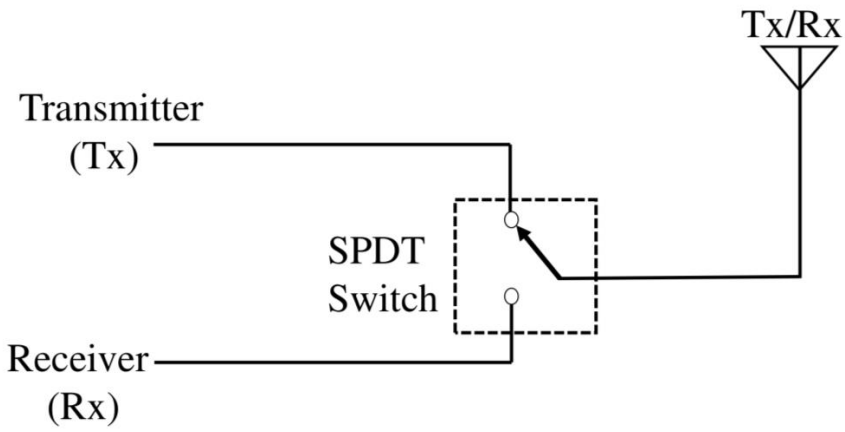


Figure 3.1 : Conventional SPDT Switch in RF transceiver system

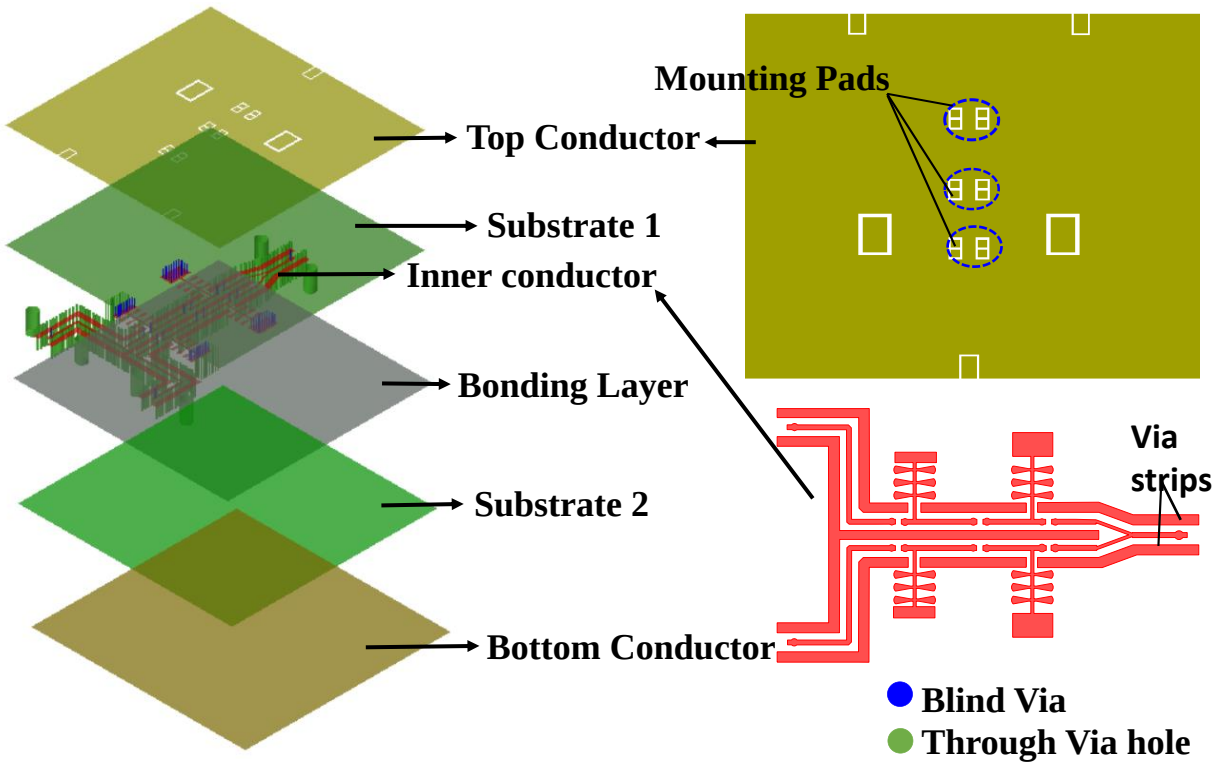


Figure 3.2 : 3-D view of the SICL based SPDT switch.

designs [Gatti *et al.*, 2006],Krishna and Mukherjee [2018b],Mukherjee [2017],Shukla and Mukherjee [2019],Shukla and Mukherjee [2024a].

In this chapter, the SICL based SPDT switch circuit adopts a low-cost PCB design technique at 27-28.5 GHz as shown in Figure 3.2. The network comprises of SPDT switching circuit using a series of butterfly stubs and mounting pads for the integration of diodes and capacitors which was introduced in [Shukla and Mukherjee, 2023]. However, the placement of the butterfly stubs at the middle layer eliminates the possibility of spurious radiation as it is shielded by the top and bottom copper plates in asymmetric stripline environment and increases the isolation between RF and DC paths. The sidewall ensures good shielding of the main RF line channels, which helps to improve the impedance matching between Tx to Tx/Rx and Rx to Tx/Rx channel. A single-layer ceramic capacitors (DC blocks) are mounted on the top layer of the SICL in the path of Tx to Tx/Rx and Rx to Tx/Rx.

The explanation of design procedure for the SPDT switch is shown in Section 3.2. The results and discussion of the circuit are presented in Section 3.3

3.2 DESIGN PROCEDURE OF PROPOSED SPDT SWITCH

In this chapter, two 0.25 mm thick Taconic TLY-5(ε_r=2.2, tanδ = 0.0009) based substrate along with bond layer Taconic FR-28 prepreg (ε_r = 2.8, tanδ = 0.0014) is used to realize the proposed design. The proposed circuit introduces an RF isolation network which are used to

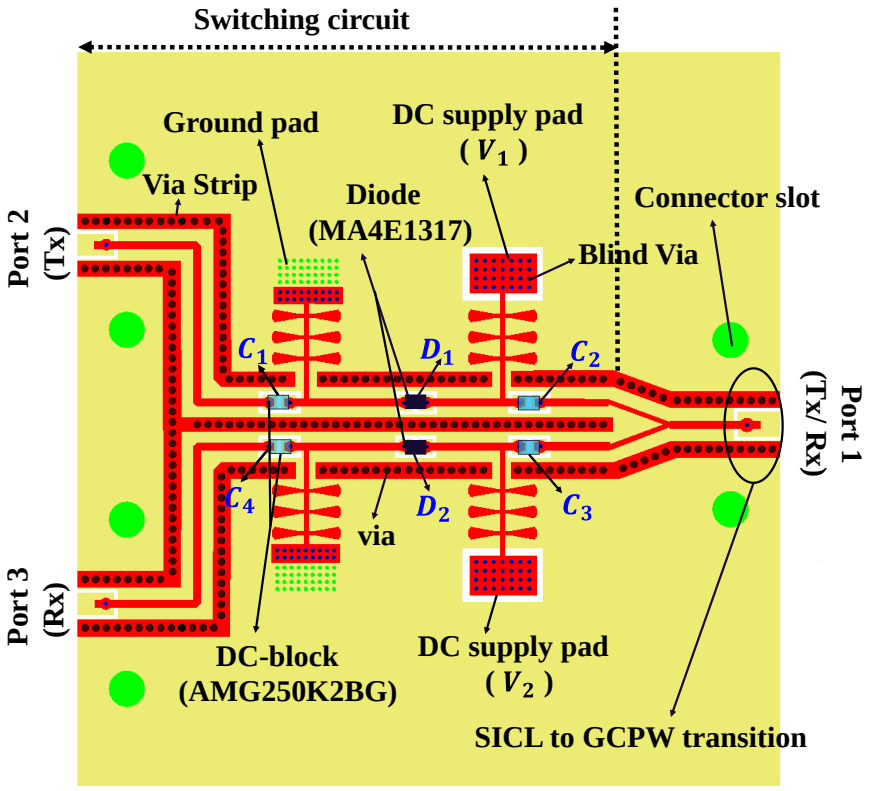


Figure 3.3 : Physical structure of the SPDT switch circuit.

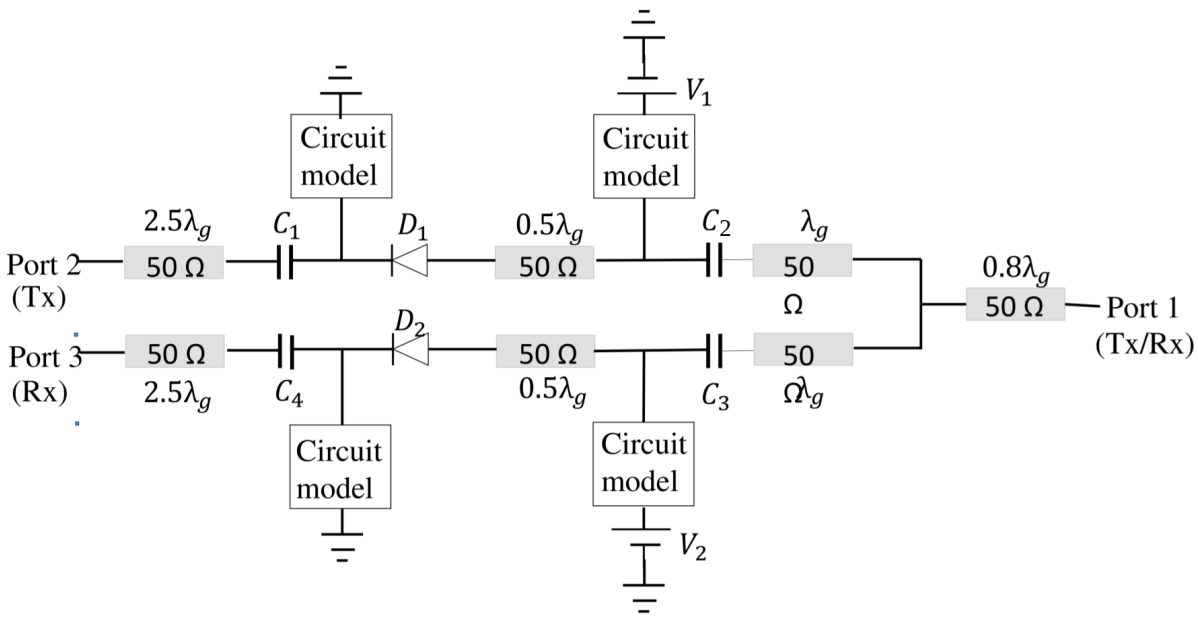


Figure 3.4 : Proposed equivalent circuit of SPDT Switch

activate the RF switches in the corresponding channels (Tx and Rx) by the DC supply. The physical layout and equivalent circuit of the SPDT circuit are shown in Figure 3.3 and Figure 3.4, respectively.

3.2.1 Design of RF isolation network for DC supply

Figures 3.5(a) and 3.5(b) show the physical layout and stack up of the substrate for the proposed isolation circuit where a series of three butterfly stubs are used for the high isolation in the middle layer of the substrate, which is separated from the top and bottom ground plate as an asymmetric stripline structure [Shukla and Mukherjee, 2023]. The characteristic impedance of the asymmetric stripline ($Z_{0,AS}$) depends on the ratio of the conductor width and distance between the signal and ground planes. The characteristics impedance ($Z_{0,AS}$) can be calculated as follows by Eq.(3.1) Wadell [1991].

$$Z_{0,AS} = \frac{1}{\sqrt{\varepsilon_r}} [Z_{0,SS}(\varepsilon_r = 1, H = h_1 + h_2 + t) - \triangle Z_{0,air}] \tag{3.1}$$

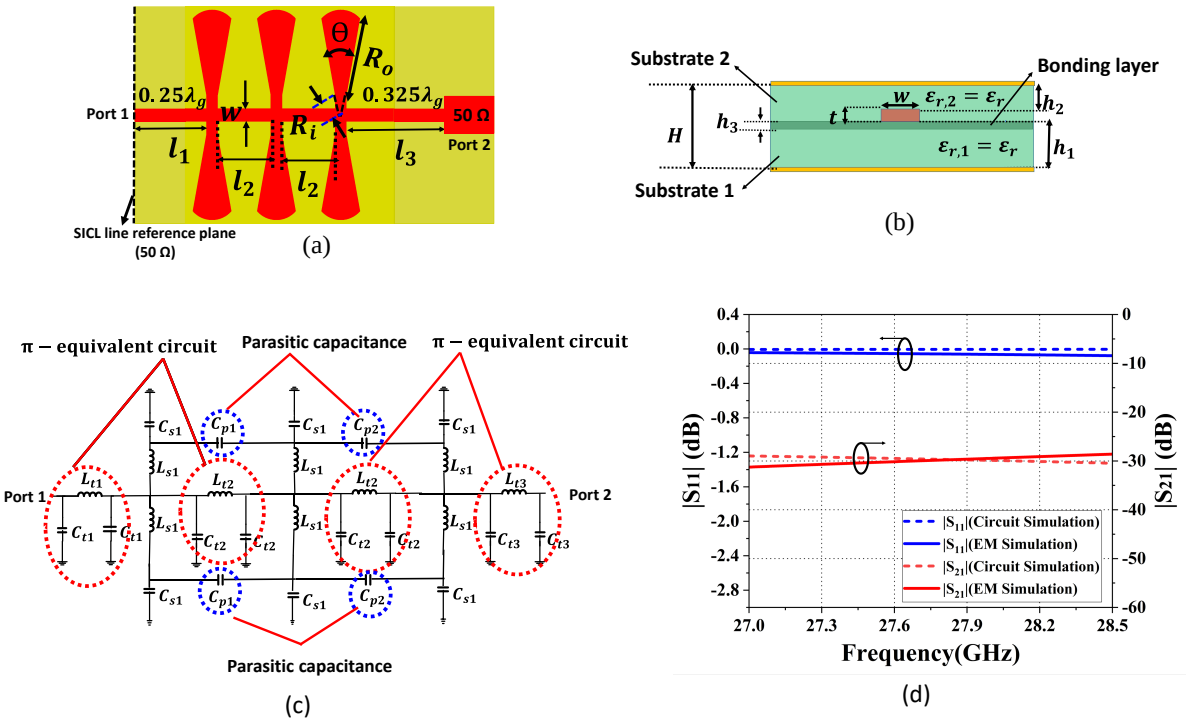


Figure 3.5 : Physical layout of a series butterfly stubs with the dimension $R_i = 0.16$ mm, $R_o = 1.9$ mm, $\theta = 23^o$,$w = 0.24$ mm;(a) Top View; (b) Substrate stackup of the proposed design where $h_1 = 0.354$ mm,$h_2 = 0.254$ mm,and $h_3 = 0.1$ mm. (c) The proposed equivalent circuit model of the series butterfly stubs with lossless central transmission lines; (d) Response of EM and circuit simulation of the series butterfly stubs with lossless central transmission lines from optimized values of $L_{t1} = 0.38$ nH, $C_{t1} = 0.0856$ pF, $L_{t2} = 0.289$ nH, $C_{t2} = 0.0373$ pF, $C_{s1} = 0.064$ pF, $L_{s1} = 0.54$ nH, $C_{t3} = 0.14$ $L_{t3} = 0.5$ nH, $C_{p1} = 0.0133$ pF, $C_{p2} = 0.0133$ pF.

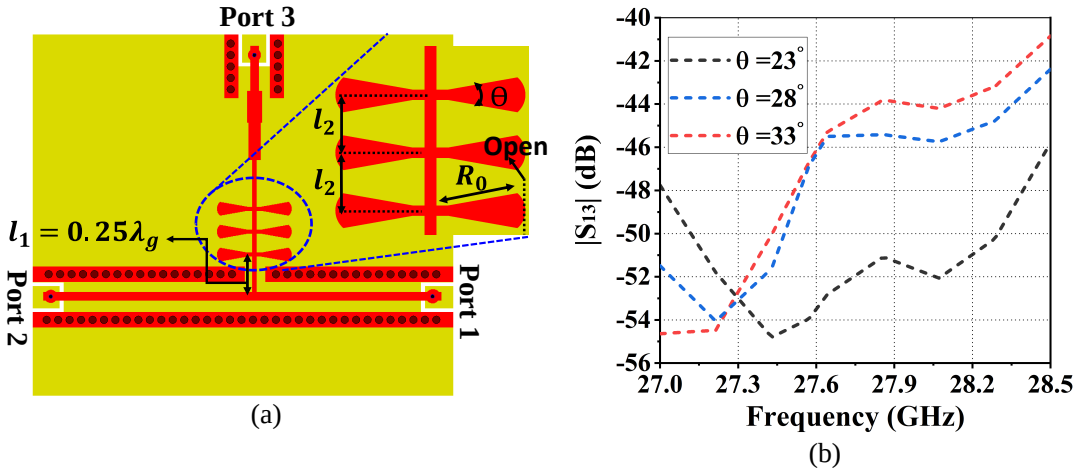


Figure 3.6 : (a) Physical layout of the RF isolation network (including three butterfly stubs) with SICL line; (b) Response of isolation between Port 1 and 3 with the variation of spanning angle (θ)

where, $Z_{0,SS}(\varepsilon_r = 1,\ H = h_1+h_2+t)$ is the characteristics impedance of symmetric stripline. The value of $Z_{0,SS}$ is derived from Eqs.(3.2) and (3.3), with air as the dielectric and having total thickness($H = h_1+h_2+t$);

$$Z_{0,SS} = \frac{\eta_0}{2\pi\sqrt{\varepsilon_r}} \ln\left\{1+\frac{4H}{\pi w'}\left[\frac{8H}{\pi w'}+\sqrt{\left(\frac{8H}{\pi w'}\right)^2+6.27}\right]\right\} \tag{3.2}$$

where

$$w' = w+\frac{t}{\pi}\ln\left\{\frac{e}{\sqrt{\left(\frac{t}{2H+t}\right)^2+\left(\frac{\pi t}{4(w+1.1t)}\right)^m}}\right\} \tag{3.3}$$

$$m = \frac{6H}{3H+2t} \tag{3.4}$$

and

$$\triangle Z_{0,air} = 0.0325\pi Z_{0,air}^2\left(0.5-\frac{1}{2}\frac{2h_1+t}{h_1+h_2+t}\right)^{2.2}\times n \tag{3.5}$$

$$n = \left(\frac{t+w}{h_1+h_2+t}\right)^{2.9} \tag{3.6}$$

where, h_1 is the distance between the signal line and the lower reference plane, h_2 is the distance between the signal line and the upper reference plane, and $Z_{0,air}$ is represented by Eq.(3.7)

$$Z_{0,air} = 2\left[\frac{Z_{0,SS}(\varepsilon_r=1,H=h_1)Z_{0,SS}(\varepsilon_r=1,H=h_2)}{Z_{0,SS}(\varepsilon_r=1,H=h_1)+Z_{0,SS}(\varepsilon_r=1,H=h_2)}\right] \tag{3.7}$$

where, $Z_{0,SS}(\varepsilon_r = 1, H = h_1)$ is the characterstic impedance of symmetric stripline as shown in Eq.(3.2) with air as the dielectric and having total thickness of the line equal to h_1 and $Z_{0,SS}(\varepsilon_r = 1, H = h_2)$ is the characteristic impedance of symmetric stripline with air as the dielectric and total thickness of the line equal to h_2.

The series of butterfly stubs are connected with a lossless central transmission line sections. The equivalent circuit parameters of the bias line are obtained with the help of the telegrapher's equation parameters as described in [Hong and Lancaster, 2004]. A high-impedance lossless line terminated at both ends by relatively low-impedance lines can be presented by a π-equivalent circuit, as shown in Figure 3.5(c). Also, the small section of high impedance line with radial stub at both ends introduces discontinuity at the junction which is represented by another π circuit. The values of L_t and C_t can be obtained from Eqs.(3.8) and (3.9).

$$L_t = \frac{1}{2\pi f_1} \times Z_{0,AS} \times \sin\left(\frac{2\pi l}{\lambda_g}\right) \tag{3.8}$$

$$C_t = \frac{1}{2\pi f_1} \times \frac{1}{Z_{0,AS}} \tan\left(\frac{\pi l}{\lambda_g}\right) \tag{3.9}$$

$$L_s = \frac{120\pi H(2.8 - 10\frac{R_i}{R_o})}{c\theta} \tag{3.10}$$

$$C_s = \frac{\theta R_o^2 \varepsilon_r}{240\pi H c} \tag{3.11}$$

The next Eqs (3.10-3.11) are obtained from [Kwon *et al.*, 2007] where, f_1 is the center frequency of the operating band, H is the total substrate height in mm, R_i is the inner radius, and R_o is the outer radius of the butterfly stub, c is the speed of light, θ is the spanning angle in radian. Using the design Eqs (3.8), (3.9), (3.10) and (3.11) with considering the parasitic capacitance effects (C_{p1}, C_{p2}) between the radial stubs, the equivalent circuit is proposed in the operating frequency of 27-28.5 GHz. With the help of known parameters such as R_o, R_i, and spanning angle θ, the initial values of L_s and C_s can be calculated. Further, the circuit is tuned slightly to have better agreement between EM and circuit simulation as shown in Figure 3.5(d). Next, the first butterfly stub is considered which is directly connected to the main RF line at the distance of l_1 and it's radial stub is an open circuit at the distance of R_0. The l_1 and R_0 are maintained to approximately odd multiple of $\lambda_g/4$, so that it behaves as open circuit for the main RF line [Fooks and Zakarevicius, 1990a],[Majidifar and Hayati, 2017]. Moreover, we added the other two butterfly stubs while maintaining the small gap of $l_2 = 1$ mm using the lossless line. Now, the series butterfly stubs are combined with the SICL line and the performance is shown in Figure 3.6(a). The isolation graph is observed ($|S_{13}|$), which varies with the spanning angle as shown in Figure 3.6(b). The optimized spanning angle is chosen, 23^0 for the proposed duplexer circuit.

3.2.2 I-V Characteristics and S-Parameter behaviour of the diode model (MA4E1317)

Figures 3.7(a), 3.7(b) and 3.7(c) show diode model and its large signal model. The diode model of MA4E1317 is selected for the proposed SPDT switch. Figures 3.8(a) and 3.8(b) show the I-V charcterstics of diode model MA4E1317 with the temperature variation at forward and reverse bias,

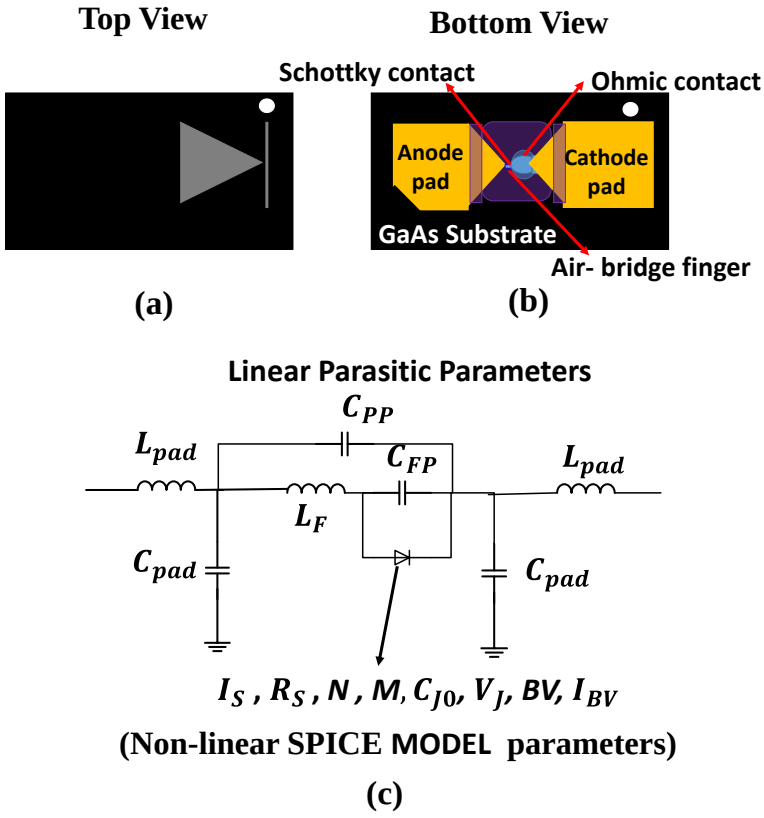


Figure 3.7 : (a) Top View of physical layout of MA4E1317; (b) Bottom View physical layout of MA4E1317; (c) Large signal equivalent circuit model of MA4E1317 (Schottky diode) with the parameters of $L_{pad} = 4.3$ pH, $C_{pad} = 4$ fF, $L_f = 0.28$ nH, $C_{PP} = 0.017$ pF, $C_{FP} = 0.016$ pF,$I_s = 0.12$ pA, $R_s = 3.15\Omega$, $N = 1.22$, $C_{jo} = 0.02$ pF, $M = 0.48$, $I_{BV} = 10$ uA, $V_j = 0.67$ V, $BV = 10$ V;

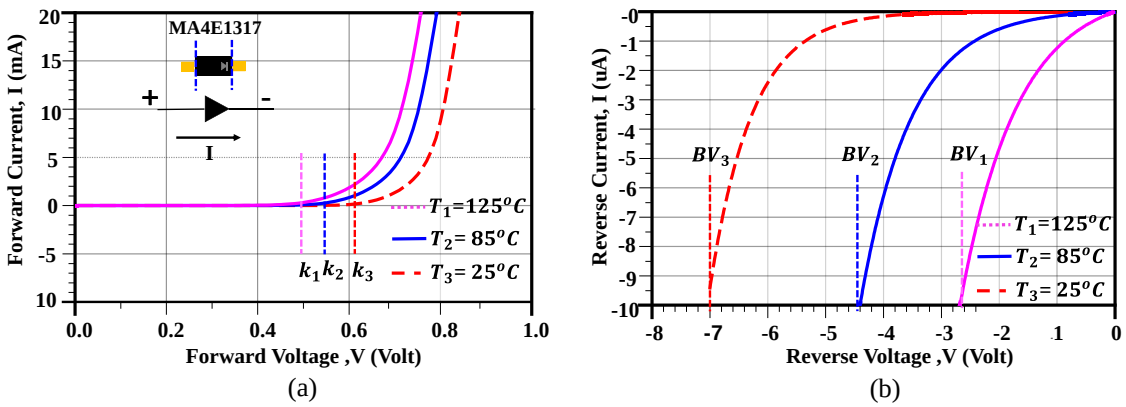


Figure 3.8 : (a) I-V characteristics of the diode (MA4E1317) in forward bias condition with different temperatures where $k_1 = 0.44$ V, $k_2 = 0.5$ V, $k_3 = 0.6$ V; (b)I-V characteristics of the diode in reverse bias condition with different temperatures where $BV_1 = 2.7$ V, $BV_2 = 4.4$ V, $BV_3 = 7$ V.

respectively. The physical model is composed of Schottky contact, Ohmic contact, Airbridge finger, Cathode and Anode contact pads and GaAs Substrate. The large signal equivalent circuit model is created by the fringing field between both pads, which is modeled as a pad-to-pad capacitance, C_{PP}. Next, Finger pad coupling is modeled as C_{FP}, self-inductance of Airbridge finger modeled as L_F, the contact pads are denoted as C_{pad} and L_{pad}. The diode Spice Model represents the Schottky junction, non-linear junction capacitance, and resistance [Chen *et al.*, 2020]. The effects of full parasitic with spice model is analyzed from the I-V characteristics in Keysight ADS software.

3.2.3 Working principle of SPDT switch as duplexer circuit

The SPDT switch as duplexer circuit consists of three port network device. It is operated with a diode ON and OFF state. In the duplexer circuit, when applying the DC bias condition such as forward voltage, $V_1 = 0.9$ V to diode D_1 and reverse voltage, $V_2 = -4$ V to diode D_2. The diode D_1 is ON state and D_2 is OFF state, respectively. The diode D_2 is placed at a distance of $2\lambda_g$ from the junction. As a result, the impedance seen from the junction towards Port 3 becomes infinity and the RF signal only passes from Port 1 to Port 2. Similarly, when the DC bias condition is reversed ($V_2 = 0.9$ V, $V_1 = -4$ V), the diode D_2 is ON, and D_1 is OFF state, respectively. In the reverse bias condition, Port 2 behaves as an open circuit which allows the transmission of RF signal from Port 1 to Port 3

3.3 RESULTS AND DISCUSSION

Figures 3.9(a) and 3.9(b) show the fabricated prototypes and responses of the SPDT circuit with the diodes (D_1 and D_1) model MA4E1317 [Chen *et al.*, 2020] and capacitors (C_1, C_2 ,C_3 and C_4). The proposed duplexer circuit has been developed with a SICL -to GCPW transition, which

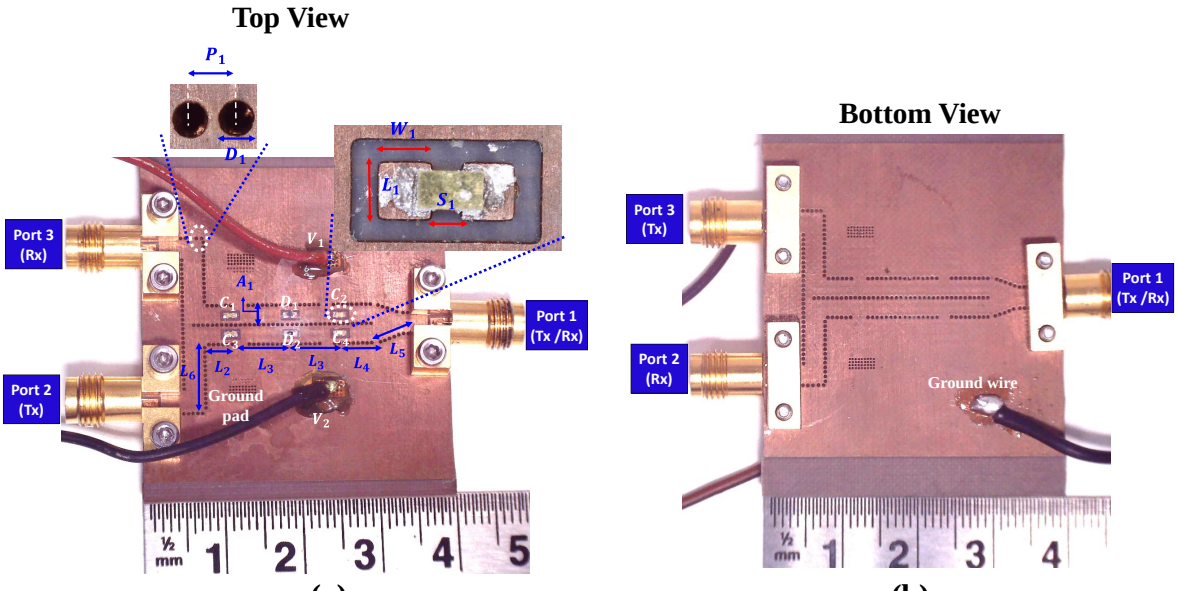


Figure 3.9 : Fabricated prototype of the SPDT switch as duplexer circuit with important dimensions, $L_1 = 0.85$mm, $L_2 = 2.7$mm, $L_3 = 5.2$mm,$L_4 = 3.9$mm,$L_5 = 3.4$mm,$L_6 = 8.4$mm,$P_1 = 0.62$mm, $D_1 = 0.42$mm,$S_1 = 0.28$mm,$A_1 = 1.7$mm, $W_1 = 0.82$mm (a) Top View;(b) Bottom View.

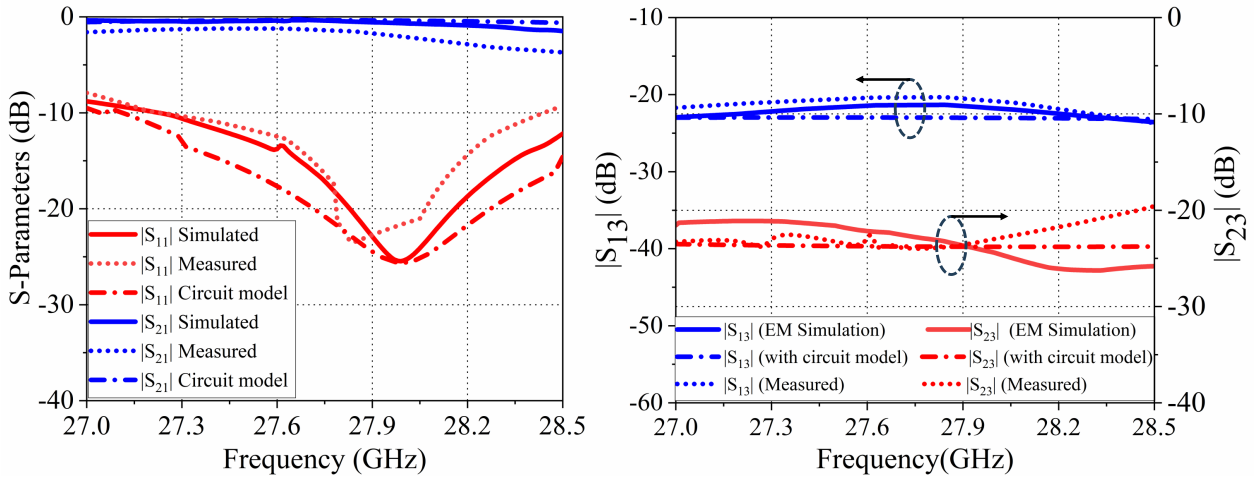


Figure 3.10 : (a) Performance of the SPDT switch circuit results in reflection coefficient ($|S_{11}|$) and insertion loss ($|S_{21}|$) from Tx/Rx to Tx channel, (b) Results of isolations ($|S_{13}|$) and ($|S_{23}|$) between Port 2(Tx)- 3 (Rx) and Port 1(Tx/Rx)-3(Rx) where $V_1 = 0.9$ V and $V_2 = -4$ V.

is applied on all ports for edge mount connector interfaces. Figures 3.10(a) and 3.10(b) present the simulated and measured results of the reflection coefficients, which is below -10 dB at the band, and insertion losses vary from 0.2-2.5 dB between Port 1 (Tx/Rx) and Port 2(Tx) while maintaining the isolation within 22 -26 dB between Port 2 (Tx) and Port 3 (Rx) when D_1 is ON and D_2 is OFF state, respectively at 27-28.5 GHz. Similarly, Figures 3.11 (a) and 3.11 (b) present the simulated and measured results for the reflection coefficients and insertion losses with the isolations maintained around 21-26 dB between Port 3 (Rx) and 2 (Tx) when D_1 is OFF state and D_2 is ON state, respectively at 27-28.5 GHz. The simulated results are validated with measured results in the frequency range of 27-28.5 GHz from Agilent N5234A Network Analyzer with DC supply HMP4030, where the measured results followed the simulated results with a slight deviation due to

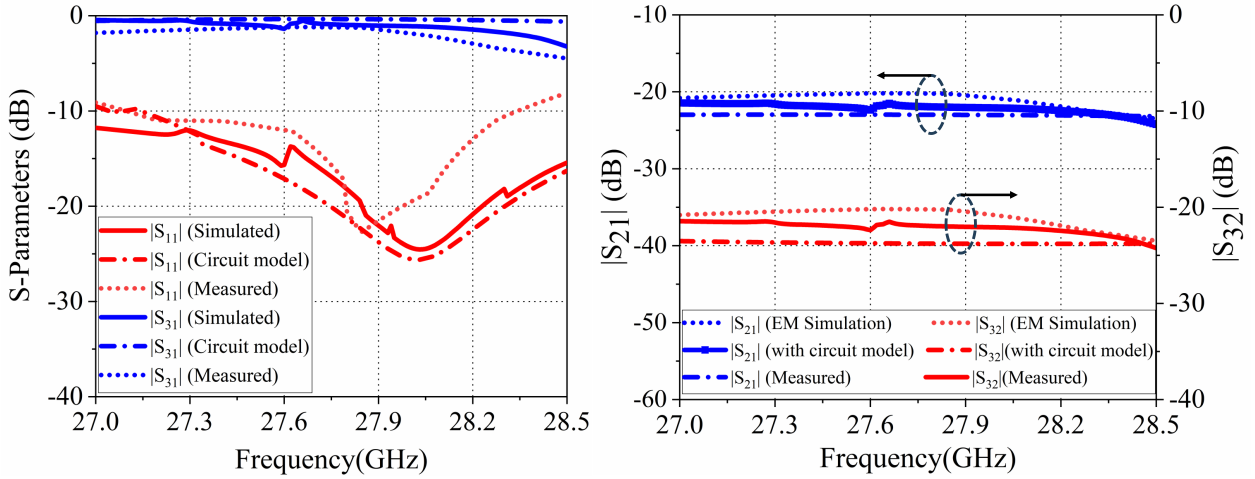


Figure 3.11 : (a) Performance of the SPDT switch circuit results in reflection coefficient ($|S_{11}|$) and insertion loss ($|S_{31}|$) from Tx/Rx to Tx channel; (b) isolations ($|S_{12}|$) and ($|S_{32}|$) between Port 1(Tx/Rx)-2 (Tx) and Port 2(Tx)-3(Rx) where $V_1 = -4$ V and $V_2 = 0.9$ V.

Table 3.1 : Comparisons of the proposed SPDT switch with the previous SPDT switch's

Ref.	**Tech.**	**Tx/Rx Center Freq (GHz)**	**Tx to Rx Iso (dB)**	**RL (dB)**	**IL (dB)**	**Electrical size (λ_g^2)**	**Fabrication complexity**
[Misran *et al.*, 2012].	ML	2.4/2.4	13.8	16.8	0.58	Not Fabricated	NA
[Hansen *et al.*, 2016].	ML	2.3/2.3* and 9.4/9.4*	15.39	15.27	1.89	2.1 and 35.22	Easy#1
[Rave *et al.*, 2014b].	ML	9.4/9.4*	30	16	2.4	2.2	Easy#1
[Shairi *et al.*, 2011b].	ML	1.75/1.75*	25	NM	1.8	NM	Easy#1
[Shairi *et al.*, 2011a].	ML with DGS	2.4/2.4*	13.7	NM	0.91	NM	Easy#1
[Chen *et al.*, 2016].	HMSIW	5/5*	28.5	15	1.78	2.9	Medium #1
[Lim and Lim, 2014].	SIW	10/10*	18	25	1.6	18.94	Medium #1
[Jang *et al.*, 2018].	65 nm CMOS	28/28 (mmWave frequency)	24	14	1.8	NM	Difficult #2
TW.	**SICL**	**28/28 (mmWave frequency)**	**26**	**20**	**1.7**	**17.26**	**Medium** #1

Tech:Technology, ML:Microstrip line, DGS:Defective ground structure, NM:Not Mentioned, NA: Not Applicable, RL:Return Loss, IL:Insertion Loss, #1 Low-cost PCB technology, #2 High-cost RFIC fabrication technology,* Microwave frequency.

fabrication tolerance and connector loss [Fooks and Zakarevicius, 1990b].

The design and development of the SPDT switch circuit for duplexer application are presented in this chapter. The results obtained from simulation and measurement are in good agreement. The results of the SPDT switch exhibit less than 2 dB insertion loss in 27-27.9 GHz and less than 2.5 dB insertion loss in 27.9-28.5 GHz with better impedance matching in the transmit (Tx) and receive (Rx) channel from Tx/Rx channel. The proposed design is realized with a low-cost PCB design technique. It is suitable for millimeter wave active circuits and communication systems application.

3.4 CONCLUSION

The proposed design employs Substrate Integrated Coaxial Line (SICL) technology to develop a single-pole double-throw (SPDT) switch in a low-profile planar configuration, enabling efficient time division duplexing (TDD) operation. This design marks a significant milestone as the first reported planar SPDT switch for duplexer applications utilizing SICL technology within the 27–28.5 GHz frequency range. The innovative use of SICL offers multiple advantages, particularly

in maintaining compactness and ensuring robust performance at millimeter-wave frequencies.One of the key attributes of this design is its self-shielded structure, which significantly enhances electromagnetic isolation and reduces unwanted coupling effects. Unlike conventional microstrip or coplanar waveguide (CPW) implementations, SICL confines the electromagnetic fields within the coaxial structure, thereby improving signal integrity and minimizing interference. This is particularly beneficial for high-frequency applications where maintaining signal purity is crucial. Furthermore, the proposed design integrates Surface Mount Device (SMD) components with SICL technology, enabling enhanced modularity and ease of fabrication. This integration facilitates the incorporation of essential circuit elements such as capacitors, resistors, inductors, diodes, and transistors within the SICL environment without requiring complex manufacturing processes. The ability to seamlessly combine active and passive components within the SICL platform paves the way for more sophisticated millimeter-wave systems, enhancing their functionality and commercial viability. A distinctive feature of this SPDT switch is the implementation of an RF isolation network within an asymmetric stripline configuration. To further optimize isolation performance, a strategically placed butterfly stub is introduced in the middle layer of the structure. This stub effectively minimizes signal leakage and reduces the risk of spurious radiation. Such an approach ensures minimal insertion loss and high isolation between the switching states, making the design suitable for high-performance communication systems operating in the millimeter-wave spectrum. Moreover, the top and bottom copper plates of the SICL structure provide inherent shielding against external RF interference, ensuring minimal electromagnetic radiation loss. This shielding mechanism enhances the overall reliability and efficiency of the circuit, particularly in complex RF environments where multiple active and passive circuits operate simultaneously. By leveraging the self-shielded nature of SICL, the proposed design achieves superior isolation characteristics while maintaining a low-loss transmission path. In summary, the development of this SICL-based SPDT switch represents a breakthrough in millimeter-wave circuit design. The integration of SMD components within the SICL framework, coupled with an optimized RF isolation network, demonstrates the potential of SICL technology in realizing highly efficient and compact RF front-end components. The proposed design not only improves signal integrity and operational efficiency but also provides a cost-effective solution for millimeter-wave communication systems, making it a strong candidate for next-generation wireless and satellite applications.